# LM5008A 95-V, 350-mA, Constant On-Time DC/DC Buck Switching Regulator

## 1 Features

- Operating Input Voltage Range: 6 V to 95 V
- Integrated 100-V N-Channel Buck Switch
- Internal Start-Up Regulator
- No Loop Compensation Required
- Ultra-Fast Transient Response
- On-Time Varies Inversely With Input Voltage
- Operating Frequency Remains Constant With Varying Line Voltage and Load Current
- Adjustable Output Voltage From 2.5 V
- Highly Efficient Operation
- Precision Internal Reference
- Low Bias Current
- Intelligent Current Limit
- Thermal Shutdown
- 8-Pin VSSOP and 8-Pin WSON Packages
- Create a Custom Design Using the LM5008A With the WEBENCH® Power Designer

## 2 Applications

- Non-Isolated Telecommunication Buck Regulators
- Secondary High-Voltage Post Regulators
- 48-V Automotive Systems

## 3 Description

The LM5008A DC/DC converter is a functional variant of the LM5008 COT Buck Switching Regulator. The functional differences of the LM5008A are: the minimum input operating voltage is 6 V, the on-time equation is slightly different, and the requirement for a minimum load current is removed.

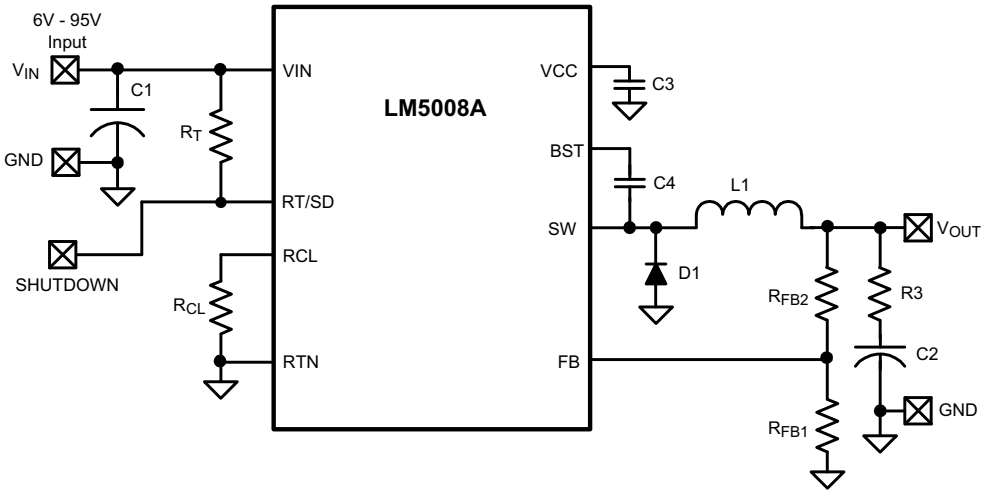
The LM5008A 350-mA step-down switching regulator features all of the functions required to implement a low-cost and efficient buck regulator. This high-voltage converter has an integrated 100-V N-channel buck switch and operates over an input voltage range of 6 V to 95 V. The device is easy to implement and is provided in 8-pin VSSOP and the thermally enhanced 8-pin WSON packages. The converter uses PWM control scheme with an on-time inversely proportional to $V_{IN}$. This feature allows the operating frequency to remain relatively constant. The control scheme requires no loop compensation. An intelligent current limit is implemented with forced off-time, which is inversely proportional to $V_{OUT}$. This scheme ensures short-circuit control while providing minimum foldback. Other features include: thermal shutdown, $V_{CC}$ undervoltage lockout, gate drive undervoltage lockout, maximum duty cycle limiter, and a pre-charge switch.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| LM5008A | VSSOP (8) | 3.00 mm × 3.00 mm |
| | WSON (8) | 4.00 mm × 4.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Typical Application, Basic Step-Down Regulator**



## Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision G (December 2016) to Revision H** **Page**

- Added links for WEBENCH ... 1
- Changed VSSOP-8 body size to 3 mm × 3 mm in *Device Information* ... 1

**Changes from Revision F (March 2013) to Revision G** **Page**

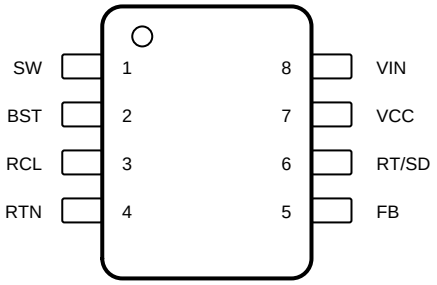
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted Lead temperature (260°C maximum) ... 4
- Changed $R_{\theta JA}$ value From: 200°C/W To: 139.7°C/W (VSSOP) and From: 40°C/W To: 42°C/W (WSON) ... 4

**Changes from Revision E (March 2013) to Revision F** **Page**

- Changed layout of National Data Sheet to TI format ... 17

# 5 Pin Configuration and Functions

**DGK Package**
**8-Pin VSSOP**
**Top View**

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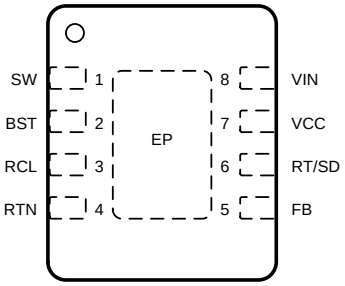
**NGU Package**
**8-Pin WSON**
**Top View**

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**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | SW | P | Switching node: power switching node. Connect to the output inductor, re-circulating diode, and bootstrap capacitor. |
| 2 | BST | I | Boost pin (bootstrap capacitor input): an external capacitor is required between the BST and the SW pins. A 0.01-µF ceramic capacitor is recommended. An internal diode charges the capacitor from $V_{CC}$ during each off-time. |
| 3 | RCL | I | Current limit off-time set pin: a resistor between this pin and RTN sets the off-time when current limit is detected. The off-time is preset to 35 µs if FB = 0 V. |
| 4 | RTN | G | Ground pin: ground for the entire circuit. |
| 5 | FB | I | Feedback input from regulated output: this pin is connected to the inverting input of the internal regulation comparator. The regulation threshold is 2.5 V. |
| 6 | RT/SD | I | On-time set pin: a resistor between this pin and VIN sets the switch on time as a function of $V_{IN}$. The minimum recommended on time is 400 ns at the maximum input voltage. This pin can be used for remote shutdown. |
| 7 | VCC | P | Output from the internal high voltage series pass regulator: this regulated voltage provides gate drive power for the internal buck switch. An internal diode is provided between this pin and the BST pin. A local 0.47-µF decoupling capacitor is required. The series pass regulator is current limited to 9 mA. |
| 8 | VIN | P | Input voltage: input operating range from 6 V to 95 V. |
| — | EP | G | Exposed pad: the exposed pad has no electrical contact. Connect to system ground plane for reduced thermal resistance. (WSON package only) |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| $V_{IN}$ to GND | –0.3 | 100 | V |
| BST to GND | –0.3 | 114 | V |
| SW to GND (steady-state) | | –1 | V |
| BST to $V_{CC}$ | | 100 | V |
| BST to SW | | 14 | V |
| $V_{CC}$ to GND | | 14 | V |
| All other inputs to GND | –0.3 | 7 | V |
| Storage temperature, $T_{stg}$ | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| $V_{IN}$ | 6 | 95 | V |
| Operating junction temperature | –40 | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | LM5008A | | UNIT |
|---|---|---|---|---|
| | | DGK (VSSOP) | NGU (WSON) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 139.7 | 42 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 51.2 | 27.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 70.5 | 18.5 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 3.4 | 0.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 69.5 | 18.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | 4.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

$T_J$ = 25°C and $V_{IN}$ = 48 V (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **VCC SUPPLY** | | | | | | | |
| $V_{CC}$ Reg | $V_{CC}$ regulator output | $V_{IN}$ = 48 V | $T_J$ = 25°C | | 7 | | V |
| | | | $T_J$ = –40°C to 125°C | 6.6 | | 7.4 | |
| | $V_{IN} – V_{CC}$ | 6 V < $V_{IN}$ < 8.5 V | | | 100 | | mV |
| | $V_{CC}$ bypass threshold | $V_{IN}$ increasing | | | 8.5 | | V |
| | $V_{CC}$ bypass hysteresis | | | | 300 | | mV |
| | $V_{CC}$ output impedance | $V_{IN}$ = 6 V | | | 100 | | Ω |
| | | $V_{IN}$ = 10 V | | | 8.8 | | Ω |
| | | $V_{IN}$ = 48 V | | | 0.8 | | Ω |
| | $V_{CC}$ current limit | $V_{IN}$ = 48 V | | | 9.2 | | mA |
| | $V_{CC}$ UVLO | $V_{CC}$ increasing | | | 5.3 | | V |
| | $V_{CC}$ UVLO hysteresis | | | | 190 | | mV |
| | $V_{CC}$ UVLO filter delay | | | | 3 | | µs |
| | $I_{IN}$ operating current | FB = 3 V, $V_{IN}$ = 48 V | $T_J$ = 25°C | | 550 | | µA |
| | | | $T_J$ = –40°C to 125°C | | | 750 | |
| | $I_{IN}$ shutdown current | RT/SD = 0 V | $T_J$ = 25°C | | 110 | | µA |
| | | | $T_J$ = –40°C to 125°C | | | 176 | |
| **CURRENT LIMIT** | | | | | | | |
| | Current limit threshold | $T_J$ = 25°C | | | 0.51 | | A |
| | | $T_J$ = –40°C to 125°C | | 0.41 | | 0.61 | |
| | Current limit response time | $I_{switch}$ overdrive = 0.1 A, time to switch off | | | 350 | | ns |
| $T_{OFF-1}$ | Off-time generator | FB = 0 V, $R_{CL}$ = 100 kΩ | | | 35 | | µs |
| $T_{OFF-2}$ | Off-time generator | FB = 2.3 V, $R_{CL}$ = 100 kΩ | | | 2.56 | | µs |
| **ON-TIME GENERATOR** | | | | | | | |
| | $T_{ON}$ – 1 | $V_{IN}$ = 10 V, $R_{ON}$ = 200 kΩ | $T_J$ = 25°C | | 2.77 | | µs |
| | | | $T_J$ = –40°C to 125°C | 2.15 | | 3.5 | |
| | $T_{ON}$ – 2 | $V_{IN}$ = 95 V, $R_{ON}$ = 200 kΩ | $T_J$ = 25°C | | 300 | | ns |
| | | | $T_J$ = –40°C to 125°C | 200 | | 420 | |
| | Remote shutdown threshold | Rising | $T_J$ = 25°C | | 0.7 | | V |
| | | | $T_J$ = –40°C to 125°C | 0.4 | | 1.05 | |
| | Remote shutdown hysteresis | | | | 35 | | mV |
| **MINIMUM OFF-TIME** | | | | | | | |
| | Minimum off-timer | $V_{FB}$ = 0 V | | | 300 | | ns |
| **REGULATION AND OV COMPARATORS** | | | | | | | |
| | FB reference threshold | Internal reference, trip point for switch ON | $T_J$ = 25°C | | 2.5 | | V |
| | | | $T_J$ = –40°C to 125°C | 2.445 | | 2.55 | |
| | FB overvoltage threshold | Trip point for switch OFF | | | 2.875 | | V |
| | FB bias current | | | | 100 | | nA |
| **THERMAL SHUTDOWN** | | | | | | | |
| Tsd | Thermal shutdown temperature | | | | 165 | | °C |
| | Thermal shutdown hysteresis | | | | 25 | | °C |

(1) All electrical characteristics having room temperature limits are tested during production with $T_A$ = $T_J$ = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Buck switch $R_{DS(on)}$ | $I_{TEST}$ = 200 mA | $T_J$ = 25°C | | 1.25 | | Ω |
| | | $T_J$ = –40°C to 125°C | | | 2.57 | |
| Gate drive UVLO | $V_{BST} – V_{SW}$ rising | $T_J$ = 25°C | | 3.8 | | V |
| | | $T_J$ = –40°C to 125°C | 2.8 | | 4.8 | |
| Gate drive UVLO hysteresis | | | | 490 | | mV |
| Pre-charge switch voltage | At 1 mA | | | 0.8 | | V |
| Pre-charge switch on-time | | | | 150 | | ns |

## 6.7 Typical Characteristics

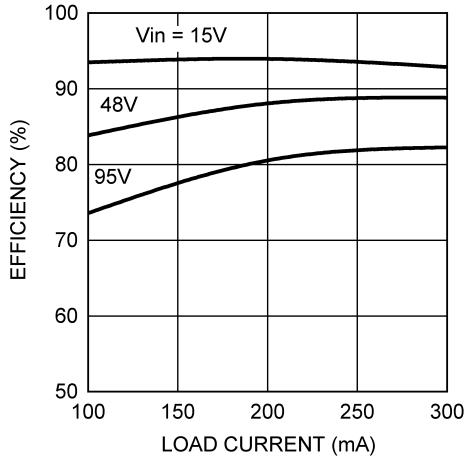



**Figure 1. Efficiency vs Load Current and $V_{IN}$ (Circuit of Figure 10)**

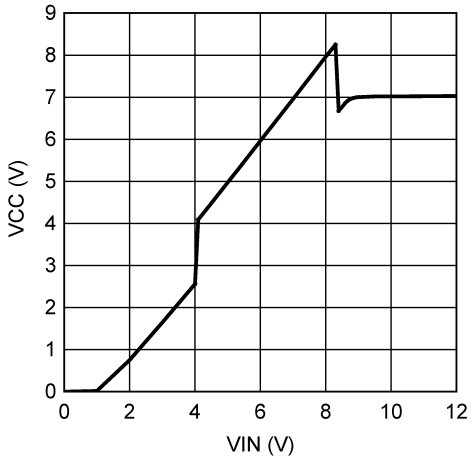



**Figure 2. $V_{CC}$ vs $V_{IN}$**

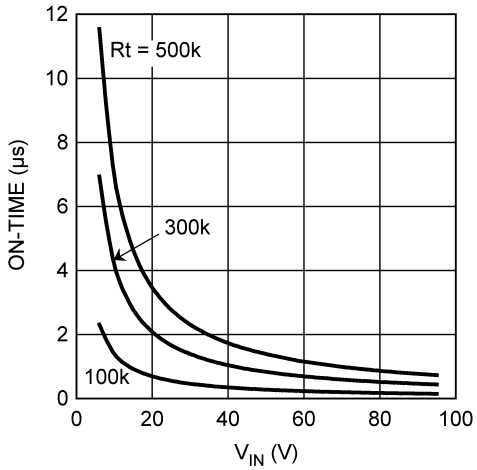



**Figure 3. On-Time vs Input Voltage and $R_T$**

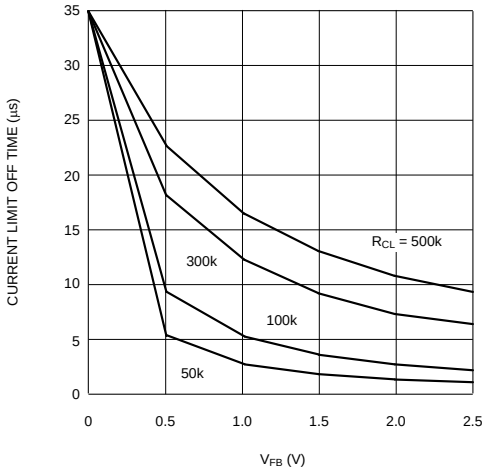



**Figure 4. Current Limit Off-Time vs $V_{FB}$ and $R_{CL}$**

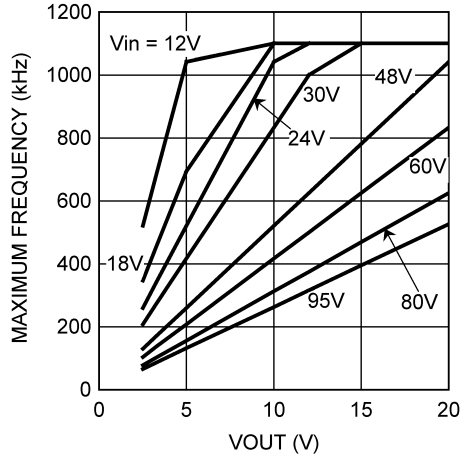



**Figure 5. Maximum Frequency vs $V_{OUT}$ and $V_{IN}$**

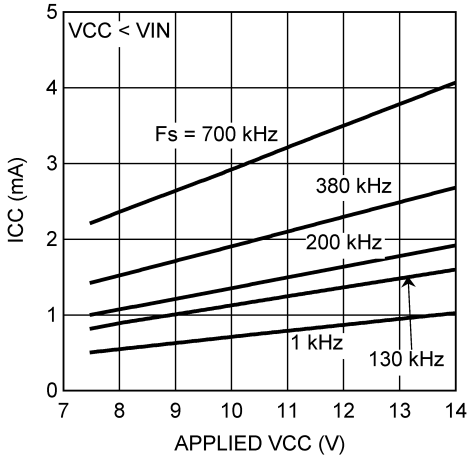



**Figure 6. $I_{CC}$ Current vs Applied $V_{CC}$ Voltage**

# 7 Detailed Description

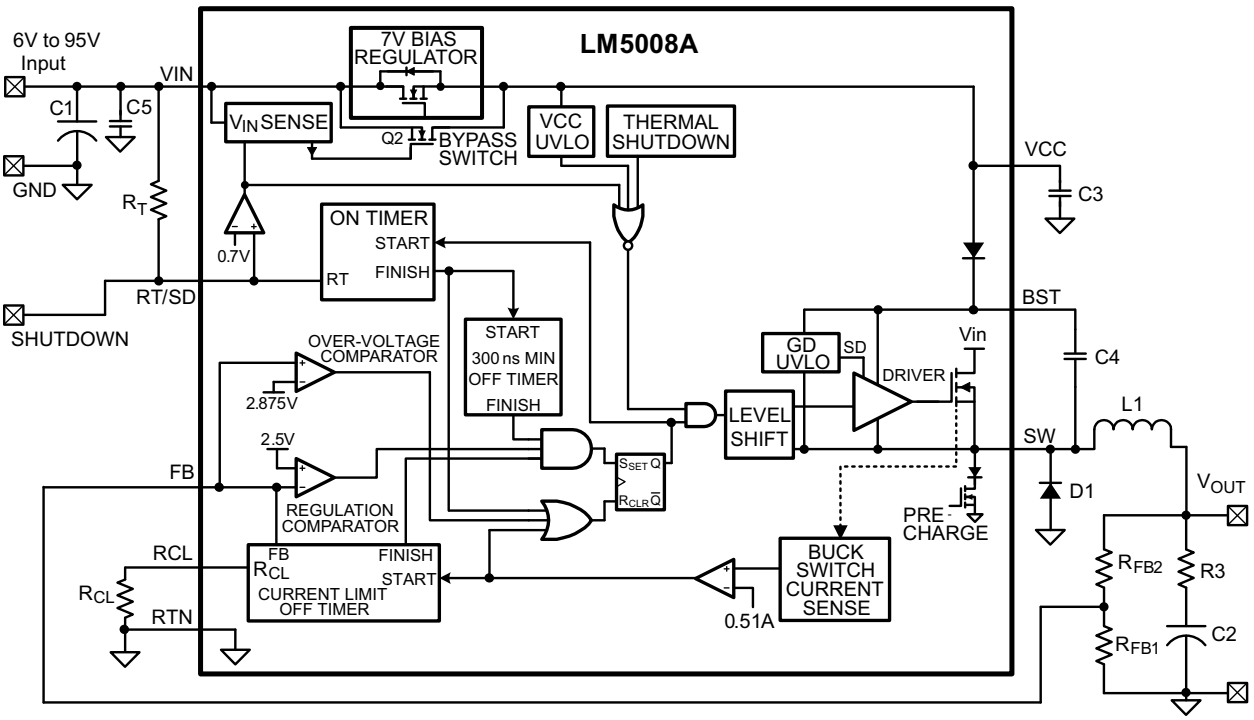
## 7.1 Overview

The LM5008A regulator is an easy-to-use buck DC-DC converter that operates from 6-V to 95-V supply voltage. The device is intended for step-down conversions from 12-V, 24-V, and 48-V unregulated, semi-regulated and fully-regulated supply rails. With integrated buck power MOSFET, the LM5008A delivers up to 350-mA DC load current with exceptional efficiency and low input quiescent current in a very small solution size.

Designed for simple implementation, a nearly fixed-frequency, constant on-time (COT) operation with discontinuous conduction mode (DCM) at light loads is ideal for low-noise, high current, fast transient load requirements. Control loop compensation is not required reducing design time and external component count.

The LM5008A incorporates other features for comprehensive system requirements, including VCC undervoltage lockout (UVLO), gate drive undervoltage lockout, maximum duty cycle limiter, intelligent current limit off-timer, a pre-charge switch, and thermal shutdown with automatic recovery. These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for simple and optimized PCB layout, requiring only a few external components.

## 7.2 Functional Block Diagram






## 7.3 Feature Description

### 7.3.1 Control Circuit Overview

The LM5008A is a buck DC-DC regulator that uses a control scheme in which the on-time varies inversely with line voltage ($V_{IN}$). Control is based on a comparator and the on-time one-shot, with the output voltage feedback (FB) compared to an internal reference (2.5 V). If the FB level is below the reference the buck switch is turned on for a fixed time determined by the line voltage and a programming resistor ($R_T$). Following the ON period, the switch remains off for at least the minimum off-timer period of 300 ns. If FB is still below the reference at that time, the switch turns on again for another on-time period. This continues until regulation is achieved.

## Feature Description (continued)

The LM5008A operates in discontinuous conduction mode at light load currents, and continuous conduction mode at heavy load current. In discontinuous conduction mode, current through the output inductor starts at zero and ramps up to a peak during the on-time, then ramps back to zero before the end of the off-time. The next on-time period starts when the voltage at FB falls below the internal reference; until then, the inductor current remains zero. In this mode, the operating frequency is lower than in continuous conduction mode and varies with load current. Therefore, at light loads, the conversion efficiency is maintained because the switching losses reduce with the reduction in load and frequency. The discontinuous operating frequency can be calculated with Equation 1.

$$F = \frac{V_{OUT}^2 \times L \times 1.04 \times 10^{20}}{R_L \times (R_T)^2} \quad (1)$$

where

- $R_L$ = the load resistance

In continuous conduction mode, current flows continuously through the inductor and never ramps down to zero. In this mode the operating frequency is greater than the discontinuous mode frequency and remains relatively constant with load and line variations. The approximate continuous mode operating frequency can be calculated with Equation 2.

$$F = \frac{V_{OUT}}{1.385 \times 10^{-10} \times R_T} \quad (2)$$

The output voltage ($V_{OUT}$) is programmed by two external resistors as shown in the *Functional Block Diagram*. The regulation point can be calculated with Equation 3.

$$V_{OUT} = 2.5 \times (R_{FB1} + R_{FB2}) / R_{FB1} \quad (3)$$

The LM5008A regulates the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor C2. A minimum of 25 mV to 50 mV of ripple voltage at the feedback pin (FB) is required for the LM5008A. In cases where the capacitor ESR is too small, additional series resistance may be required (R3 in the *Functional Block Diagram*).

For applications where lower output voltage ripple is required, the output can be taken directly from a low-ESR output capacitor as shown in Figure 7. However, R3 slightly degrades the load regulation.

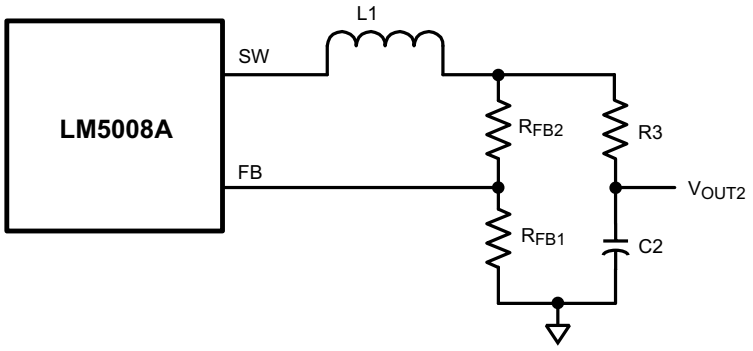





**Figure 7. Low-Ripple Output Configuration**

### 7.3.2 Start-Up Regulator ($V_{CC}$)

The high voltage bias regulator is integrated within the LM5008A. The input pin (VIN) can be connected directly to line voltages between 6 V and 95 V, with transient capability to 100 V. Referring to the *Functional Block Diagram* and Figure 2, when $V_{IN}$ is between 6 V and the bypass threshold (nominally 8.5 V), the bypass switch (Q2) is on, and $V_{CC}$ tracks $V_{IN}$ within 100 mV to 150 mV. The bypass switch on-resistance is approximately 100 Ω, with inherent current limiting at approximately 100 mA. When $V_{IN}$ is above the bypass threshold Q2 is turned off, and $V_{CC}$ is regulated at 7 V. The $V_{CC}$ regulator output current is limited at approximately 9.2 mA. When the LM5008A is shut down using the RT/SD pin, the $V_{CC}$ bypass switch is shut off regardless of the voltage at $V_{IN}$.

## Feature Description (continued)

When VIN exceeds the bypass threshold, the time required for Q2 to shut off is approximately 2 µs to 3 µs. The capacitor at VCC (C3) must be a minimum of 0.47 µF to prevent the voltage at $V_{CC}$ from rising above its absolute maximum rating in response to a step input applied at $V_{IN}$. C3 must be placed as close as possible to the VCC and RTN pins. In applications with a relatively high input voltage, power dissipation in the bias regulator is a concern. An auxiliary voltage of between 7.5 V and 14 V can be diode connected to the VCC pin to shut off the $V_{CC}$ regulator, thereby reducing internal power dissipation. The current required into the VCC pin is shown in Figure 6. Internally a diode connects VCC to VIN requiring that the auxiliary voltage be less than $V_{IN}$.

The turnon sequence is shown in Figure 8. During the initial delay (t1), VCC ramps up at a rate determined by its current limit and C3 while internal circuitry stabilizes. When $V_{CC}$ reaches the upper threshold of its undervoltage lockout (UVLO, typically 5.3 V), the buck switch is enabled. The inductor current increases to the current limit threshold ($I_{LIM}$), and during t2 the $V_{OUT}$ increases as the output capacitor charges up. When $V_{OUT}$ reaches the intended voltage the average inductor current decreases (t3) to the nominal load current ($I_O$).

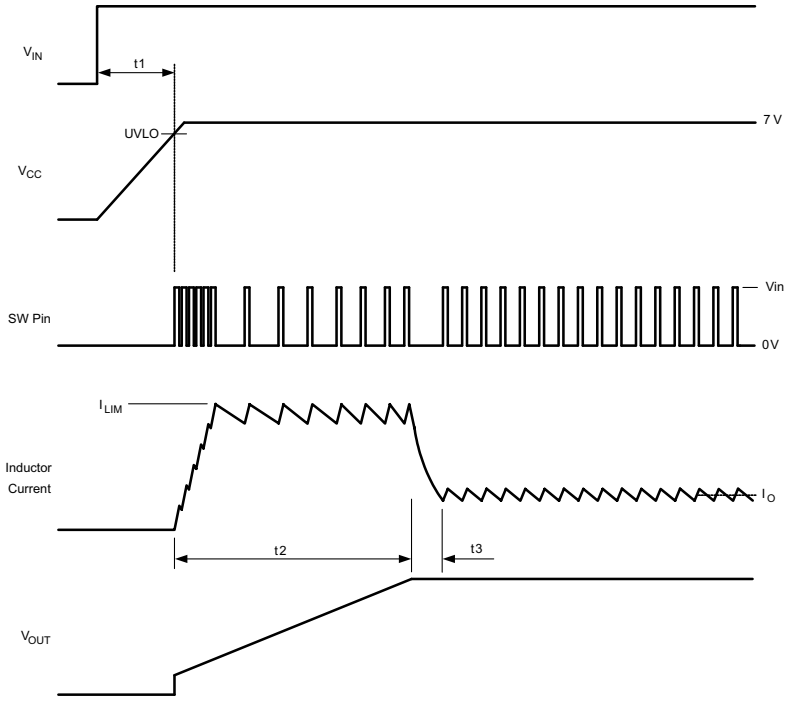



**Figure 8. Start-Up Sequence**

### 7.3.3 Regulation Comparator

The feedback voltage at FB is compared to an internal 2.5-V reference. In normal operation (the output voltage is regulated), an on-time period is initiated when the voltage at FB falls below 2.5 V. The buck switch stays on for the on-time, causing the FB voltage to rise above 2.5 V. After the on-time period, the buck switch stays off until the FB voltage again falls below 2.5 V. During start-up, the FB voltage is below 2.5 V at the end of each on-time, resulting in the minimum off-time of 300 ns. Bias current at the FB pin is nominally 100 nA.

### 7.3.4 Overvoltage Comparator

The feedback voltage at FB is compared to an internal 2.875-V reference. If the voltage at FB rises above 2.875 V, the on-time pulse is immediately terminated. This condition can occur if the input voltage or the output load change suddenly. The buck switch does not turn on again until the voltage at FB falls below 2.5 V.

### 7.3.5 On-Time Generator and Shutdown

The on-time for the LM5008A is determined by the $R_T$ resistor and is inversely proportional to the input voltage ($V_{IN}$), resulting in a nearly constant frequency as Vin is varied over its range. The on-time equation for the LM5008A is Equation 4.

## Feature Description (continued)

$$T_{ON} = 1.385 \times 10^{-10} \times R_T / V_{IN} \quad (4)$$

$R_T$ must be selected for a minimum on-time (at maximum $V_{IN}$) greater than 400 ns, for proper current limit operation. This requirement limits the maximum frequency for each application, depending on $V_{IN}$ and $V_{OUT}$.

The LM5008A can be remotely disabled by taking the $R_T$/SD pin to ground. See Figure 9. The voltage at the $R_T$/SD pin is between 1.5 V and 3 V, depending on $V_{IN}$ and the value of the $R_T$ resistor.

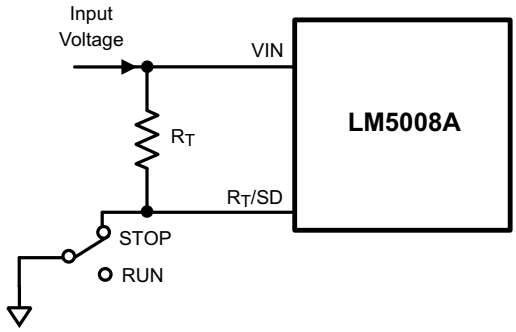





**Figure 9. Shutdown Implementation**

### 7.3.6 Current Limit

The LM5008A contains an intelligent current limit OFF timer. If the current in the Buck switch exceeds 0.51 A the present cycle is immediately terminated and a non-resetable OFF timer is initiated. The length of off-time is controlled by an external resistor ($R_{CL}$) and the FB voltage (see Figure 4). When FB = 0 V, a maximum off-time is required, and the time is preset to 35 µs. This condition occurs when the output is shorted and during the initial part of start-up. This amount of time ensures safe short-circuit operation up to the maximum input voltage of 95 V. In cases of overload where the FB voltage is above zero volts (not a short circuit), the current limit off-time is less than 35 µs. Reducing the off-time during less severe overloads reduces the amount of foldback, recovery time, and the start-up time. The off-time is calculated from Equation 5.

$$T_{OFF} = \frac{10^{-5}}{0.285 + \frac{V_{FB}}{\left(6.35 \times 10^{-6} \times R_{CL}\right)}} \quad (5)$$

The current limit-sensing circuit is blanked for the first 50 ns to 70 ns of each on-time, so it is not falsely tripped by the current surge which occurs at turnon. The current surge is required by the re-circulating diode (D1) for its turnoff recovery.

### 7.3.7 N-Channel Buck Switch and Driver

The LM5008A integrates an N-Channel Buck switch and associated floating high voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. A 0.01-µF ceramic capacitor (C4) connected between the BST pin and SW pin provides the voltage to the driver during the on-time.

During each off-time, the SW pin is at approximately 0 V and the bootstrap capacitor charges from $V_{CC}$ through the internal diode. The minimum off-timer, set to 300 ns, ensures a minimum time each cycle to recharge the bootstrap capacitor.

The internal pre-charge switch at the SW pin is turned on for ≅ 150 ns during the minimum off-time period, ensuring sufficient voltage exists across the bootstrap capacitor for the on-time. This feature helps prevent operating problems which can occur during very light-load conditions, involving a long off-time, during which the voltage across the bootstrap capacitor could otherwise reduce below the Gate Drive UVLO threshold. The pre-charge switch also helps prevent start-up problems which can occur if the output voltage is pre-charged prior to turnon. After current limit detection, the pre-charge switch is turned on for the entire duration of the forced off-time.

## Feature Description (continued)

### 7.3.8 Thermal Protection

The LM5008A must be operated so the junction temperature does not exceed 125°C during normal operation. An internal Thermal Shutdown circuit is provided to shutdown the LM5008A in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low-power reset state by disabling the buck switch. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature reduces below 140°C (typical hysteresis = 25°C), normal operation is resumed.

## 7.4 Device Functional Modes

### 7.4.1 Shutdown Mode

The RT/SD pin provides ON and OFF control for the LM5008A. When $V_{SD}$ is below approximately 0.7 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 110 µA (typical) at $V_{IN}$ = 48 V. The LM5008A also employs $V_{CC}$ bias rail undervoltage protection. If the $V_{CC}$ bias supply voltage is below its UV threshold, the regulator remains off.

### 7.4.2 Active Mode

LM5008A is in active mode when the internal bias rail, VCC, is above its UV threshold. Depending on the load current, the device operates in either DCM or CCM mode.

Whenever the load current is reduced to a level less than half the peak-to-peak inductor ripple current, the device enters discontinuous conduction mode (DCM). Calculate the critical conduction boundary using Equation 6.

$$I_{BOUNDARY} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \cdot (1 - D)}{2 \cdot L_F \cdot F_{SW}} \quad (6)$$

When the inductor current reaches zero, the SW node becomes high impedance. Resonant ringing occurs at SW as a result of the LC tank circuit formed by the buck inductor and the parasitic capacitance at the SW node. At light loads, several pulses may be skipped in between switching cycles, effectively reducing the switching frequency and further improving light-load efficiency.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

LM5008A requires only a few external components to convert from a wide range of supply voltages to a fixed output voltage. To expedite and streamline the process of designing a LM5008A-based converter, a comprehensive LM5008A Quick-Start tool is available for download to assist the designer with component selection for a given application. WEBENCH® online software is also available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following sections discuss a design procedure using a typical application example. Figure 10 shows the LM5008A in a configuration suitable for several application use cases. See the LM5008A EVM for more details.

## 8.2 Typical Application

The final circuit is shown in Figure 10. The circuit was tested, and the resulting performance is shown in Figure 14 and Figure 15.

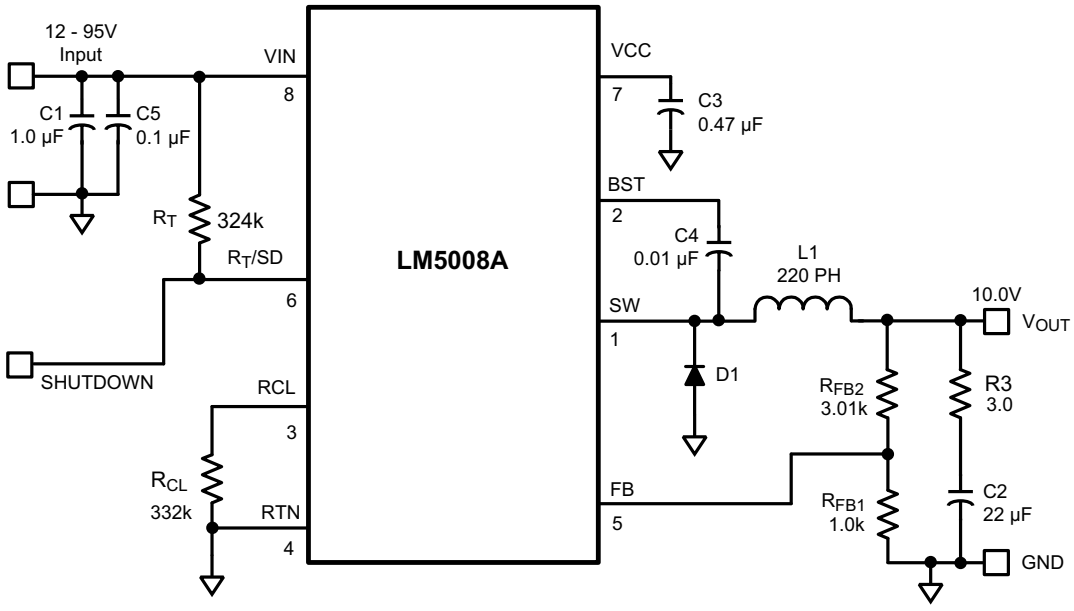





**Figure 10. LM5008A Example Circuit**

### 8.2.1 Design Requirements

A guide for determining the component values is shown in Figure 10. Table 1 lists the bill of materials for this application example. The following steps configure the LM5008A:

- Input voltage range ($V_{IN}$): 12 V to 95 V
- Output voltage ($V_{OUT1}$): 10 V
- Load current (for continuous conduction mode): 100 mA to 300 mA

## Typical Application (continued)

**Table 1. Bill of Materials**

| ITEM | DESCRIPTION | PART NUMBER | VALUE |
|---|---|---|---|
| C1 | Ceramic Capacitor | TDK C4532X7R2A105M | 1 µF, 100 V |
| C2 | Ceramic Capacitor | TDK C4532X7R1E226M | 22 µF, 25 V |
| C3 | Ceramic Capacitor | Kemet C1206C474K5RAC | 0.47 µF, 50 V |
| C4 | Ceramic Capacitor | Kemet C1206C103K5RAC | 0.01 µF, 50 V |
| C5 | Ceramic Capacitor | TDK C3216X7R2A104M | 0.1 µF, 100 V |
| D1 | Schottky Power Diode | Diodes Inc. DFLS1100 | 100 V, 1 A |
| L1 | Power Inductor | COILTRONICS DR125-221-R or TDK SLF10145T-221MR65 | 220 µH |
| $R_{FB2}$ | Resistor | Vishay CRCW12063011F | 3.01 kΩ |
| $R_{FB1}$ | Resistor | Vishay CRCW12061001F | 1.0 kΩ |
| R3 | Resistor | Vishay CRCW12063R00F | 3.0 Ω |
| $R_T$ | Resistor | Vishay CRCW12063243F | 324 kΩ |
| $R_{CL}$ | Resistor | Vishay CRCW12063323F | 332 kΩ |
| U1 | Switching Regulator | LM5008A | |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Custom Design With WEBENCH® Tools*

Click here to create a custom design using the LM5008A device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

#### *8.2.2.2 Selection Of External Components*

**$R_{FB1}$, $R_{FB2}$:** $V_{OUT} = V_{FB} \times (R_{FB1} + R_{FB2}) / R_{FB1}$, and because $V_{FB}$ = 2.5 V, the ratio of $R_{FB2}$ to $R_{FB1}$ calculates as 3:1. Standard values of 3.01 kΩ and 1 kΩ are chosen. Other values could be used as long as the 3:1 ratio is maintained.

**$F_s$ and $R_T$:** The recommended operating frequency range for the LM5008A is 50 kHz to 1.1 MHz. Unless the application requires a specific frequency, the choice of frequency is generally a compromise because it affects the size of L1 and C2 and the switching losses. The maximum allowed frequency, based on a minimum on-time of 400 ns, is calculated with Equation 7.

$$F_{MAX} = V_{OUT} / (V_{INMAX} \times 400\ ns) \quad (7)$$

For this exercise, $F_{MAX}$ = 263 kHz. From Equation 2, $R_T$ calculates to 274 kΩ. A standard value 324-kΩ resistor is used to allow for tolerances in Equation 2, resulting in a frequency of 223 kHz.

**L1:** The main parameter affected by the inductor is the output current ripple amplitude. The choice of inductor value therefore depends on both the minimum and maximum load currents, keeping in mind that the maximum ripple current occurs at maximum $V_{IN}$.

a. **Minimum load current:** To maintain continuous conduction at minimum Io (100 mA), the ripple amplitude

($I_{OR}$) must be less than 200 mAp-p so the lower peak of the waveform does not reach zero. L1 is calculated using Equation 8.

$$L1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{OR} \times F_s \times V_{IN}} \quad (8)$$

At $V_{IN}$ = 95 V, L1 (minimum) calculates to 200 µH. The next larger standard value (220 µH) is chosen and with this value $I_{OR}$ calculates to 182 mAp-p at $V_{IN}$ = 95 V, and 34 mAp-p at $V_{IN}$ = 12 V.

b. **Maximum load current:** At a load current of 300 mA, the peak of the ripple waveform must not reach the minimum value of the LM5008A's current limit threshold (410 mA). Therefore the ripple amplitude must be less than 220 mAp-p, which is already satisfied in Equation 8. With L1 = 220 µH, at maximum $V_{IN}$ and $I_O$, the peak of the ripple is 391 mA. While L1 must carry this peak current without saturating or exceeding its temperature rating, it also must be capable of carrying the maximum value of the LM5008A's current limit threshold (610 mA) without saturating because the current limit is reached during start-up.

   The DC resistance of the inductor must be as low as possible. For example, if the inductor's DCR is 1 Ω, the power dissipated at maximum load current is 0.09 W. While small, it is not insignificant compared to the load power of 3 W.

**C3:** The capacitor on the $V_{CC}$ output provides not only noise filtering and stability, but its primary purpose is to prevent false triggering of the $V_{CC}$ UVLO at the buck switch on and off transitions. C3 must be no smaller than 0.47 µF.

**C2, and R3:** When selecting the output filter capacitor C2, the items to consider are ripple voltage due to its ESR, ripple voltage due to its capacitance, and the nature of the load.

**ESR and R3:** A low ESR for C2 is generally desirable to minimize power losses and heating within the capacitor. However, the regulator requires a minimum amount of ripple voltage at the feedback input for proper loop operation. For the LM5008A the minimum ripple required at pin 5 is 25 mVp-p, requiring a minimum ripple at $V_{OUT}$ of 100 mV. Because the minimum ripple current (at minimum $V_{IN}$) is 34 mA p-p, the minimum ESR required at $V_{OUT}$ is 100 mV / 34 mA = 2.94 Ω. Because quality capacitors for SMPS applications have an ESR considerably less than this, R3 is inserted as shown in the *Functional Block Diagram*. R3's value, along with C2's ESR, must result in at least 25 mVp-p ripple at pin 5. Generally, R3 is 0.5 to 3 Ω.

**$R_{CL}$:** When current limit is detected, the minimum off-time set by this resistor must be greater than the maximum normal off-time, which occurs at maximum input voltage. Using Equation 4, the minimum on-time is 472 ns, yielding an off-time of 4 µs (at 223 kHz). Due to the 25% tolerance on the on-time, the off-time tolerance is also 25%, yielding a maximum off-time of 5 µs. Allowing for the response time of the current limit detection circuit (350 ns) increases the maximum off-time to 5.35 µs. This is increased an additional 25% to 6.7 µs to allow for the tolerances of Equation 5. Using Equation 5, $R_{CL}$ calculates to 325 kΩ at $V_{FB}$ = 2.5 V. A standard value 332-kΩ resistor is used.

**D1:** The important parameters are reverse recovery time and forward voltage. The reverse recovery time determines how long the reverse current surge lasts each time the buck switch is turned on. The forward voltage drop is significant in the event the output is short-circuited as it is only this diode's voltage which forces the inductor current to reduce during the forced off-time. For this reason, a higher voltage is better, although that affects efficiency. A good choice is a Schottky power diode, such as the DFLS1100. D1's reverse voltage rating must be at least as great as the maximum $V_{IN}$, and its current rating be greater than the maximum current limit threshold (610 mA).

**C1:** This capacitor's purpose is to supply most of the switch current during the on-time, and limit the voltage ripple at $V_{IN}$, on the assumption that the voltage source feeding $V_{IN}$ has an output impedance greater than zero. At maximum load current, when the buck switch turns on, the current into pin 8 suddenly increases to the lower peak of the output current waveform, ramp up to the peak value, then drop to zero at turnoff. The average input current during this on-time is the load current (300 mA). For a worst-case calculation, C1 must supply this average load current during the maximum on-time. To keep the input voltage ripple to less than 2 V (for this exercise), C1 is calculated with Equation 9.

$$C1 = \frac{I \times t_{ON}}{\Delta V} = \frac{0.3A \times 3.74\ \mu S}{2.0\,V} = 0.56\ \mu F \quad (9)$$

Quality ceramic capacitors in this value have a low ESR which adds only a few millivolts to the ripple. It is the capacitance which is dominant in this case. To allow for the capacitor's tolerance, temperature effects, and voltage effects, a 1-µF, 100-V, X7R capacitor is used.

**C4:** The recommended value is 0.01 µF for C4, as this is appropriate in the majority of applications. A high-quality ceramic capacitor with low ESR is recommended as C4 supplies the surge current to charge the buck switch gate at turnon. A low ESR also ensures a quick recharge during each off-time. At minimum $V_{IN}$, when the on-time is at maximum, it is possible during start-up that C4 does not fully recharge during each 300-ns off-time. The circuit is not able to complete the start-up, and achieve output regulation. This can occur when the frequency is intended to be low (for example, $R_T$ = 500 K). In this case C4 must be increased so it can maintain sufficient voltage across the buck switch driver during each on-time.

**C5:** This capacitor helps avoid supply voltage transients and ringing due to long lead inductance at $V_{IN}$. A low-ESR, 0.1-µF ceramic chip capacitor is recommended placed close to the LM5008A.

### *8.2.2.3 Low-Output Ripple Configurations*

For applications where low-output ripple is required, the following options can be used to reduce or nearly eliminate the ripple:

a. **Reduced ripple configuration:** In Figure 11, Cff is added across $R_{FB2}$ to AC-couple the ripple at $V_{OUT}$ directly to the FB pin. This allows the ripple at $V_{OUT}$ to be reduced to a minimum of 25 mVp-p by reducing R3, because the ripple at $V_{OUT}$ is not attenuated by the feedback resistors. The minimum value for Cff is determined by Equation 10:

$$Cff = \frac{3 \times t_{ON(max)}}{(R_{FB1} // R_{FB2})} \quad (10)$$

where

- $t_{ON(max)}$ is the maximum on-time, which occurs at $V_{IN(min)}$. The next larger standard value capacitor must be used for Cff.

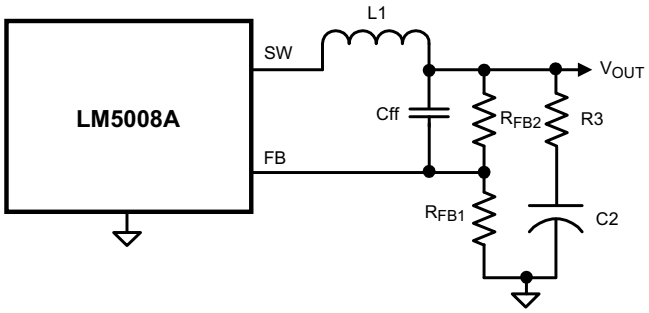





**Figure 11. Reduced Ripple Configuration**

b. **Minimum ripple configuration:** If the application requires a lower value of ripple (<10 mVp-p), the circuit of Figure 12 can be used. R3 is removed, and the resulting output ripple voltage is determined by the inductor's ripple current and C2's characteristics. RA and CA are chosen to generate a sawtooth waveform at their junction, and that voltage is AC-coupled to the FB pin through CB. To determine the values for RA, CA, and CB, use the following procedure in Equation 11:

Calculate $V_A = V_{OUT} – (V_{SW} \times (1 – (V_{OUT}/V_{IN(min)})))$ (11)

where

- $V_{SW}$ is the absolute value of the voltage at the SW pin during the off-time (typically 1 V). VA is the DC voltage at the RA/CA junction, and is used in Equation 12.

Calculate $RA \times CA = (V_{IN(min)} – V_A) \times t_{ON}/\Delta V$ (12)

where

- $t_{ON}$ is the maximum on-time (at minimum input voltage), and $\Delta V$ is the desired ripple amplitude at the RA/CA junction (typically 40-50 mV). RA and CA are then chosen from standard value components to satisfy the above product. Typically CA is 1000 pF to 5000 pF, and RA is 10 kΩ to 300 kΩ. CB is then chosen large compared to CA, typically 0.1 µF.

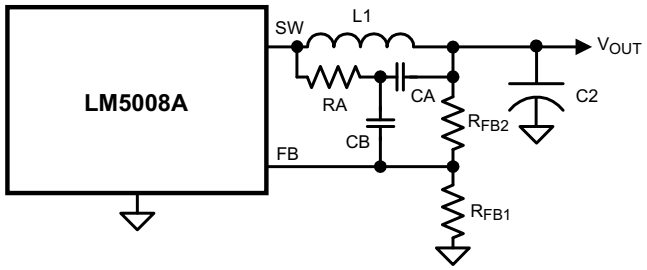





**Figure 12. Minimum Output Ripple Using Ripple Injection**

c. **Alternate minimum ripple configuration:** The circuit in Figure 13 is the same as that in the *Functional Block Diagram*, except the output voltage is taken from the junction of R3 and C2. The ripple at $V_{OUT}$ is determined by the inductor's ripple current and C2's characteristics. However, R3 slightly degrades the load regulation. This circuit may be suitable if the load current is fairly constant.

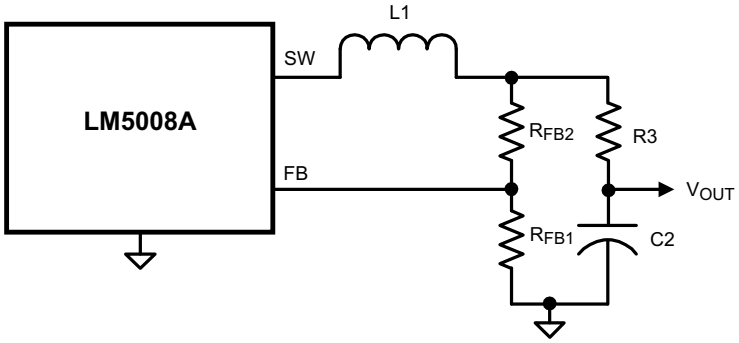





**Figure 13. Alternate Minimum Output Ripple Configuration**

### 8.2.3 Application Curves

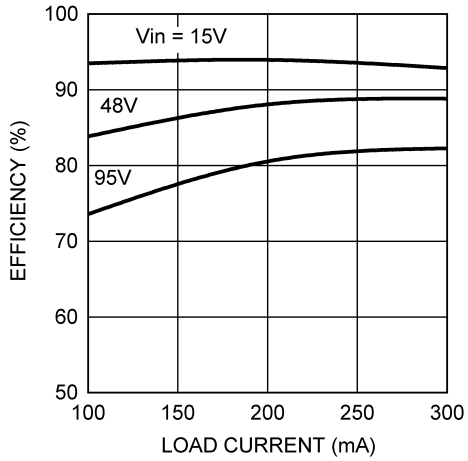



**Figure 14. Efficiency vs Load Current and $V_{IN}$**

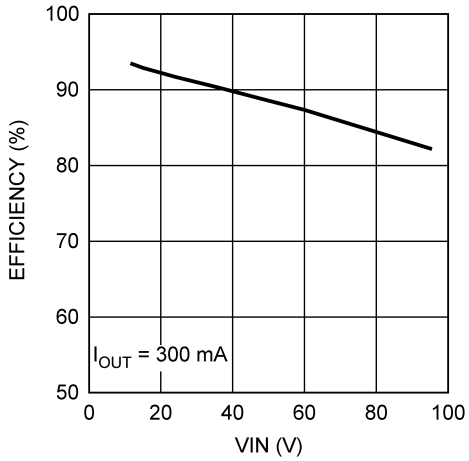



**Figure 15. Efficiency vs $V_{IN}$**

## 9 Power Supply Recommendations

The LM5008A converter is designed to operate from a wide input voltage range from 6 V to 95 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Estimate the average input current with Equation 13.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \quad (13)$$

where

- $\eta$ is the efficiency

If the converter is connected to an input supply through long wires or PCB traces with large impedance, special care is required to achieve stable performance. The parasitic inductance and resistance of the input cables may have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the regulator is operating close to the minimum input voltage, this dip can cause false UVLO fault triggering and a system reset. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10 µF to 47 µF is usually sufficient to provide input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The user's guide *Simple Success Wth Conducted EMI for DC-DC Converters* (SNVA489) provides helpful suggestions when designing an input filter for any switching regulator.

# 10 Layout

## 10.1 Layout Guidelines

The LM5008A regulation and overvoltage comparators are very fast, and as such responds to short-duration noise pulses. Layout considerations are therefore critical for optimum performance:

1. Minimize the area of the high di/dt switching current loop consisting of the VIN pin, input ceramic capacitor, SW node and freewheeling power diode. Keep the input capacitor as close as possible to the VIN pin and route a short, direct connection to the RTN pin using polygon copper pours.
2. Minimize SW copper area to reduce radiated noise related to high dv/dt.
3. Locate all components as physically close as possible to their respective pins, thereby minimizing noise pickup in the printed-circuit tracks.
4. The FB trace should be away from noise sources and inductors. The lower feedback resistor should connect to ground close to the IC RTN.

If the internal dissipation of the LM5008A converter produces excessive junction temperatures during normal operation, optimal use of the PCB ground plane can help considerably to dissipate heat. The exposed pad on the bottom of the WSON-8 package can be soldered to a ground plane on the PCB, and that plane should extend out from beneath the IC to help dissipate the heat. Additionally, the use of wide PCB traces for power connection can also help conduct heat away from the IC. Judicious positioning of the LM5008A converter within the end product, along with use of any available air flow (forced or natural convection), can help reduce the operating junction temperature.

## 10.2 Layout Example

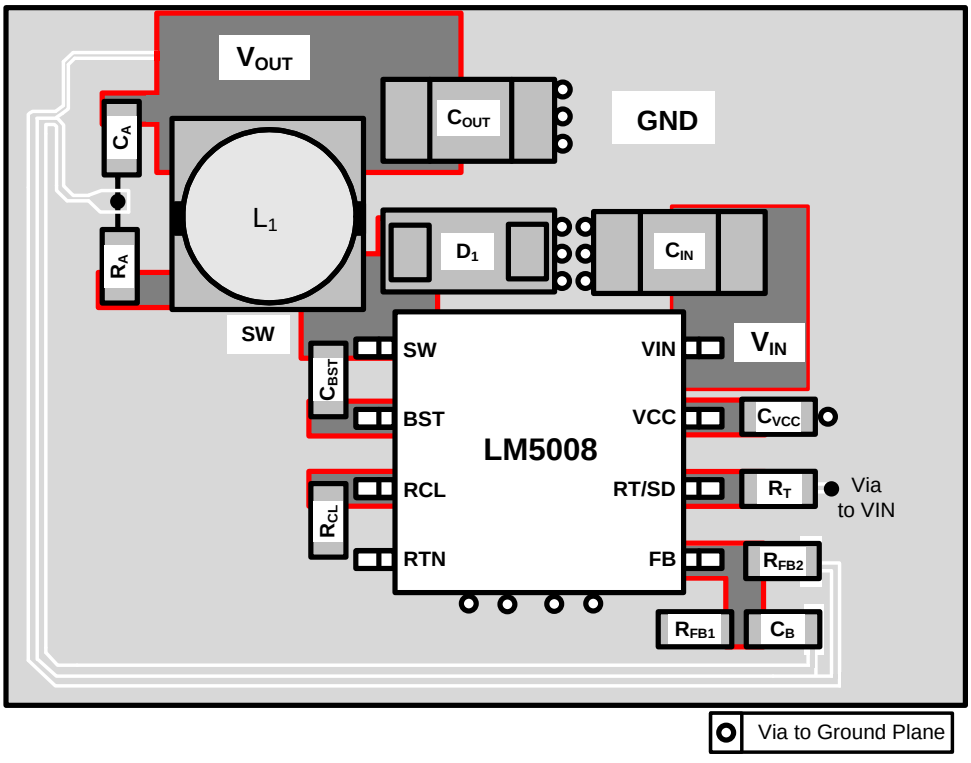



**Figure 16. LM5008A PCB Layout Example**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 11.1.2 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5008A device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

### 11.1.3 Development Support

For development support see the following:

- For TI's reference design library, visit TI Designs
- For TI's WEBENCH Design Environments, visit WEBENCH® Design Center
- For selecting components in LM5008A applications, see the LM5008A Quick-Start Calculator

## 11.2 Documentation Support

### 11.2.1 Related Documentation

For related documentation see the following:

- *LM5008 Quick-start Calculator*
- *AN-1925 LM5008A Evaluation Board* (SNVA380)
- *AN-1330 LM5008 Evaluation Board* (SNVA090)
- *Buck Regulator Topologies for Wide Input/Output Voltage Differentials* (SNVA594)
- White Papers:
  - *Valuing Wide $V_{IN}$, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*
  - *An Overview of Conducted EMI Specifications for Power Supplies*
  - *An Overview of Radiated EMI Specifications for Power Supplies*

#### *11.2.1.1 PCB Layout Resources*

- *AN-1149 Layout Guidelines for Switching Power Supplies* (SNVA021)
- *AN-1229 Simple Switcher PCB Layout Guidelines* (SNVA054)
- *Constructing Your Power Supply – Layout Considerations* (SLUP230)
- *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x* (SNVA721)
- *AN-2162 Simple Success With Conducted EMI From DC-DC Converters* (SNVA489)
- *Reduce Buck-Converter EMI and Voltage Stress by Minimizing Inductive Parasitics* (SLYT682)

## Documentation Support (continued)

- Power House Blogs:
  - *High-Density PCB Layout of DC/DC Converters*

#### 11.2.1.2 Thermal Design Resources

- *AN-2020 Thermal Design By Insight, Not Hindsight* (SNVA419)
- *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* (SNVA183)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *Thermal Design Made Simple with LM43603 and LM43602* (SNVA719)
- *PowerPAD™Thermally Enhanced Package* (SLMA002)
- *PowerPAD Made Easy* (SLMA004)
- *Using New Thermal Metrics* (SBVA025)

### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

### 11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM5008AMM/NOPB | ACTIVE | VSSOP | DGK | 8 | 1000 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | SAYA | Samples |
| LM5008AMMX/NOPB | ACTIVE | VSSOP | DGK | 8 | 3500 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | SAYA | Samples |
| LM5008ASD/NOPB | ACTIVE | WSON | NGU | 8 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | L00070A | Samples |
| LM5008ASDX/NOPB | ACTIVE | WSON | NGU | 8 | 4500 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | L00070A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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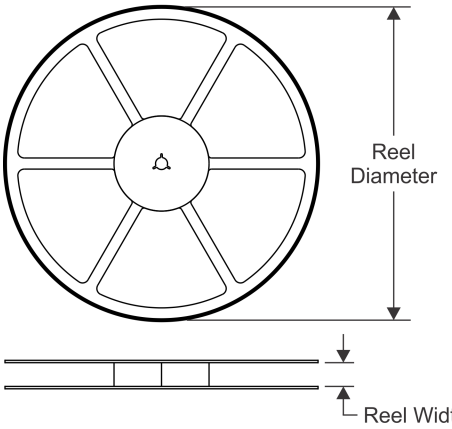
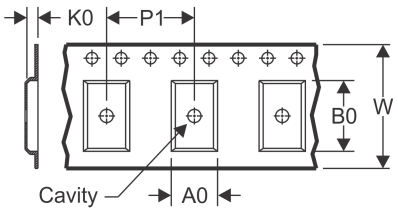
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

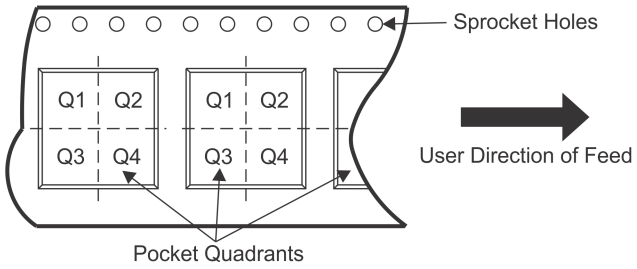



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

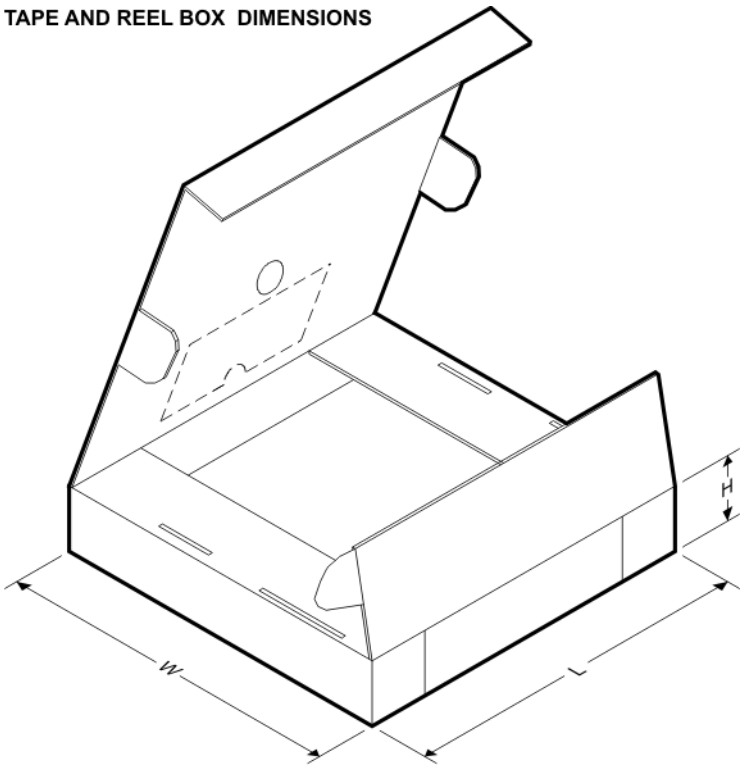
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM5008AMM/NOPB | VSSOP | DGK | 8 | 1000 | 178.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LM5008AMMX/NOPB | VSSOP | DGK | 8 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LM5008ASD/NOPB | WSON | NGU | 8 | 1000 | 180.0 | 12.4 | 4.3 | 4.3 | 1.1 | 8.0 | 12.0 | Q1 |
| LM5008ASDX/NOPB | WSON | NGU | 8 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |

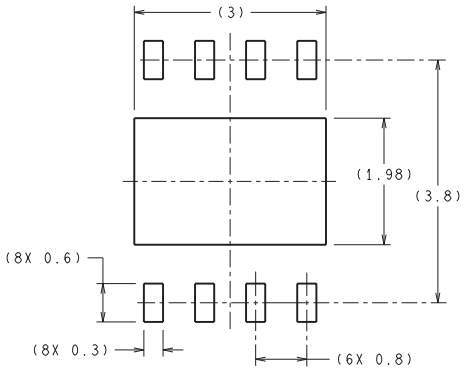
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

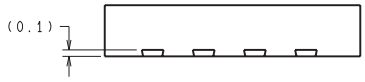
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM5008AMM/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |
| LM5008AMMX/NOPB | VSSOP | DGK | 8 | 3500 | 367.0 | 367.0 | 35.0 |
| LM5008ASD/NOPB | WSON | NGU | 8 | 1000 | 203.0 | 203.0 | 35.0 |
| LM5008ASDX/NOPB | WSON | NGU | 8 | 4500 | 367.0 | 367.0 | 35.0 |

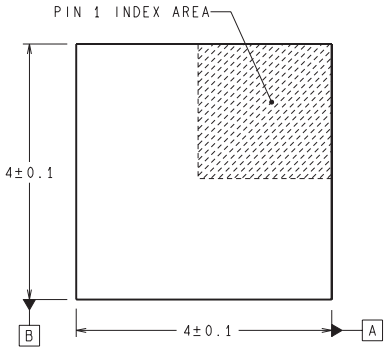
# NGU0008B

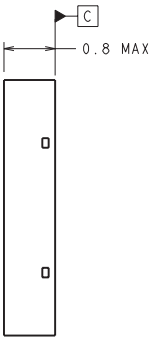


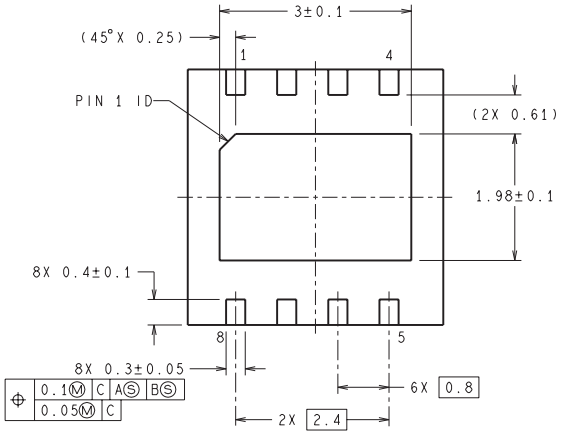

RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



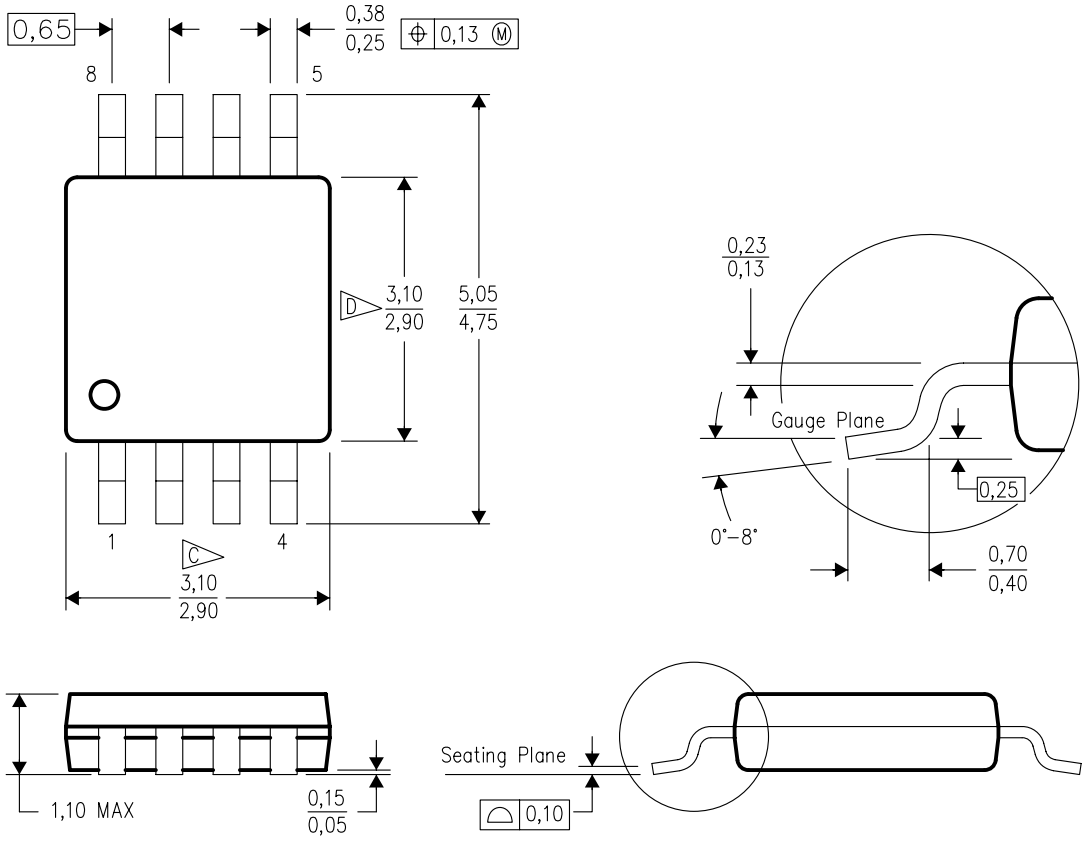




SDC08B (Rev A)

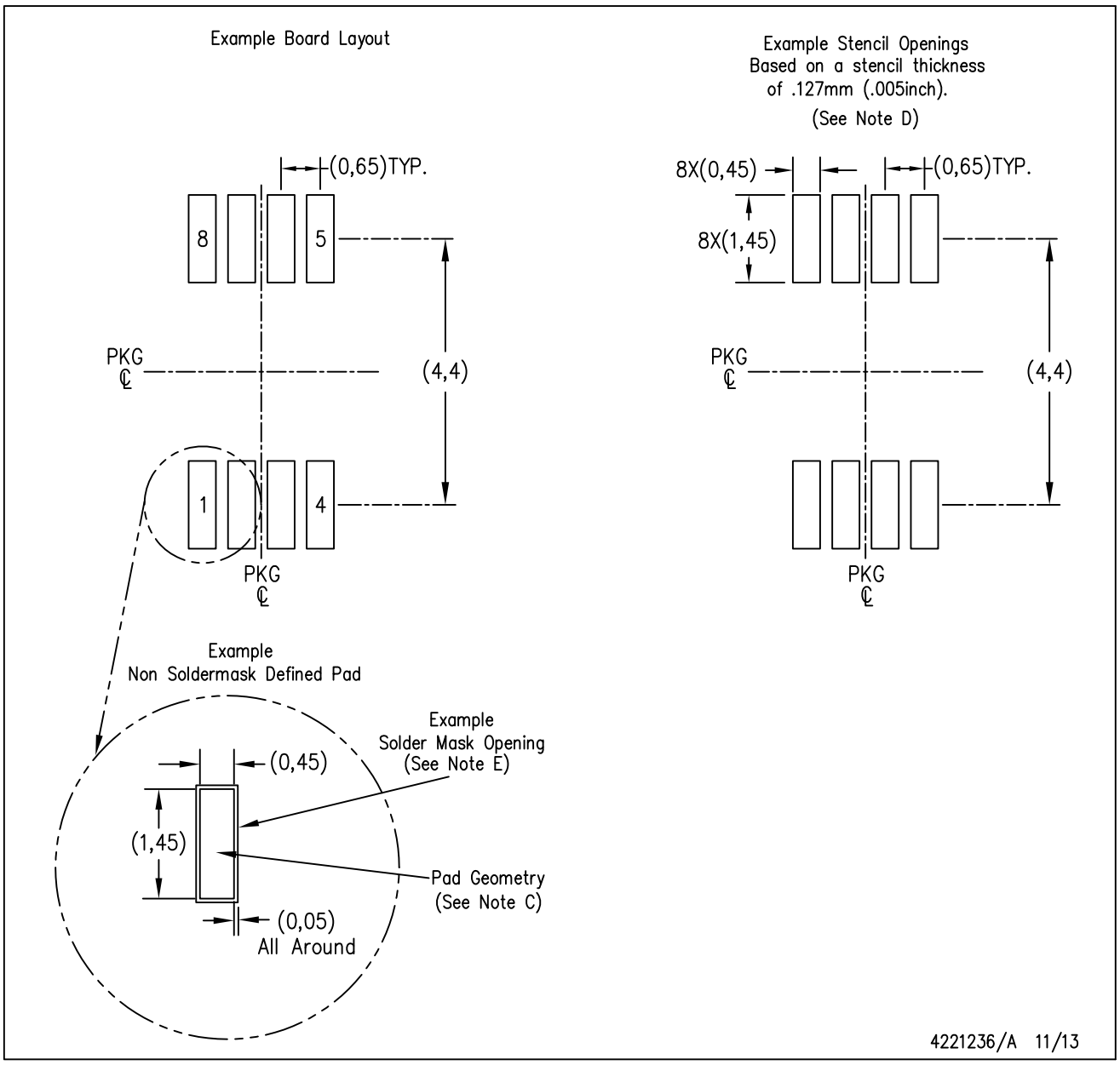
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

# DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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