

# TC74HCT138AP,TC74HCT138AF,TC74HCT138AFN

## 3-to-8 Line Decoder

The TC74HCT138A is a high speed CMOS 3-to-8 LINE DECODER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs ( $\bar{Y}_0$  -  $\bar{Y}_7$ ) will go low.

When enable input G1 is held low or either  $\bar{G}_{2A}$  or  $\bar{G}_{2B}$  is held high, decoding function is inhibited and all outputs go high.

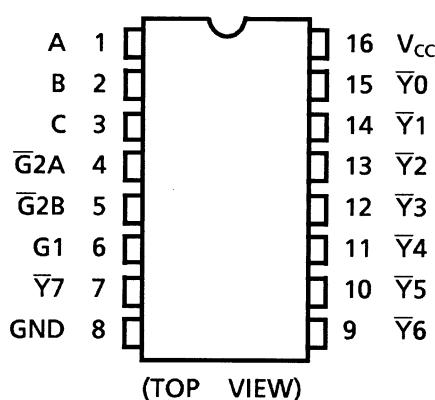
$\bar{G}_1$ ,  $\bar{G}_{2A}$ , and  $\bar{G}_{2B}$  inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

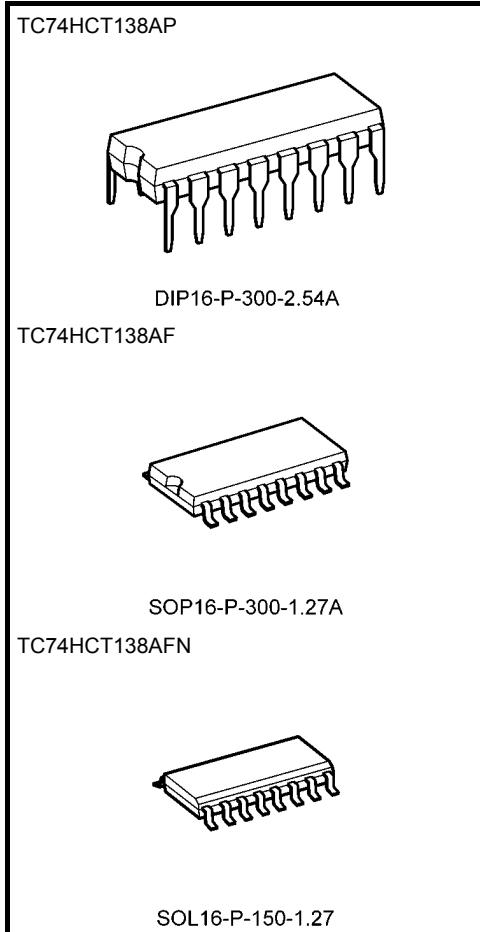
## Features

- High speed:  $t_{pd} = 17$  ns (typ.) at  $V_{CC} = 5$  V
- Low power dissipation:  $I_{CC} = 4$   $\mu$ A (max) at  $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs:  $V_{IH} = 2$  V (min)  
 $V_{IL} = 0.8$  V (max)
- Wide interfacing ability: LSTTL, NMOS, CMOS
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 4$  mA (min)
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with 74LS138

## Pin Assignment



Note: xxxFN (JEDEC SOP) is not available in Japan.



### Weight

DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)

## IEC Logic Symbol

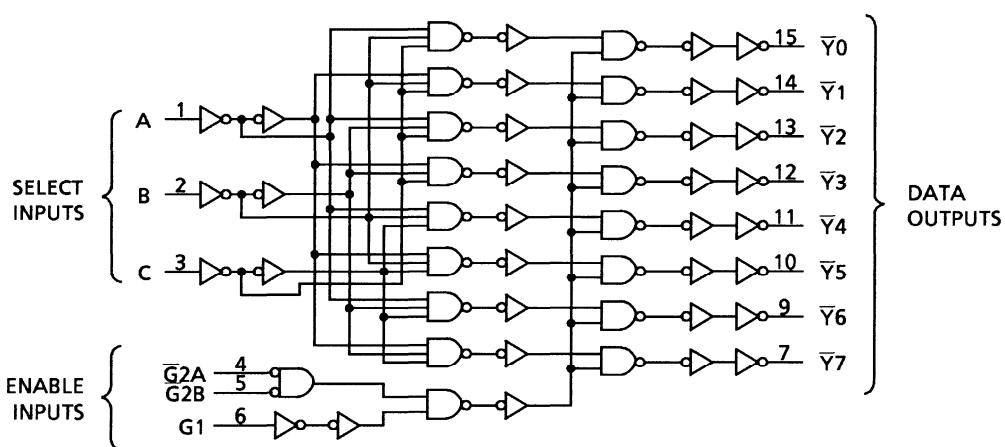


## Truth Table

Inputs						Outputs								Selected Output
Enable			Select			$\bar{Y}_0$	$\bar{Y}_1$	$\bar{Y}_2$	$\bar{Y}_3$	$\bar{Y}_4$	$\bar{Y}_5$	$\bar{Y}_6$	$\bar{Y}_7$	
G1	$\bar{G}_{2A}$	$\bar{G}_{2B}$	C	B	A									
L	X	X	X	X	X	H	H	H	H	H	H	H	H	None
X	H	X	X	X	X	H	H	H	H	H	H	H	H	None
X	X	H	X	X	X	H	H	H	H	H	H	H	H	None
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\bar{Y}_0$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\bar{Y}_1$
H	L	L	L	H	L	H	H	H	L	H	H	H	H	$\bar{Y}_2$
H	L	L	L	H	H	H	H	H	H	L	H	H	H	$\bar{Y}_3$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\bar{Y}_4$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\bar{Y}_5$
H	L	L	H	H	H	H	H	H	H	H	H	H	H	$\bar{Y}_6$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\bar{Y}_7$

X: Don't care

## Logic Diagram



**Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	-0.5~7.0	V
DC input voltage	V <sub>IN</sub>	-0.5~V <sub>CC</sub> + 0.5	V
DC output voltage	V <sub>OUT</sub>	-0.5~V <sub>CC</sub> + 0.5	V
Input diode current	I <sub>IK</sub>	±20	mA
Output diode current	I <sub>OK</sub>	±20	mA
DC output current	I <sub>OUT</sub>	±25	mA
DC V <sub>CC</sub> /ground current	I <sub>CC</sub>	±50	mA
Power dissipation	P <sub>D</sub>	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T <sub>stg</sub>	-65~150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of Ta = -40 to 65°C. From Ta = 65 to 85°C a derating factor of -10 mW/°C shall be applied until 300 mW.

**Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	4.5~5.5	V
Input voltage	V <sub>IN</sub>	0~V <sub>CC</sub>	V
Output voltage	V <sub>OUT</sub>	0~V <sub>CC</sub>	V
Operating temperature	T <sub>opr</sub>	-40~85	°C
Input rise and fall time	t <sub>r</sub> , t <sub>f</sub>	0~500	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either V<sub>CC</sub> or GND.

**Electrical Characteristics****DC Characteristics**

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40~85°C		Unit
		V <sub>CC</sub> (V)	Min	Typ.	Max	Min	Max		
High-level input voltage	V <sub>IH</sub>	—	4.5~5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V <sub>IL</sub>	—	4.5~5.5	—	—	0.8	—	0.8	V
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	4.5	4.4	4.5	—	4.4	V
			I <sub>OH</sub> = -4 mA	4.5	4.18	4.31	—	4.13	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	4.5	—	0.0	0.1	—	V
			I <sub>OL</sub> = 4 mA	4.5	—	0.17	0.26	—	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	4.0	—	40.0	μA
	I <sub>C</sub>	Per input: V <sub>IN</sub> = 0.5 V or 2.4 V Other input: V <sub>CC</sub> or GND	5.5	—	—	2.0	—	2.9	mA

AC Characteristics ( $C_L = 15 \text{ pF}$ ,  $V_{CC} = 5 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ , input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}$ $t_{THL}$	—	—	4	8	ns
Propagation delay time (A, B, C- $\bar{Y}$ )	$t_{pLH}$ $t_{pHL}$	—	—	17	28	ns
Propagation delay time (G1- $\bar{Y}$ )	$t_{pLH}$ $t_{pHL}$	—	—	15	25	ns
Propagation delay time ( $\bar{G}2$ - $\bar{Y}$ )	$t_{pLH}$ $t_{pHL}$	—	—	17	28	ns

AC Characteristics ( $C_L = 50 \text{ pF}$ , input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		Unit
			4.5	Min	Typ.	Max	Min	Max	
Output transition time	$t_{TLH}$ $t_{THL}$	—	4.5	—	8	15	—	19	ns
			5.5	—	7	14	—	18	
Propagation delay time (A, B, C- $\bar{Y}$ )	$t_{pLH}$ $t_{pHL}$	—	4.5	—	21	33	—	44	ns
			5.5	—	18	30	—	40	
Propagation delay time (G1- $\bar{Y}$ )	$t_{pLH}$ $t_{pHL}$	—	4.5	—	19	30	—	38	ns
			5.5	—	17	27	—	34	
Propagation delay time ( $\bar{G}2$ - $\bar{Y}$ )	$t_{pLH}$ $t_{pHL}$	—	4.5	—	22	33	—	41	ns
			5.5	—	20	30	—	37	
Input capacitance	$C_{IN}$	—	—	5	10	—	10	pF	
Power dissipation capacitance	$C_{PD}$ (Note)	—	—	55	—	—	—	pF	

Note:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

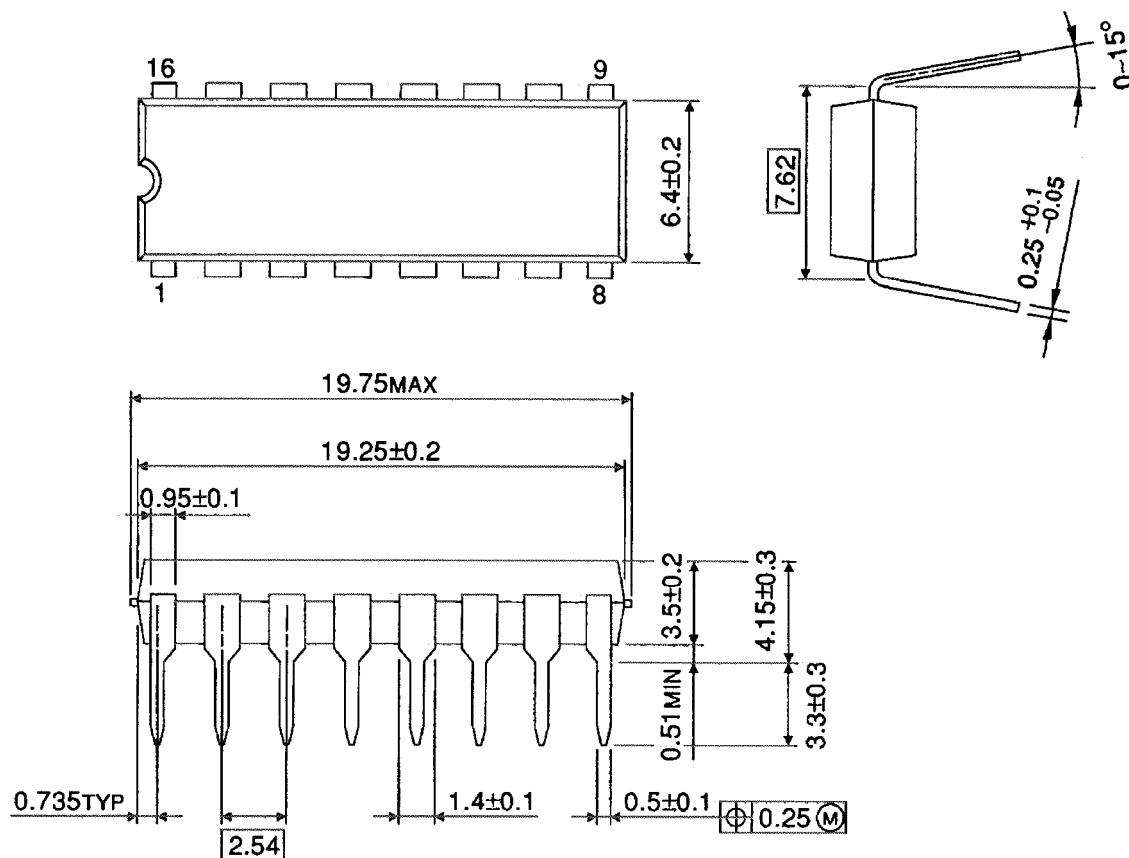
Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

**Package Dimensions**

DIP16-P-300-2.54A

Unit : mm

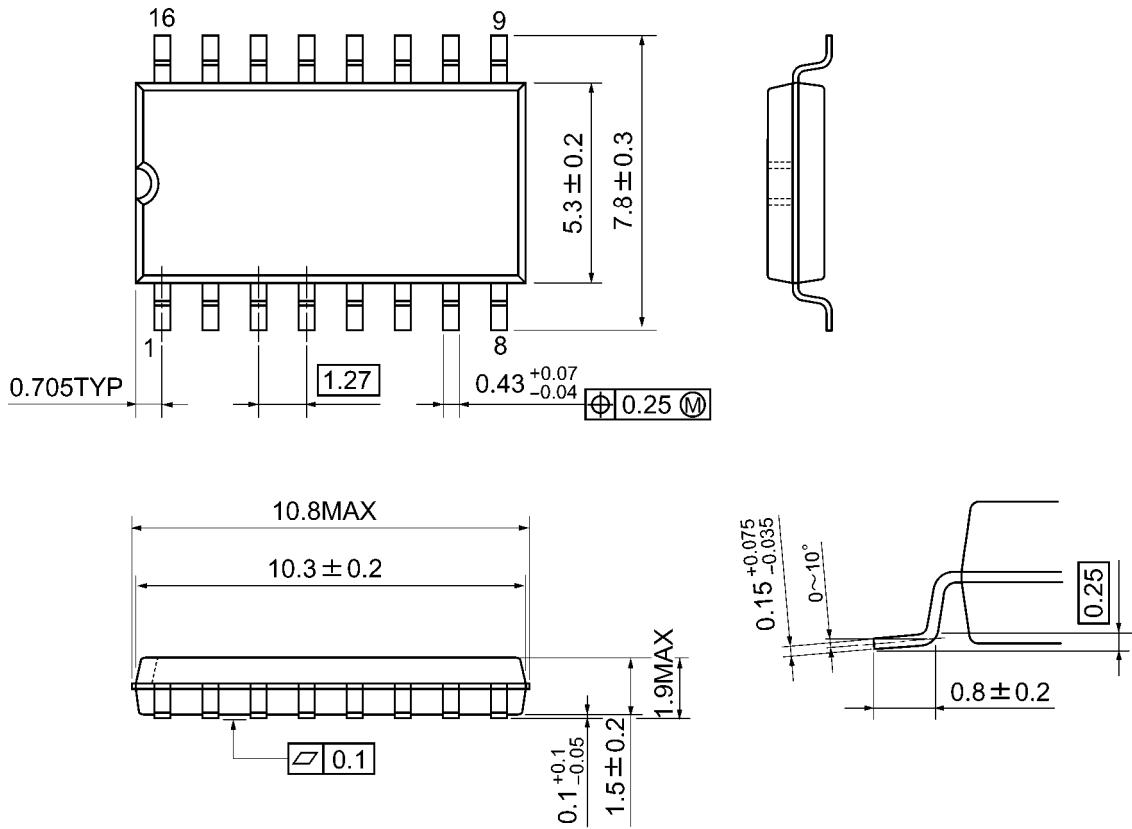


Weight: 1.00 g (typ.)

**Package Dimensions**

SOP16-P-300-1.27A

Unit: mm

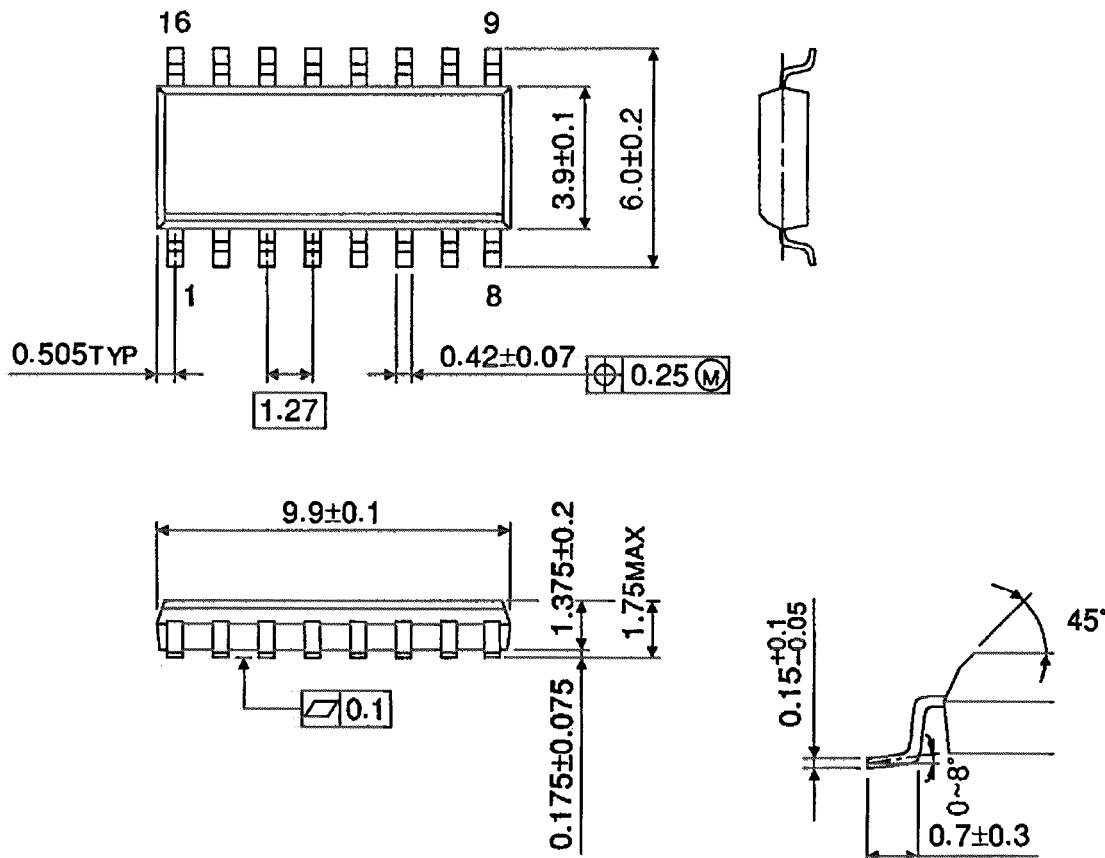


Weight: 0.18 g (typ.)

**Package Dimensions (Note)**

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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