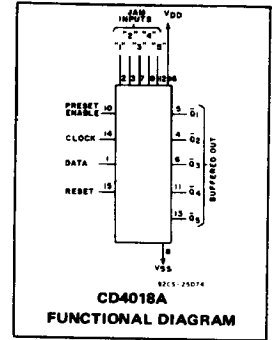


CMOS Presettable Divide-By-'N' Counter

The RCA-CD4018A types consist of 5 Johnson-Counter stages, buffered $\bar{Q}$ outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\bar{Q}_5, \bar{Q}_4, \bar{Q}_3, \bar{Q}_2, \bar{Q}_1$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a CD4011A gate package to properly gate the feedback connection to the DATA input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018A

units. The counter is advanced one count at the positive clock-signal transition. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



Features:

- Medium speed operation . . . 5 MHz (typ.) at $V_{DD} - V_{SS} = 10\text{ V}$
- Fully static operation
- Quiescent current specified to 15 μA
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters
- Fixed and programmable counters greater than 10
- Programmable decade counters
- Divide-by-'N' counters/frequency synthesizers
- Frequency division
- Counter control/timers

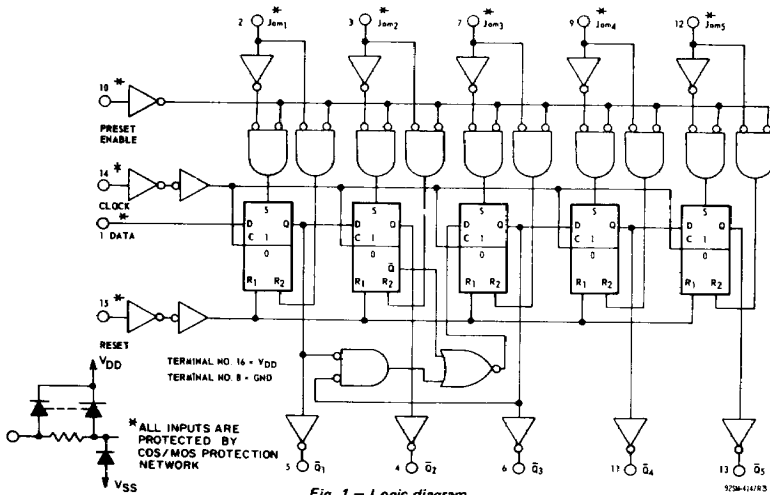


Fig. 1 - Logic diagram.

("DATA" INPUT TIED TO $\bar{Q}_5$ FOR DECADE COUNTER CONFIGURATION)

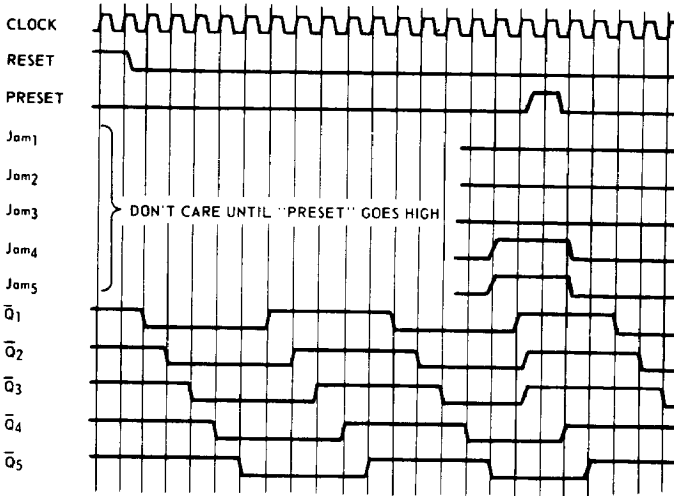


Fig. 2 - Timing diagram.

92SS-4148R2

EXTERNAL CONNECTIONS FOR DIVIDE BY 10, 9, 8, 7, 6, 5, 4, 3 OPERATION

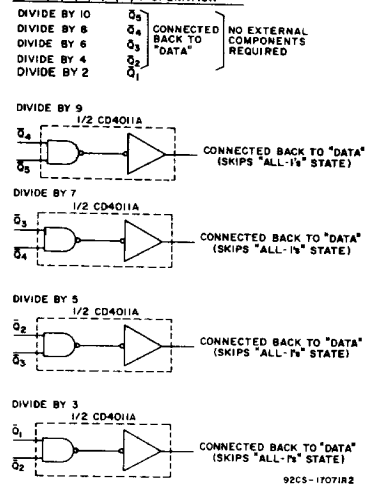


Fig. 3 - External connections for divide by 10, 9, 8, 7, 6, 5, 4, 3, 2 operation.

CD4018A Types

MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T_{stg}) -65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
 PACKAGE TYPES D, F, K, H -55 to +125°C
 PACKAGE TYPE E -40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
 (Voltages referenced to V_{SS} Terminal): -0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
 FOR T_A = -40 to +60°C (PACKAGE TYPE E)500 mW
 FOR T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW
 FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K)500 mW
 FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
 FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} + 0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
 At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_f, t_r = 20\text{ ns}$,
 $C_L = 15\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS							UNITS	
		VDD (V)	D, F, K, H Packages			E Package				
			Min.	Typ.	Max.	Min.	Typ.	Max.		
CLOCKED OPERATION										
Propagation Delay Time; tPLH, tPHL To Q5 Output		5	—	350	1000	—	350	1300	ns	
		10	—	125	250	—	125	300		
	To Other Outputs	5	—	500	1200	—	500	1600		
		10	—	200	400	—	200	500		
Transition Time; tTHL, tTLH To Q5 Output		5	—	100	300	—	100	350	ns	
		10	—	50	150	—	50	200		
	To Other Outputs	5	—	300	900	—	300	1200	ns	
		10	—	125	350	—	125	450		
Maximum Clock Input Frequency, fCL		5	1	2.5	—	0.6	2.5	—	MHz	
		10	3	5	—	2	5	—		
Min. Clock Pulse Width, tW		5	—	200	500	—	200	830	ns	
		10	—	100	170	—	100	250		
Clock Rise & Fall Time; tCL, tCL		5	—	—	15	—	—	15	μs	
		10	—	—	15	—	—	15		
Min. Data Input Set-Up Time, tS		5	—	175	500	—	175	700	ns	
		10	—	75	200	—	75	300		
Average Input Capacitance, Ci	Any Input	—	5	—	—	—	5	—	pF	
PRESET* OR RESET OPERATION										
Propagation Delay Time: tPLH, tPHL To Q5 Output		5	—	350	1000	—	350	1300	ns	
		10	—	125	250	—	125	300		
	To Other Outputs	5	—	500	1200	—	500	1600		
		10	—	200	400	—	200	500		
Min. Preset or Reset Pulse Width tW		5	—	200	500	—	200	830	ns	
		10	—	100	165	—	100	250		
Min. Preset or Reset Removal Time		5	—	300	750	—	300	1000		
		10	—	100	225	—	100	275		

* At PRESET ENABLE OR JAM Inputs.

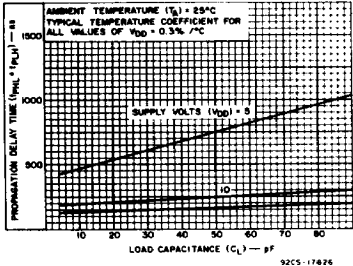


Fig. 4 — Typical propagation delay time vs. load capacitance for decoded outputs.

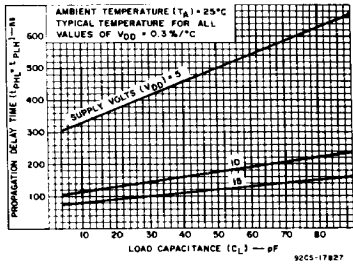


Fig. 5 — Typical propagation delay time vs. load capacitance for $\bar{Q}_5$ output.

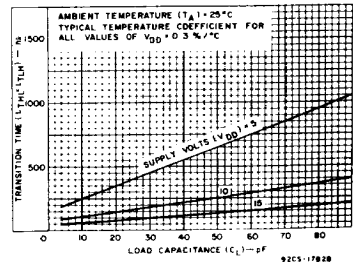


Fig. 6 — Typical transition time vs. load capacitance for decoded outputs.

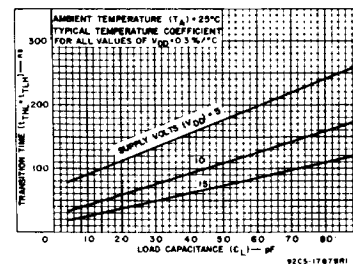


Fig. 7 — Typical transition time vs. load capacitance for $\bar{Q}_5$ output.

CD4018A Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$. Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	VDD (V)	LIMITS				UNITS
		D, F, K, H Packages		E Package		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T _A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t _S	5 10	500 200	— —	700 300	— —	ns
Clock Pulse Width, t _W	5 10	500 170	— —	830 250	— —	ns
Clock Input Frequency, f _{CL}	5 10	dc dc	1 3	dc dc	0.6 2	MHz
Clock Rise and Fall Time, t _{rCL} , t _{fCL}	5 10	— —	15 15	— —	15 15	μs
Preset or Reset Pulse Width, t _W	5 10	500 165	— —	830 250	— —	ns
Preset or Reset Removal Time	5 10	750 225	— —	1000 275	— —	ns

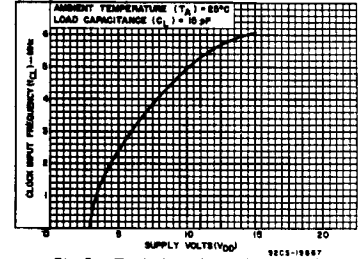


Fig. 8 - Typical maximum input clock frequency vs. supply voltage.

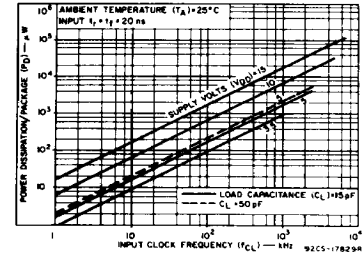


Fig. 9 - Typical dissipation characteristics

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Unit	
				D, F, K, H Packages				E Package					
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	+25		+125	-40	+25		+85		
Quiescent Device Current I _L Max.	—	—	5	5	0.3	5	300	50	0.5	50	700	μA	
	—	—	10	10	0.5	10	600	100	1	100	1400		
	—	—	15	50	1	50	2000	500	5	500	5000		
Output Voltage: Low Level, V _{OL} High Level V _{OH}	—	5	5	0 Typ.; 0.05 Max.									V
	—	10	10	0 Typ.; 0.05 Max.									
	—	0	5	4.95 Min.; 5 Typ.									
	—	0	10	9.95 Min.; 10 Typ.									
Noise Immunity: Inputs Low, V _{NL} Inputs High V _{NH}	4.2	—	5	1.5 Min.; 2.25 Typ.									V
	9	—	10	3 Min.; 4.5 Typ.									
	0.8	—	5	1.5 Min.; 2.25 Typ.									
	1	—	10	3 Min.; 4.5 Typ.									
Noise Margin: Inputs Low, V _{NML} Inputs High, V _{NMH}	4.5	—	5	1 Min.									V
	9	—	10	1 Min.									
	0.5	—	5	1 Min.									
	1	—	10	1 Min.									
Output Drive Current: n-Channel (Sink) I _{DN} Min. p-Channel (Source) I _{DP} Min.	$\bar{Q}_5$	0.5	—	5	0.18	0.4	0.15	0.105	0.095	0.4	0.08	0.065	mA
		0.5	—	10	0.45	1	0.35	0.25	0.3	1	0.25	0.2	
	$\bar{Q}_1, \bar{Q}_2$	0.5	—	5	0.06	0.1	0.05	0.035	0.03	0.1	0.025	0.02	
		0.5	—	10	0.25	0.4	0.2	0.14	0.18	0.4	0.15	0.12	
	$\bar{Q}_3, \bar{Q}_4$	0.5	—	5	-0.185	-0.4	-0.15	-0.105	-0.095	-0.4	-0.08	-0.065	
		0.5	—	10	-0.45	-1	-0.35	-0.25	-0.3	-1	-0.25	-0.2	
	$\bar{Q}_5$	4.5	—	5	-0.075	-0.15	-0.06	-0.04	-0.035	-0.15	-0.03	-0.024	
		9.5	—	10	-0.25	-0.4	-0.2	-0.14	-0.18	-0.4	-0.15	-0.12	
	$\bar{Q}_1, \bar{Q}_2$	4.5	—	5	-0.075	-0.15	-0.06	-0.04	-0.035	-0.15	-0.03	-0.024	
		9.5	—	10	-0.25	-0.4	-0.2	-0.14	-0.18	-0.4	-0.15	-0.12	
	$\bar{Q}_3, \bar{Q}_4$	4.5	—	5	-0.075	-0.15	-0.06	-0.04	-0.035	-0.15	-0.03	-0.024	
		9.5	—	10	-0.25	-0.4	-0.2	-0.14	-0.18	-0.4	-0.15	-0.12	
Input Leakage Current, I _{IL} , I _{IH} Max.	Any Input — — 15			±10 ⁻⁵ Typ., ±1 Max.									μA

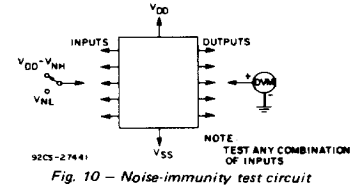


Fig. 10 - Noise-immunity test circuit

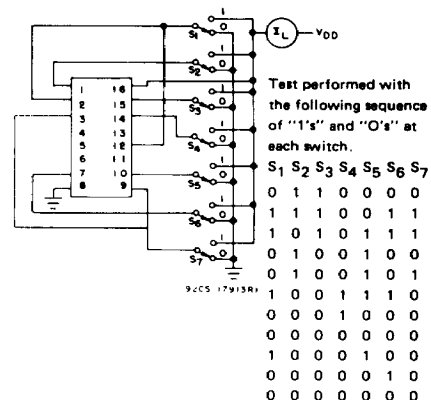


Fig. 11 - Quiescent-device-current test circuit.

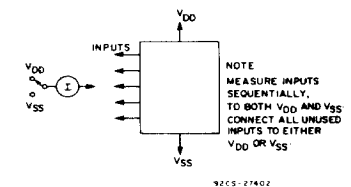


Fig. 12 - Input-leakage-current test circuit.