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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HD74HC273

Octal D-type Flip-Flops (with Clear)



ADE-205-482 (Z)
1st. Edition
Sep. 2000

Description

This device contains 8 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the clock input. The clear input when low, sets all outputs to a low state.

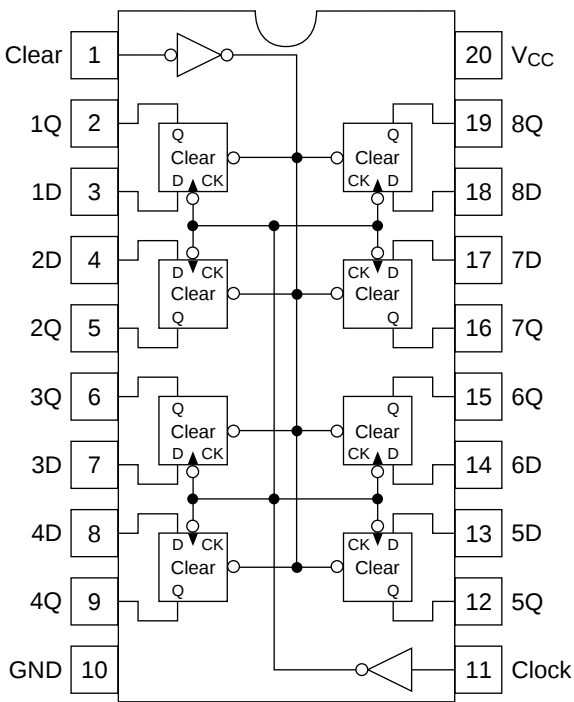
Features

- High Speed Operation: t_{pd} (Clock to Q) = 18 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

Function Table

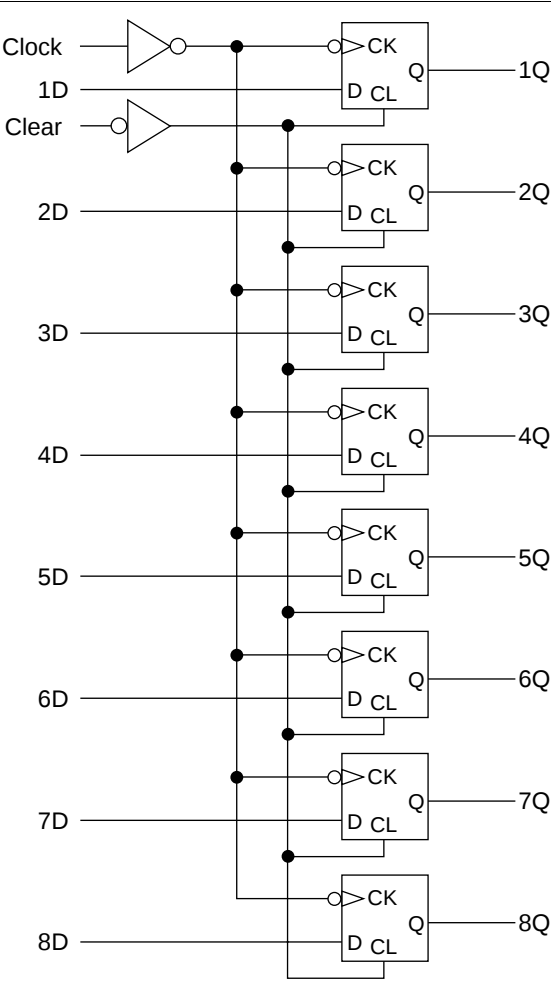
Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H		H	H
H		L	L
H	L	X	No change
H		X	No change

Pin Arrangement



(Top view)

Logic Diagram



DC Characteristics

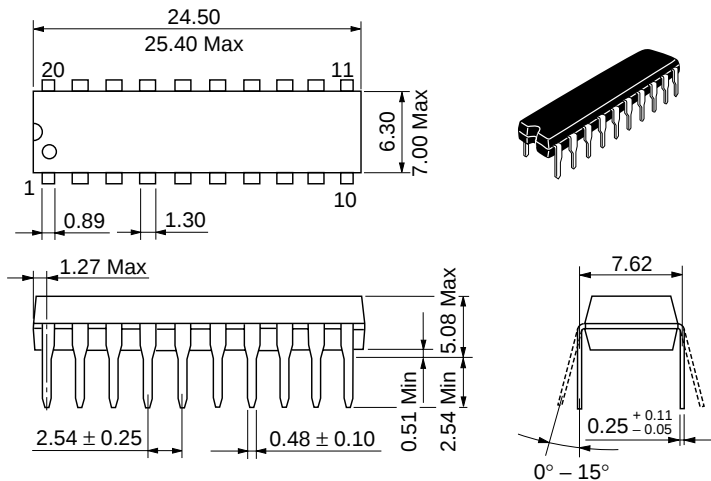
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I _{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I _{OL} = 5.2 mA
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	$f_{\max}$	2.0	—	—	6	—	5	MHz	
		4.5	—	—	30	—	24		
		6.0	—	—	35	—	28		
Propagation delay time	t_{PHL}	2.0	—	—	145	—	180	ns	Clock to Q
		4.5	—	18	29	—	36		
		6.0	—	—	25	—	31		
	t_{PLH}	2.0	—	—	145	—	180	ns	
		4.5	—	18	29	—	36		
		6.0	—	—	25	—	31		
	t_{PHL}	2.0	—	—	145	—	180	ns	Clear to Q
		4.5	—	15	29	—	36		
		6.0	—	—	25	—	31		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	Data to clock
		4.5	20	2	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	Clock to data
		4.5	5	0	—	5	—		
		6.0	5	—	—	5	—		
Removal time	t_{rem}	2.0	100	—	—	125	—	ns	Clear to clock
		4.5	20	-1	—	25	—		
		6.0	17	—	—	21	—		
Pulse width	t_w	2.0	80	—	—	100	—	ns	Clock, clear
		4.5	16	8	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	
	t_{THL}	4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

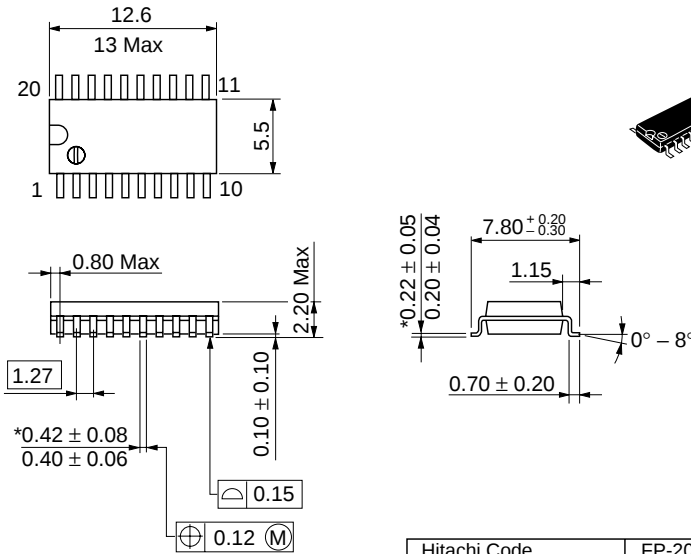
Package Dimensions

Unit: mm



Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Mass (reference value)	1.26 g

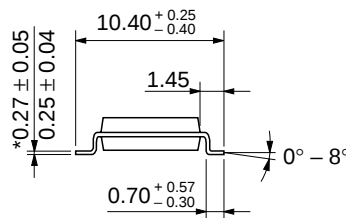
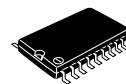
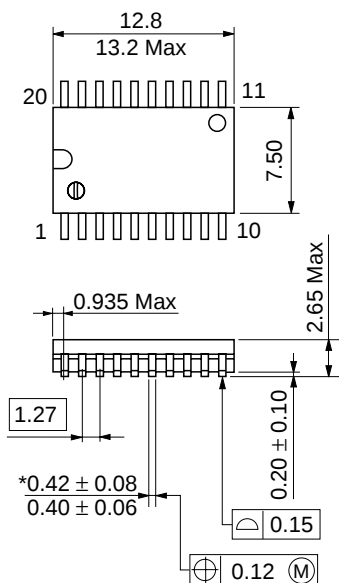
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.31 g

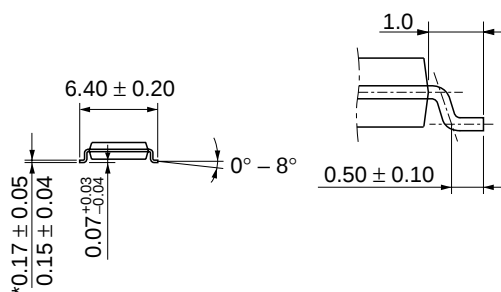
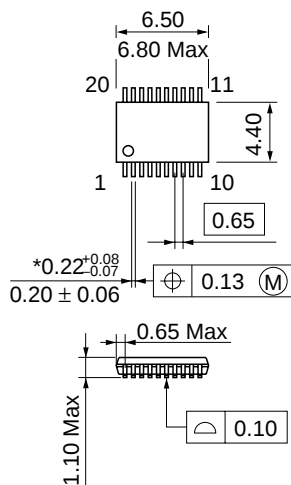
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.52 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Mass (reference value)	0.07 g

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	:	http://semiconductor.hitachi.com/
	Europe	:	http://www.hitachi-eu.com/hel/ecg
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For further information write to:

Hitachi Semiconductor
(America) Inc.

179 East Tasman Drive,
San Jose, CA 95134

Tel: <1> (408) 433-1990

Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic Components Group

Dornacher Straße 3
D-85622 Feldkirchen, Munich

Germany

Tel: <49> (89) 9 9180-0

Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.

Whitebrook Park

Lower Cookham Road

Maidenhead

Berkshire SL6 8YA, United Kingdom

Tel: <44> (1628) 585000

Fax: <44> (1628) 585160

Hitachi Asia Ltd.

Hitachi Tower

16 Collyer Quay #20-00,

Singapore 049318

Tel: <65>-538-6533/538-8577

Fax: <65>-538-6933/538-3877

URL: <http://www.hitachi.com.sg>

Hitachi Asia Ltd.

(Taipei Branch Office)

4/F, No. 167, Tun Hwa North Road,

Hung-Kuo Building,

Taipei (105), Taiwan

Tel: <886>-(2)-2718-3666

Fax: <886>-(2)-2718-8180

Telex: 23222 HAS-TP

URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.

Group III (Electronic Components)

7/F., North Tower,

World Finance Centre,

Harbour City, Canton Road

Tsim Sha Tsui, Kowloon,

Hong Kong

Tel: <852>-(2)-735-9218

Fax: <852>-(2)-730-0281

URL: <http://www.hitachi.com.hk>

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