

TC74LVX00FN

Quad 2-Input NAND Gate

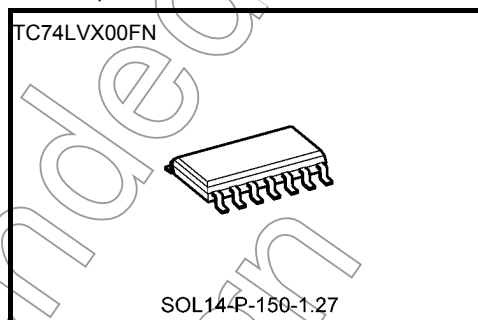
The TC74LVX00FN is a high-speed CMOS 2-input NAND gate fabricated with silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low-voltage and battery operated systems.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Note: xxxFN (JEDEC SOP) is not available in Japan.

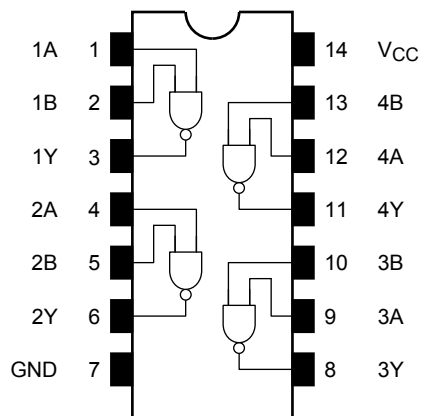


Weight
SOL14-P-150-1.27 : 0.12 g (typ.)

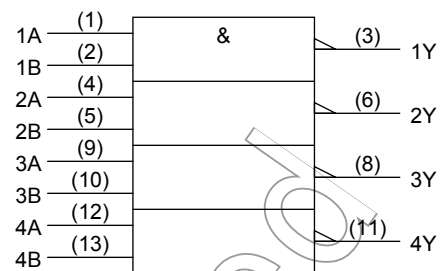
Features

- High-speed: $t_{pd} = 4.1 \text{ ns (typ.)}$ ($V_{CC} = 3.3 \text{ V}$)
- Low power dissipation: $I_{CC} = 2 \mu\text{A (max)}$ ($T_a = 25^\circ\text{C}$)
- Input voltage level: $V_{IL} = 0.8 \text{ V (max)}$ ($V_{CC} = 3 \text{ V}$)
 $V_{IH} = 2.0 \text{ V (min)}$ ($V_{CC} = 3 \text{ V}$)
- Power-down protection provided on all inputs
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Low noise: $V_{OLP} = 0.5 \text{ V (max)}$
- Pin and function compatible with 74HC00

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Input		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 3.6	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics		Symbol	Test Condition		Ta = 25°C				Ta = -40 to 85°C		Unit
					VCC (V)	Min	Typ.	Max	Min	Max	
Input voltage	H-level	VIH	—	2.0	1.5	—	—	1.5	—	V	
				3.0	2.0	—	—	2.0	—		
				3.6	2.4	—	—	2.4	—		
	L-level	VIL		2.0	—	—	0.5	—	0.5		
				3.0	—	—	0.8	—	0.8		
				3.6	—	—	0.8	—	0.8		
Output voltage	H-level	VOH	VIN = VIH or VIL	IOH = -50 μA	2.0	1.9	2.0	—	1.9	—	V
				IOH = -50 μA	3.0	2.9	3.0	—	2.9	—	
				IOH = -4 mA	3.0	2.58	—	—	2.48	—	
	L-level	VOL	VIN = VIH	IOL = 50 μA	2.0	—	0	0.1	—	0.1	
				IOL = 50 μA	3.0	—	0	0.1	—	0.1	
				IOL = 4 mA	3.0	—	—	0.36	—	0.44	
Input leakage current		IIN	VIN = 5.5 V or GND	3.6	—	—	±0.1	—	±1.0	μA	
Quiescent supply current		ICC	VIN = VCC or GND	3.6	—	—	2.0	—	20.0	μA	

AC Characteristics (input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
			VCC (V)	CL (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time	t _{pLH}	—	2.7	15	—	5.4	10.1	1.0	12.5	ns
				50	—	7.9	13.6	1.0	16.0	
	t _{pHL}		3.3 ± 0.3	15	—	4.1	6.2	1.0	7.5	
				50	—	6.6	9.7	1.0	11.0	
Output to output skew	t _{osLH}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
	t _{osHL}		3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input capacitance	C _{IN}	(Note 2)			—	4	10	—	10	pF
Power dissipation capacitance	C _{PD}	(Note 3)			—	19	—	—	—	pF

Note 1: Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Note 2: Parameter guaranteed by design.

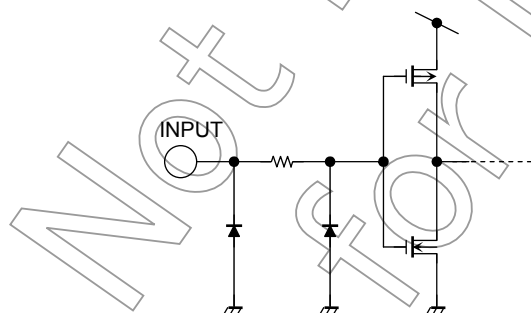
Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$$

Noise Characteristics (Ta = 25°C, input: $t_r = t_f = 3\text{ ns}$, C_L = 50 pF)

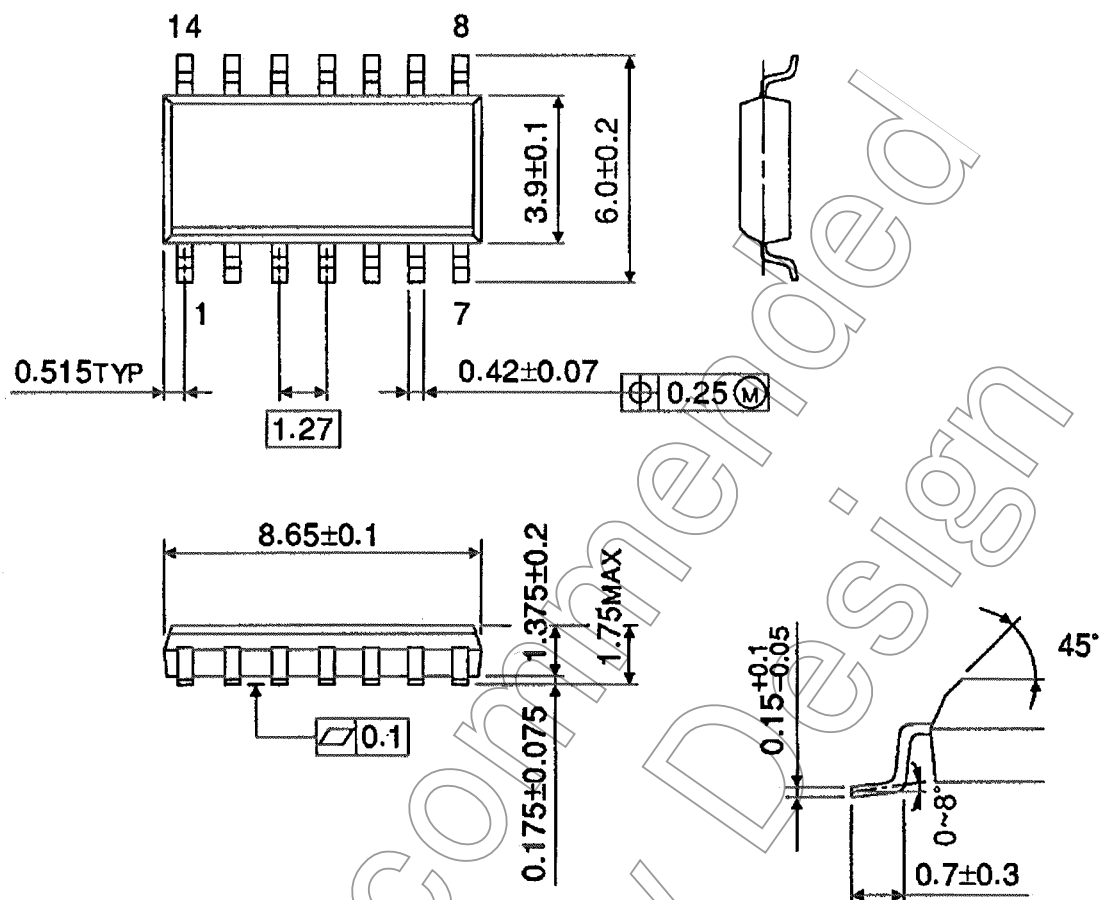
Characteristics	Symbol	Test Condition		Typ.	Limit	Unit
			V _{CC} (V)			
Quiet output maximum dynamic V _{OL}	V _{OLP}	—	3.3	0.3	0.5	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	—	3.3	−0.3	−0.5	V
Minimum high level dynamic input voltage V _{IH}	V _{IHD}	—	3.3	—	2.0	V
Maximum low level dynamic input voltage V _{IL}	V _{ILD}	—	3.3	—	0.8	V

Input Equivalent Circuit

Package Dimensions (Note)

SOL14-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.12 g (typ.)

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