

30A, 60V, 0.065 Ohm, P-Channel Power MOSFETs

These are P-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They are designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA09834.

Ordering Information

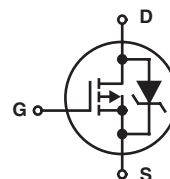
PART NUMBER	PACKAGE	BRAND
RFG30P06	TO-247	RFG30P06
RFP30P06	TO-220AB	RFP30P06
RF1S30P06SM	TO-263AB	F1S30P06

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, i.e. RF1S30P06SM9A.

Features

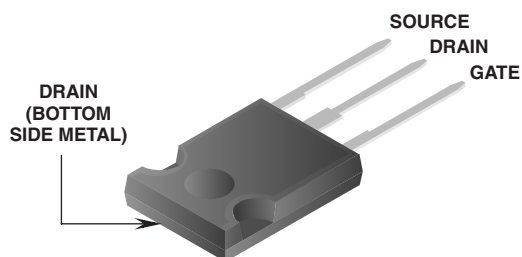
- 30A, 60V
- $r_{DS(ON)} = 0.065\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

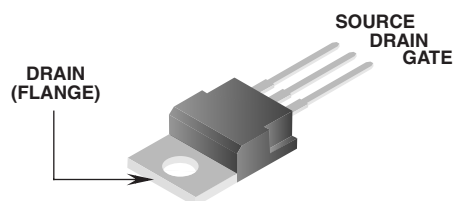


Packaging

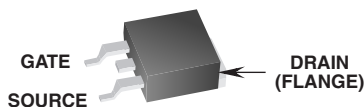
JEDEC STYLE TO-247



JEDEC TO-220AB



JEDEC TO-263AB



RFG30P06, RFP30P06, RF1S30P06SM

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

	RFG30P06, RFP30P06 RF1S30P06SM	UNITS
Drain to Source Voltage (Note 1)	V_{DSS} -60	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR} -60	V
Gate to Source Voltage	V_{GS} ± 20	V
Continuous Drain Current	I_D 30	A
Pulsed Drain Current (Note 3) (Figure 5)	I_{DM} Refer to Peak Current Curve	
Single Pulse Avalanche Rating (Figure 6)	E_{AS} Refer to UIS Curve	
Power Dissipation	P_D 135	W
Linear Derating Factor	0.9	W/ $^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG} -55 to 175	$^{\circ}\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L 300	$^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg} 260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	-2	-	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60\text{V}$, $V_{GS} = 0\text{V}$	-	-	-1	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$, $T_C = 150^{\circ}\text{C}$	-	-	-25	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = -30\text{A}$, $V_{GS} = -10\text{V}$ (Figure 9)	-	-	0.065	Ω
Turn-On Time	$t_{(ON)}$	$V_{DD} = -30\text{V}$, $I_D = 15\text{A}$, $R_L = 2.00\Omega$, $V_{GS} = -10\text{V}$ $R_G = 6.25\Omega$ (Figure 13)	-	-	80	ns
Turn-On Delay Time	$t_{d(ON)}$		-	15	-	ns
Rise Time	t_r		-	23	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	28	-	ns
Fall Time	t_f		-	18	-	ns
Turn-Off Time	$t_{(OFF)}$		-	-	100	ns
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0$ to -20V	-	140	170	nC
Gate Charge at -10V	$Q_{g(-10)}$	$V_{GS} = 0$ to -10V	-	70	85	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0$ to -2V	-	5.5	6.6	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 12)	-	3200	-	pF
Output Capacitance	C_{OSS}		-	800	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	175	-	pF
Thermal Resistance, Junction to Case	$R_{\theta JC}$		-	-	1.11	$^{\circ}\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	TO-220, TO-263	-	-	62	$^{\circ}\text{C/W}$
		TO-247			30	$^{\circ}\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	MAX
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = -30\text{A}$	-	-	-1.5	V
Diode Reverse Recovery Time	t_{RR}	$I_{SD} = -30\text{A}$, $dI_{SD}/dt = -100\text{A}/\mu\text{s}$	-	-	150	ns

NOTES:

2. Pulse test: pulse width $\leq 300\mu\text{s}$ maximum, duty cycle $\leq 2\%$.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).

Typical Performance Curves Unless Otherwise Specified

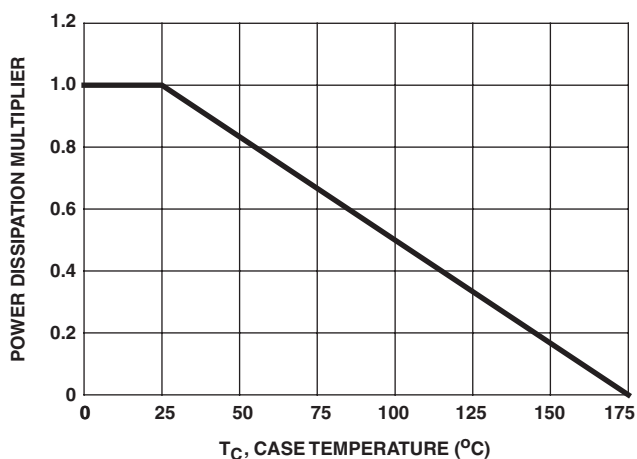


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

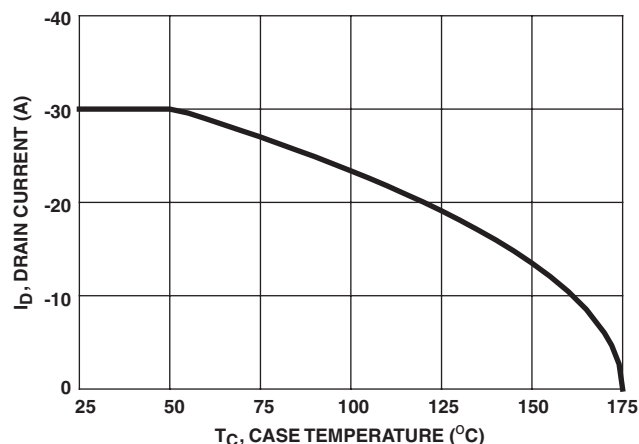


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

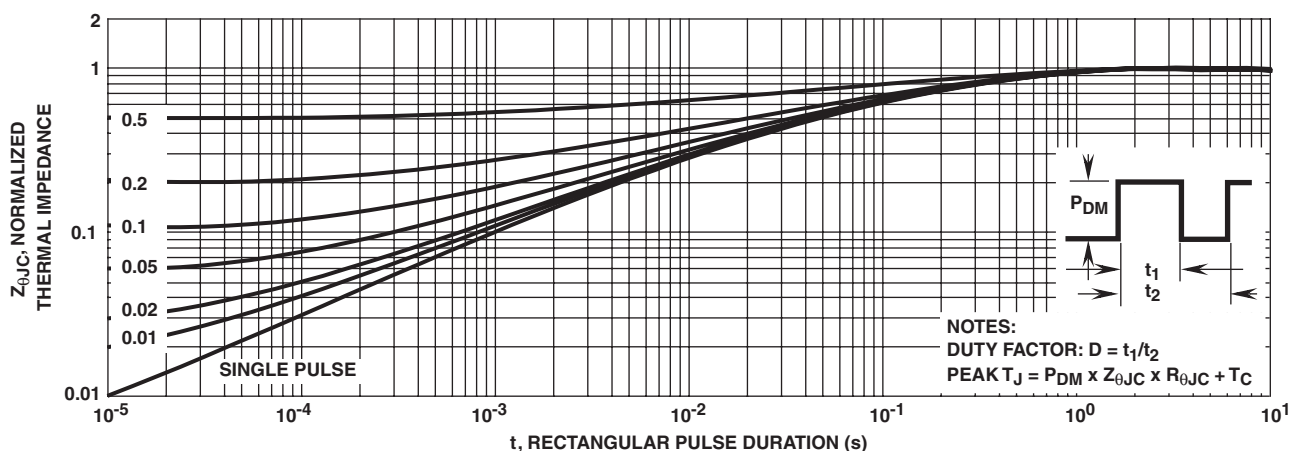


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

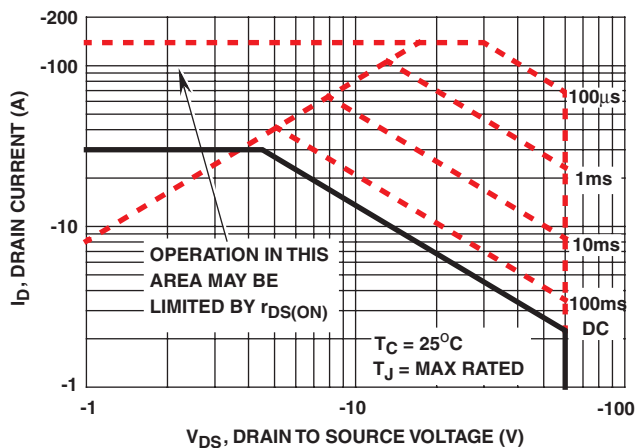


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

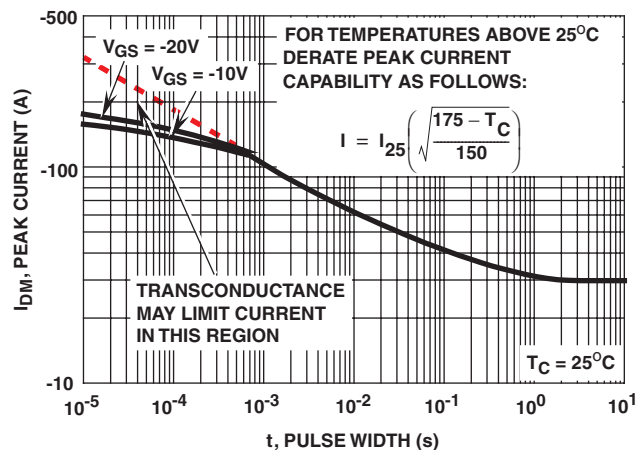
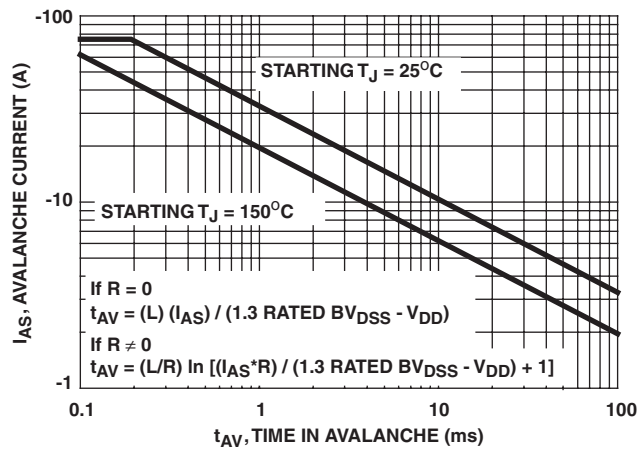


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)

NOTE: Refer to Fairchild Application Notes AN9321 and AN9322,
FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

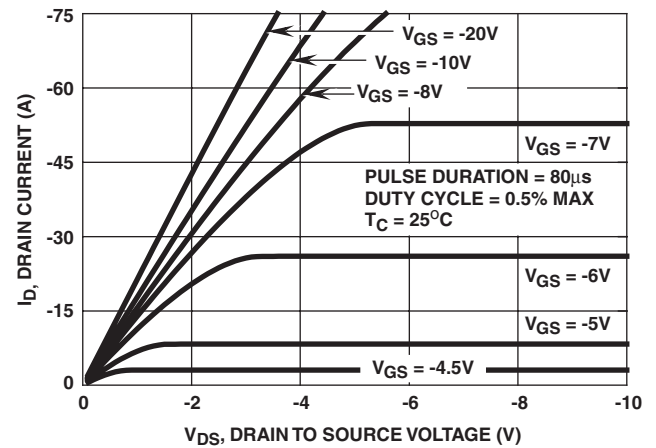


FIGURE 7. SATURATION CHARACTERISTICS

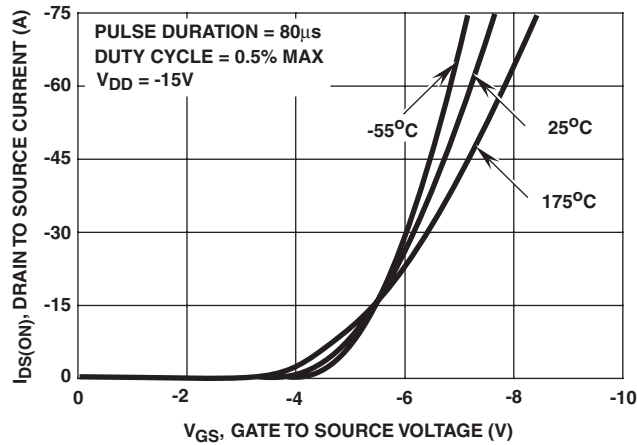


FIGURE 8. TRANSFER CHARACTERISTICS

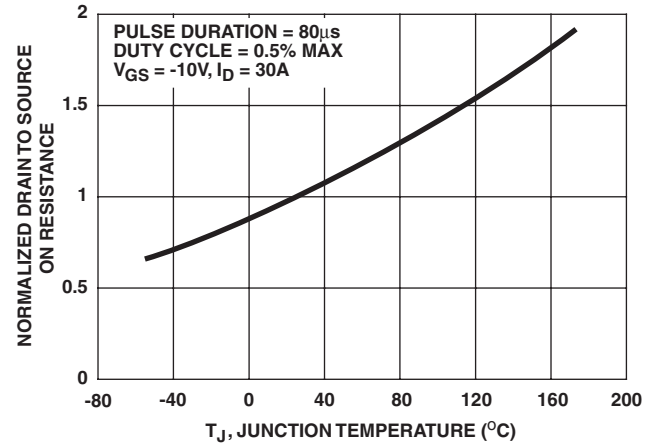


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

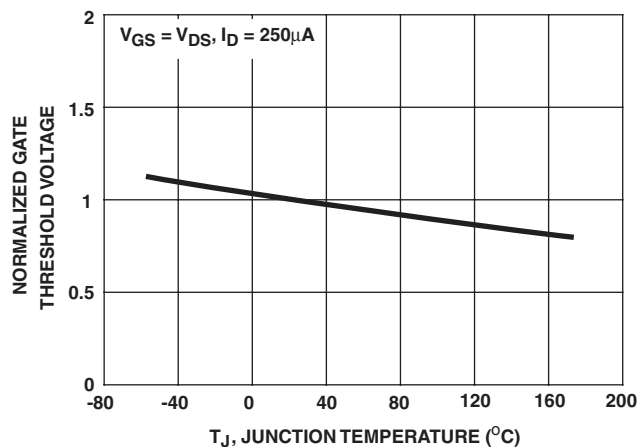


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

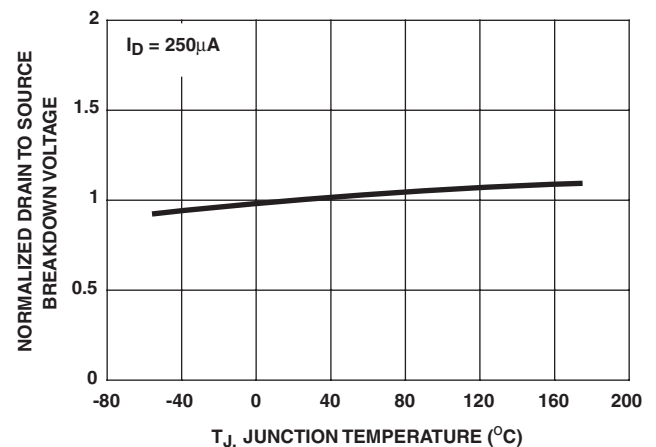


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

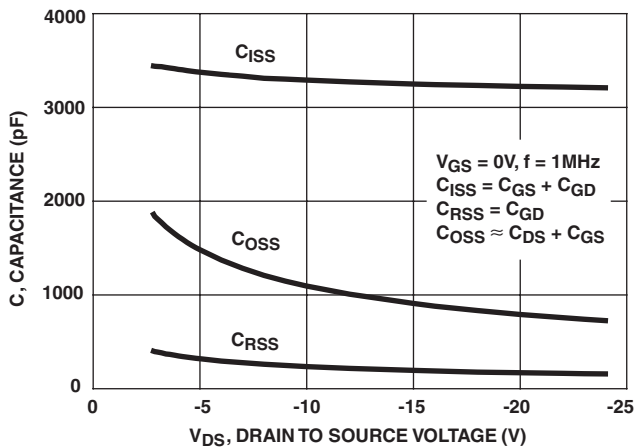
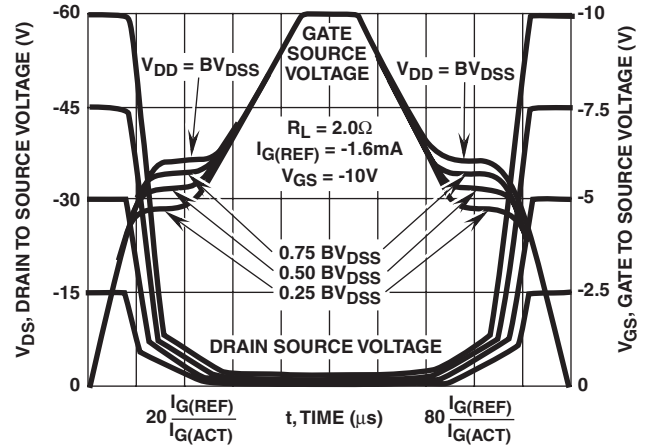


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

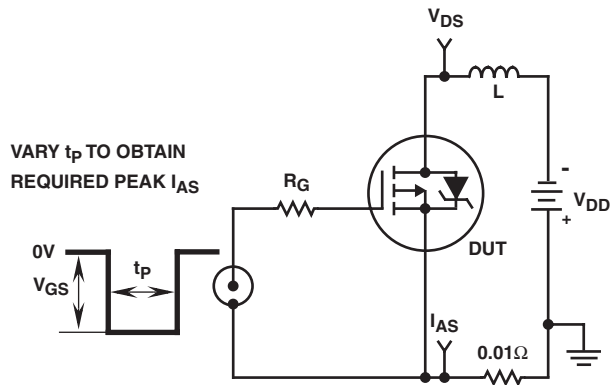


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

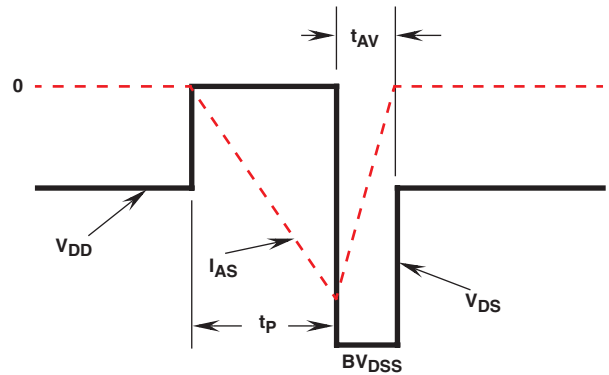


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

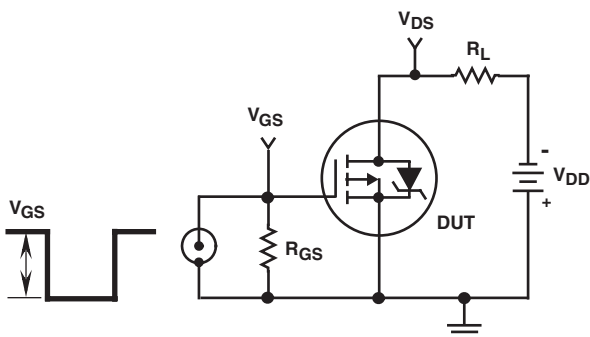


FIGURE 16. SWITCHING TIME TEST CIRCUIT

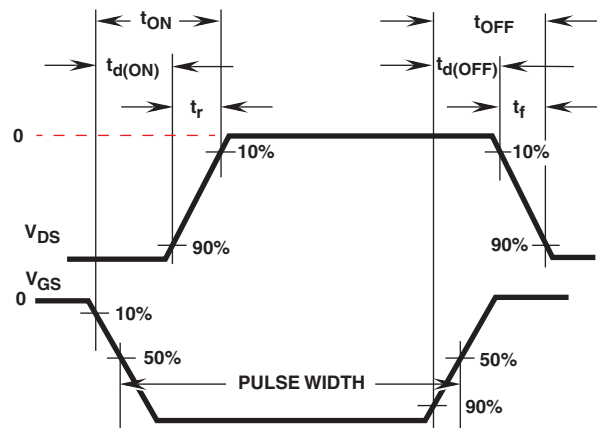


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

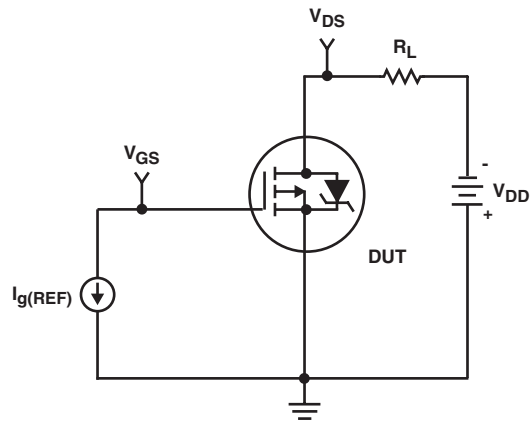


FIGURE 18. GATE CHARGE TEST CIRCUIT

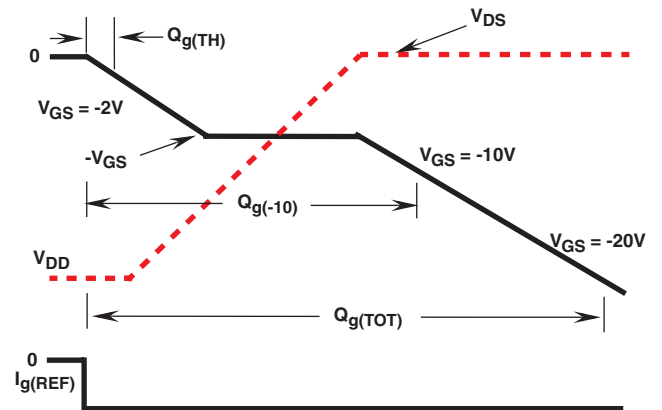


FIGURE 19. GATE CHARGE WAVEFORMS

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