

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4538B

MSI

Dual precision monostable multivibrator

Product specification
File under Integrated Circuits, IC04

January 1995

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DESCRIPTION

The HEF4538B is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has an active LOW trigger/retrigger input ($\bar{I}_0$), an active HIGH trigger/retrigger input (I_1), an overriding active LOW direct reset input ($\bar{C}_D$), an output (O) and its complement ($\bar{O}$), and two pins ($C_{TC}^{(1)}$, RC_{TC}) for connecting the external timing components C_t and R_t . Typical pulse width variation over temperature range is $\pm 0,2\%$.

The HEF4538B may be triggered by either the positive or the negative edges of the input pulse and will produce an

accurate output pulse with a pulse width range of 10 μ s to infinity. The duration and accuracy of the output pulse are determined by the external timing components C_t and R_t . The output pulse width (T) is equal to $R_t \times C_t$. The linear design techniques in LOC MOS guarantee precise control of the output pulse width.

A LOW level at $\bar{C}_D$ terminates the output pulse immediately. Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times.

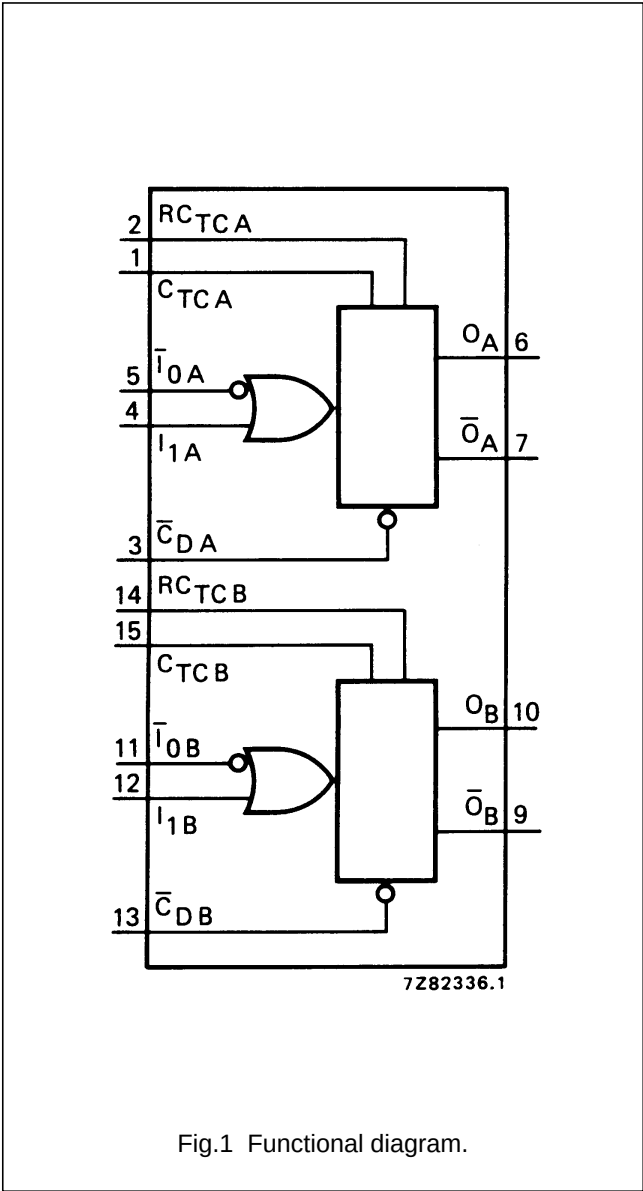
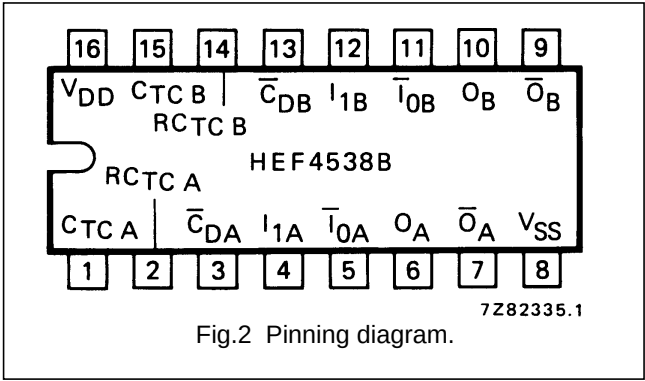


Fig.1 Functional diagram.



- HEF4538BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4538BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4538BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

$\bar{I}_{0A}, \bar{I}_{0B}$	input (HIGH to LOW triggered)
I_{1A}, I_{1B}	input (LOW to HIGH triggered)
$\bar{C}_{DA}, \bar{C}_{DB}$	direct reset input (active LOW)
O_A, O_B	output
$\bar{O}_A, \bar{O}_B$	complementary output (active LOW)
$C_{TC A}, C_{TC B}$	external capacitor connections ⁽¹⁾
$RC_{TC A}, RC_{TC B}$	external capacitor/ resistor connections

Note

1. Always connected to ground.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family specifications.

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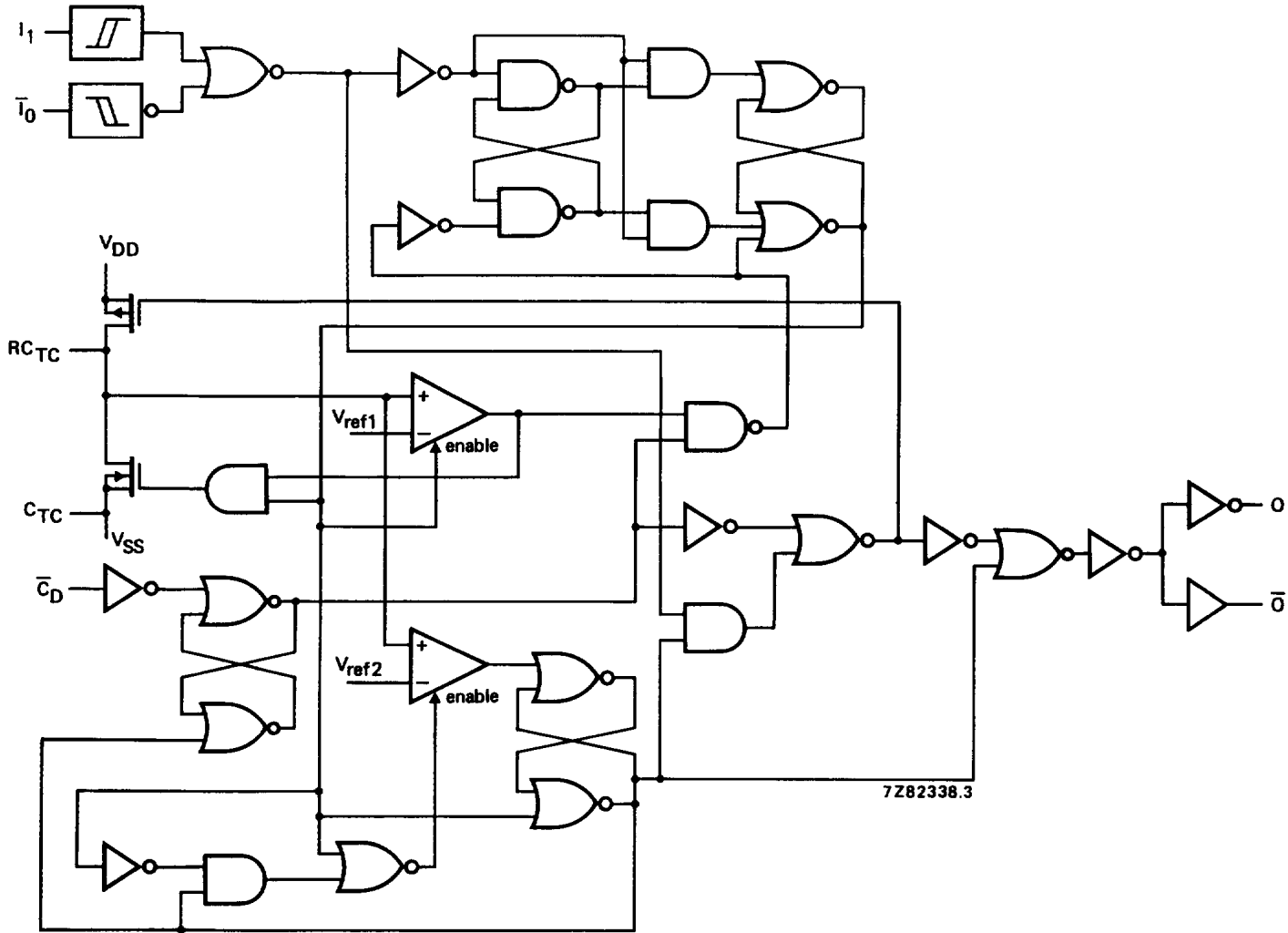


Fig.3 Logic diagram.

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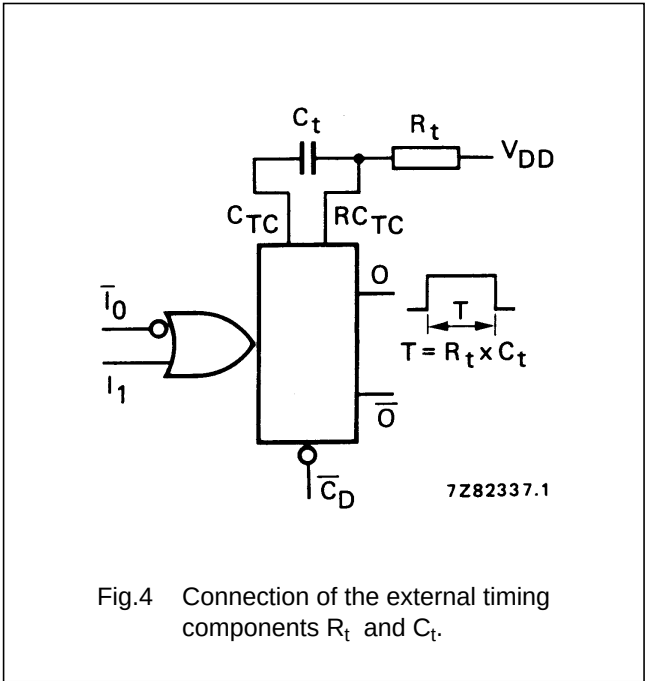
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FUNCTION TABLE

INPUTS			OUTPUTS	
$\bar{I}_0$	I_1	$\bar{C}_D$	O	$\bar{O}$
	L	H		
H		H		
X	X	L	L	H

Notes

1. H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
 = positive output pulse
 = negative output pulse
 = positive-going transition
 = negative-going transition



DC CHARACTERISTICS

$V_{SS} = 0\text{ V}$

	V _{DD} V	SYMBOL	T _{amb} (°C)					
			– 40		+ 25		+ 85	
			TYP.	MAX.	TYP.	MAX.	TYP.	MAX.
Supply current	5	I _D	55				μA	
active state	10		150				μA	
(see note)	15		220				μA	
Input leakage current (pins 2 and 14)	15	± I _{IN}	300				1000 nA	

Note

1. Only one monostable is switching: current present during output pulse (output O is HIGH).

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AC CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays $\bar{I}_0, I_1 \rightarrow O$ HIGH to LOW $\bar{I}_0, I_1 \rightarrow \bar{O}$ LOW to HIGH $\bar{C}_D \rightarrow O$ HIGH to LOW $\bar{C}_D \rightarrow \bar{O}$ LOW to HIGH	5			200	460 ns	173 ns + (0,55 ns/pF) C_L
	10	t_{PHL}		90	180 ns	79 ns + (0,23 ns/pF) C_L
	15			60	120 ns	52 ns + (0,16 ns/pF) C_L
	5			220	440 ns	193 ns + (0,55 ns/pF) C_L
	10	t_{PLH}		85	190 ns	74 ns + (0,23 ns/pF) C_L
	15			60	120 ns	52 ns + (0,16 ns/pF) C_L
	5			125	250 ns	98 ns + (0,55 ns/pF) C_L
	10	t_{PHL}		55	110 ns	44 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
	5			125	250 ns	98 ns + (0,55 ns/pF) C_L
	10	t_{PLH}		55	110 ns	44 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
Recovery times $\bar{C}_D \rightarrow \bar{I}_0, I_1$	5			20	40 ns	
	10	t_{RCD}		10	20 ns	
	15			5	10 ns	
Retrigger times $O, \bar{O} \rightarrow \bar{I}_0, I_1$	5		0		ns	
	10	t_{RO}	0		ns	
	15		0		ns	
Minimum $\bar{I}_0$ pulse width; LOW	5		90	45	ns	
	10	t_{WIOL}	30	15	ns	
	15		24	12	ns	
Minimum I_1 pulse width; HIGH	5		50	25	ns	
	10	t_{WI1H}	24	12	ns	
	15		20	10	ns	
Minimum $\bar{C}_D$ pulse width; LOW	5		55	25	ns	
	10	t_{WCDL}	25	12	ns	
	15		20	10	ns	
Output O or $\bar{O}$ pulse width	5		218	230	242 μ s	$R_t = 100$ k Ω $C_t = 0,002$ μ F
	10	t_{WO}	213	224	235 μ s	
	15		211	223	234 μ s	
Output O or $\bar{O}$ pulse width	5		10,3	10,8	11,3 ms	$R_t = 100$ k Ω $C_t = 0,1$ μ F
	10	t_{WO}	10,2	10,7	11,2 ms	
	15		10,1	10,6	11,1 ms	
Output O or $\bar{O}$ pulse width	5		1,01	1,09	1,11 s	$R_t = 100$ k Ω $C_t = 10$ μ F
	10	t_{WO}	0,99	1,04	1,09 s	
	15		0,99	1,04	1,09 s	

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AC CHARACTERISTICS

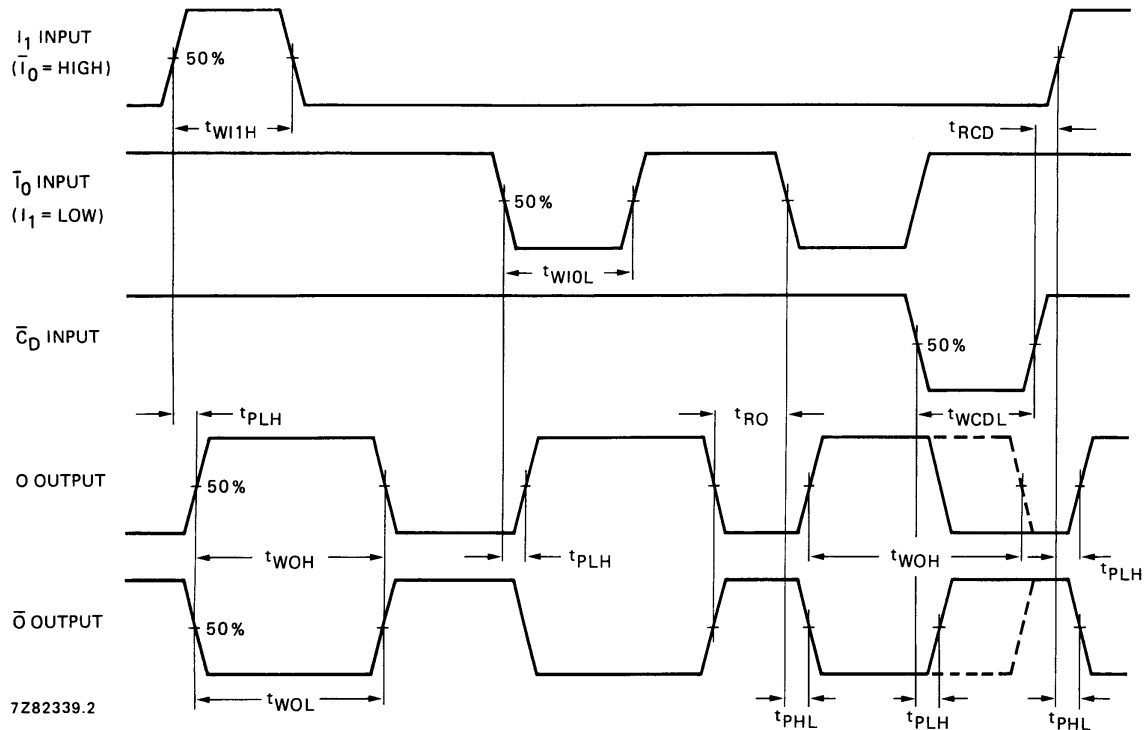
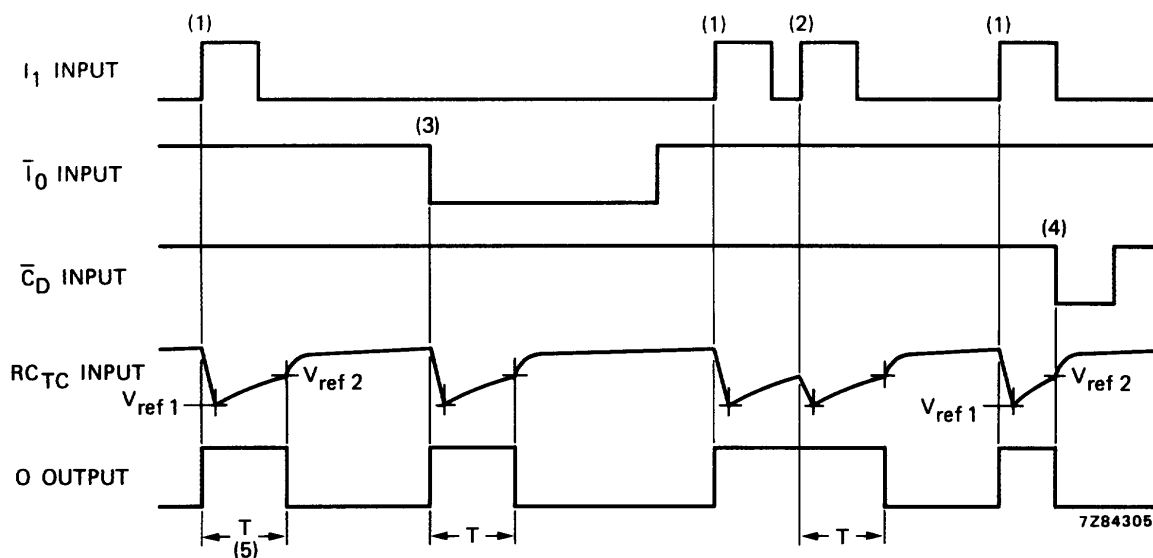
 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	
Change in output O pulse width over temperature (T_{amb})	5 10 15	Δt_{WO}		$\pm 0,2$ $\pm 0,2$ $\pm 0,2$	% % %	
Change in output O pulse width over V_{DD} range 5 to 15 V		Δt_{WO}		$\pm 1,5$	%	
Pulse width variation between circuits in same package	5 10 15	Δt_{WO}		± 1 ± 1 ± 1	% % %	
External timing resistor		R_t	5	—	⁽¹⁾	$k\Omega$
External timing capacitor		C_t	2000	—	no limits	pF
Input capacitance (pin 2 or 14)		C_{IN}		15		pF

Note

1. The maximum permissible resistance R_t , which holds the specified accuracy of t_{WO} , depends on the leakage current of the capacitor C_t and the leakage of the HEF4538B.

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- (1) Positive edge triggering.
- (2) Positive edge re-triggering (pulse lengthening).
- (3) Negative edge triggering.
- (4) Reset (pulse shortening).
- (5) $T = R_t \times C_t$.

Fig.6 Timing diagram.

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