Description

The SC2595 is an integrated linear DDR termination device which provides a complete solution for DDR termination designs while meeting the JEDEC requirements of SSTL-2 specifications for DDR-SDRAM termination.

The SC2595 can source and sink 1.5A current at the output V_{TT} while maintaining excellent load regulation.

V_{TT} is designed to track the V_{REF} voltage with a tight tolerance over the entire current range while preventing shoot through on the output stage.

A V_{SENSE} pin is incorporated to provide excellent load regulation, along with a buffered reference voltage.

The SC2595 incorporates a disable function built into the AV_{CC} pin to tri-state the output during Suspend To Ram (STR) states.

(Multiple patents pending.)

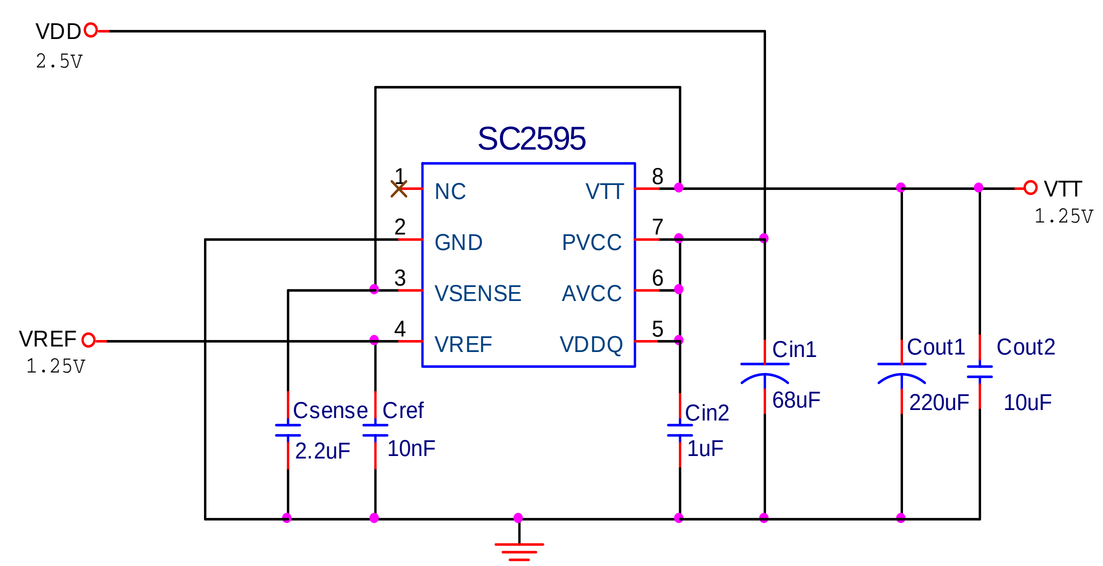
Features

- Available in the SOIC-8L EDP or MLPQ-16 package
- Regulates while sourcing or sinking 1.5A
- AV_{CC} range is from 2.5V to 5V
- Reference output
- Minimum number of external components
- Accurate internal voltage divider
- Disable function

Applications

- DDR memory termination
- High speed data line termination
- PC motherboards
- Graphics boards
- Disk drives
- CD-ROM drives

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
PVCC, AVCC, VDDQ to GND	V_{CC}	-0.3 to +6.0	V
Thermal Resistance Junction to Case SOIC-8L EDP MLPQ-16	θ_{JC}	 5.5 1.5	°C/W
Thermal Resistance Junction to Ambient SOIC-8L EDP MLPQ-16	θ_{JA}	 36.5 47	°C/W
Operating Temperature Range	T_A	-40 to +105	°C
Operating Junction Temperature Range	T_J	-40 to +150	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Peak IR Reflow Temperature 10 - 40s	T_{LEAD}	260	°C
ESD Rating (Human Body Model)	ESD	2	KV

Operating Range

Parameter	Symbol	Maximum	Units
Junction Temperature Range	T_J	-40 to +150	°C
AVCC to GND	AV_{CC}	2.3 to 5.5	V
PVCC to GND	PV_{CC}	2.3 to AV_{CC}	V

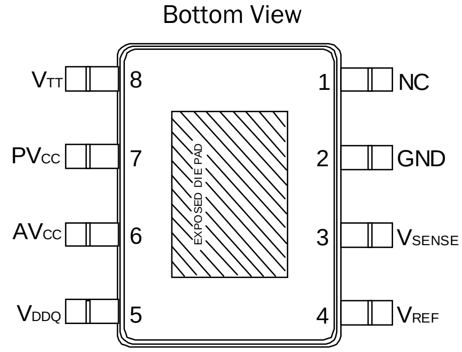
Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C and limits in boldface type apply over the full Operating Temperature Range (T_J = -40°C to +150°C). Unless otherwise specified, $AV_{CC} = PV_{CC}$ = 2.5V, V_{DDQ} = 2.5V.

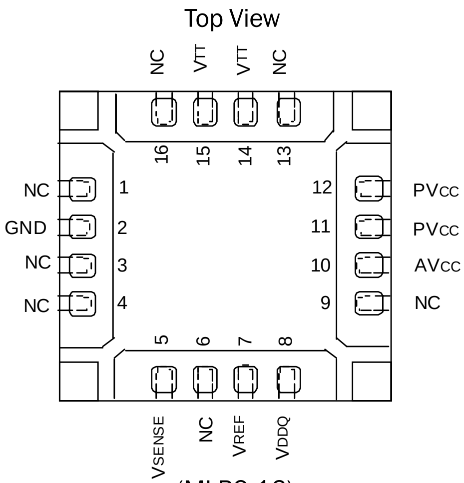
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reference Voltage	V_{REF}	I_{REF_OUT} = 0mA	VDDQ/2 - 40mV	1.25	VDDQ/2 + 40mV	V
Load Regulation (1)	REG_{LOAD}	I_{LOAD} : 0 to +1.5A I_{LOAD} : 0 to -1.5A		-0.5 +0.5		%
VTT Output Voltage Offset	VOS_{VTT}	I_{OUT}=0A, V_{TT}- V_{REF}	-20	0	+20	mV
Quiescent Current	I_Q	I_{LOAD} = 0A		400		µA
AVCC Enable Threshold				2.1		V
VDDQ Input Impedance	Z_{VDDQ}			100		kΩ

Note:
(1) For Load Regulation, use a 10ms current pulse width when measuring V_{TT}.

Pin Configuration



(SOIC-8L EDP)



(MLPQ-16)

Ordering Information

Part Number	Package	Temp. Range (T_A)
SC2595STR(1)	SOIC-8L EDP	-40 to +105°C
SC2595MLTR(1)	MLPQ-16	
SC2595STRT(1)(2)	SOIC-8L EDP	-40 to +105°C
SC2595MLTRT(1))(2)	MLPQ-16	
SC2595EVB	Evaluation Board	

Notes:

(1) Only available in tape and reel packaging. A reel contains 2500 devices for SOIC-8L and 3000 devices for MLPQ-16 package.

(2)Lead free package. Device is fully WEEE and RoHS compliant.

Pin Descriptions

(see Notes on page5).

SOIC-8L EDP Pin #	MLPQ-16 Pin #	Pin Name	Pin Function
1	1,3,4,6,9,-13,16	NC	No internal connection. (1)
2	2	GND	Ground.
3	5	VSENSE	V_{SENSE} is a feedback pin. V_{TT} plane is usually a narrow and long strip plane in most motherboard applications. This long strip plane will cause a large trace inductance and trace resistance. Consider the load transient condition; a fast load current going through V_{TT} strip plane can create voltage spikes on the V_{TT} plane. The load current can also cause a DC voltage drop on the V_{TT} plane. It is recommended that V_{SENSE} should be connected to the center of V_{TT} plane to improve the load regulation and the noise immunity. In case that one can't connect the V_{SENSE} pin to the center of the V_{TT} plane, one should connect it to the SC2595 V_{TT} pin directly. A longer trace of V_{SENSE} may pick up noise and cause the error of load regulation; hence the longer trace must be avoided. A 1uf to 2.2uf ceramic capacitor close to the V_{SENSE} pin is required to avoid oscillation during transient condition.
4	7	VREF	V_{REF} is an output pin, which provides the buffered output of the internal reference voltage. System designer can use the V_{REF} output voltage for Northbridge chipset and memory. Because these input pins are typically high impedance, there should be a small amount of current drawn from the V_{REF} pin [figure 9, 10]. To improve the noise immunity, a ceramic capacitor (10nF - 100nF) should be added from the V_{REF} pin to ground with short distance.
5	8	VDDQ(2)	The V_{DDQ} pin is an input for creating internal reference voltage to regulate $V_{TT.}$ The V_{DDQ} voltage is connected to internal 50Kohm resistor divider. The central tap of resistor divider ($V_{DDQ}/2$) is connected to the internal voltage buffer, which output is connected to V_{REF} pin and the non-inverting input of the error amplifier as the reference voltage. With the feedback loop closed, the V_{TT} output voltage will always track the $V_{DDQ}/2$ precisely. It is a recommended that a 1uF ceramic capacitor should be added next to the V_{DDQ} pin to increase the noise immunity.
6	10	AVCC (2)	The AV_{CC} pin is used to supply all of the internal control circuitry. AV_{CC} voltage has to be greater than its UVLO threshold voltage (2.1V typical) to allow the SC2595 be in normal operation. If AV_{CC} voltage is lower than the UVLO threshold voltage, the V_{TT} output voltage will remain at 0V.
7	11,12	PVCC (2)	The PV_{CC} pin provides the rail voltage from where the V_{TT} pin draws load current. There is a limitation between AV_{CC} and PV_{CC}. The PV_{CC} voltage must be less or equal to AV_{CC} voltage to ensure the correct output voltage regulation. The V_{TT} source current capability is dependent on PV_{CC} voltage. Higher the voltage on PV_{CC}, higher the source current; however, it will cause more power loss and higher temperature rise [figure 5, 11, 12].
8	14,15	VTT	The V_{TT} pin is the output of SC2595. It can sink and source 1.5A continuous current and 3A peak current while keeping excellent load regulation. It is recommended that one should use at least 220uF low ESR capacitors and 10uF ceramic capacitors, which are uniformly spread on the V_{TT} strip plane to reduce the voltage spike under load transient condition.

Pin Descriptions (Cont.)

Notes:

(1) Can be used for vias.

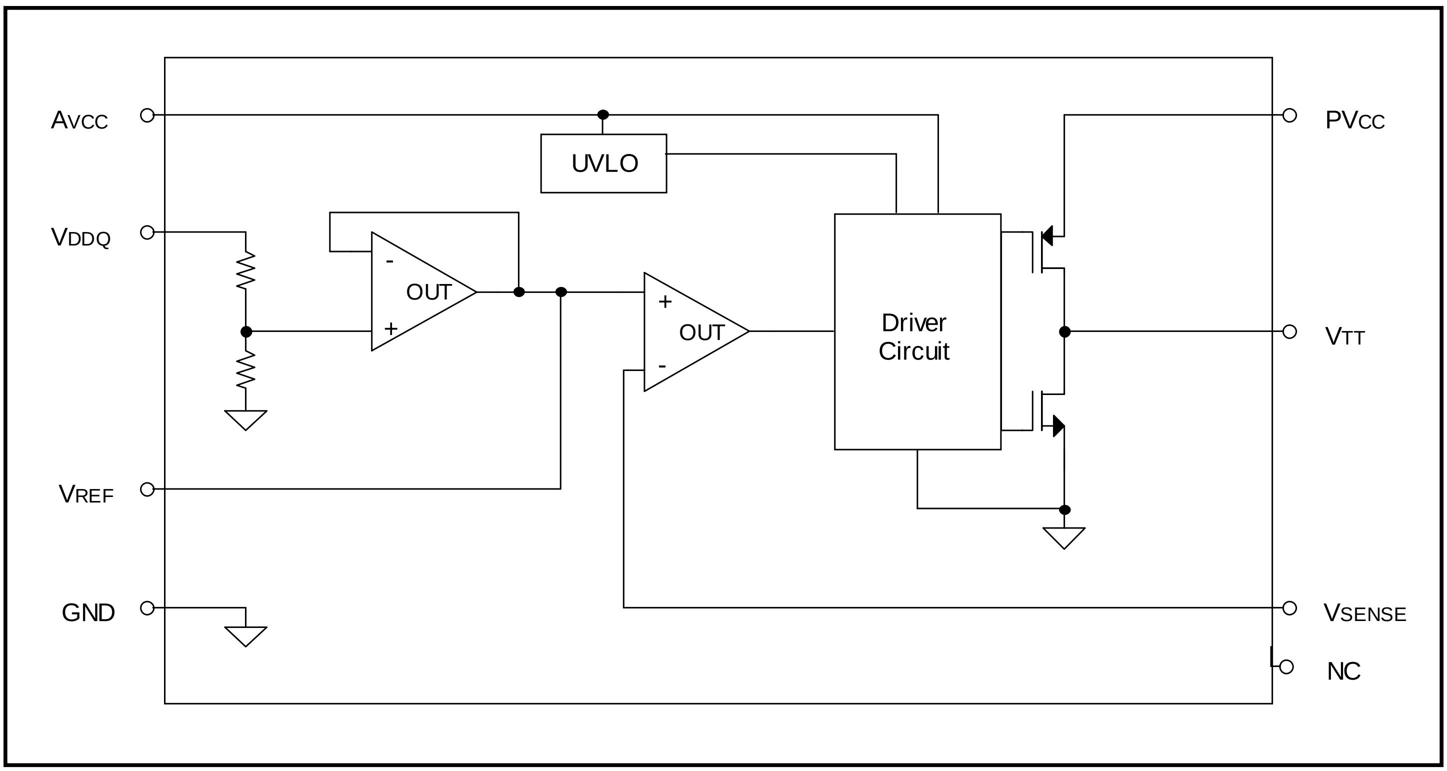
(2) Power up of AV_{CC}, PV_{CC} and V_{DDQ} supplies.

(a) The preferred mode of operation is when the AV_{CC}, PV_{CC} and V_{DDQ} pins are tied together to a single supply.

(b) If and when AV_{CC}, PV_{CC} pins are tied to a supply separate to that of the V_{DDQ} supply pin; then the V_{DDQ} supply should lead AV_{CC}, PV_{CC} supply or the V_{DDQ} supply and the AV_{CC}, PV_{CC} supply should rise simultaneously.

(c) If the AV_{CC}, PV_{CC} and V_{DDQ} supply pins are connected in a way such that, AV_{CC}, PV_{CC} supplies precedes V_{DDQ} supply; then V_{TT} output precedes V_{DDQ}. This can cause the SDRAM device to latch-up, which may cause permanent damage to the SDRAM.

Block Diagram



Application Information

Overview

Double Data Rate (DDR) SDRAM was defined by JEDEC 1997. While today's DDR SDRAM has a clock speed the the same as previous SDRAM, its data transfer speeds are now twice that of SDRAM. The requirement voltage range has changed as well, from 3.3V to 2.5V, and the power dissipation is smaller than that SDRAM. For the above reasons, DDR is very popular and is widely used in a multitude of applications, including PC motherboards, notebook boards, video cards, CD-ROM drives and disk drives.

To obtain an appropriate DDR power management solution, SYSTEM DESIGNERS can be select between two topologies. One solution is a switching mode regulator that features greater sink/source current capability along with a higher cost and greater board space requirements. The other solution is a linear mode regulator which costs less and requires less board space. For two DIMM motherboards, system designers prefer the linear mode solution.

Typical Application Circuits & Waveforms

Two different application circuits are shown below in Figure 1 and 2. Each circuit is designed for a specific condition; details are provided with each example. See Note 1 below for recommended power-up sequencing.

Application_1: Standard SSTL-2 Application

The AV_{CC} pin, the PV_{CC} pin, and the V_{DDQ} pin can be tied together for SSTL-2 application. It only needs a 2.5V power rail for normal operation. System designer can save the PCB space and reduce the cost. Please refer to figures 3 and 4 for test waveforms.

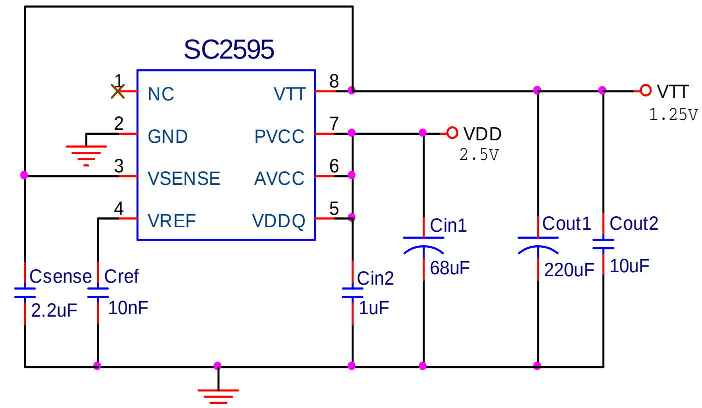


Figure 1: Standard SSTL-2 application

Application_2: Lower Power Loss Configuration for SSTL-2

If power loss is a major concern, separating the PV_{CC} form the AV_{CC} and the V_{DDQ} will be a good choice. The PV_{CC} can operate at lower voltage (1.8V to 2.5V) if 2.5V voltage is applied on AV_{CC} and the V_{DDQ}, but the source current is lower due to the lower operating voltage applied on the PV_{CC}. Please find the relative test result in Figures 5, 11 and 12.

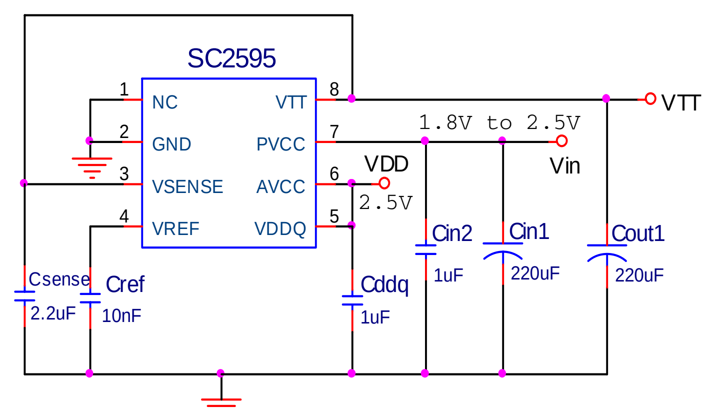


Figure 2: Lower power loss for SSTL-2 application

Application Information (Cont.)

Notes:

(1) Power up of AV_{CC}, PV_{CC} and V_{DDQ} supplies.

(a) The preferred mode of operation is when the AV_{CC}, PV_{CC} and V_{DDQ} pins are tied together to a single supply.

(b) If and when AV_{CC}, PV_{CC} pins are tied to a supply separate to that of the V_{DDQ} supply pin; then the V_{DDQ} supply should lead AV_{CC}, PV_{CC} supply or the V_{DDQ} supply and the AV_{CC}, PV_{CC} supply should rise simultaneously.

(c) If the AV_{CC}, PV_{CC} and V_{DDQ} supply pins are connected in a way such that, AV_{CC}, PV_{CC} supplies precedes V_{DDQ} supply; then V_{TT} output precedes V_{DDQ}. This can cause the SDRAM device to latch-up, which may cause permanent damage to the SDRAM.

Layout guidelines

1)The SC2595 has a power SO-8 package. It can improve the thermal impedance (θ_{JC}) significantly. A suitable thermal pad should be added to the PCB layout. Some thermal vias are required to connect the thermal pad to the PCB ground layer. This will improve the thermal performance .

2)To increase the noise immunity, a ceramic capacitor of 10nf to 100nf is required to decouple the V_{REF} pin with the shortest connection trace, also a 1uF to 2.2uF ceramic capacitor close to the V_{SENSE} pin is required to avoid oscillation during transient condition.

3)To reduce the noise on the input power rail for standard SSTL-2 application, a 68μF low ESR capacitor and a 1μF ceramic capacitor have to be used on the input power rail with shortest possible connection.

4)For a low power loss SSTL-2 application, a 220μF AL. capacitor and a 1μF ceramic must be added on the PV_{CC} pin; there should also be a 1μF ceramic capacitor added on the V_{DDQ} pin with shortest possible connections.

5)V_{TT} output copper plane should be as large as possible.

6)V_{SENSE} trace should be as short as possible.

Test Waveforms

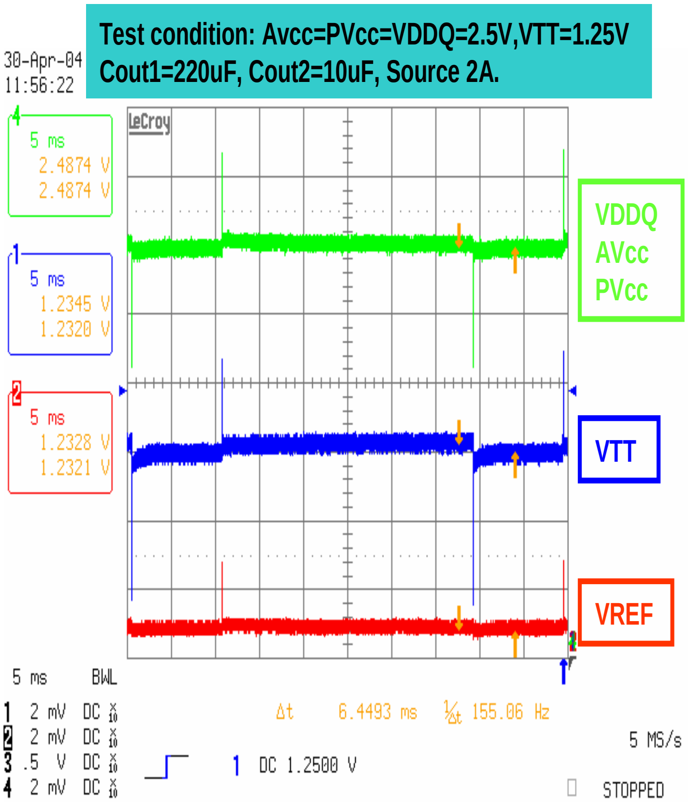


Figure 3

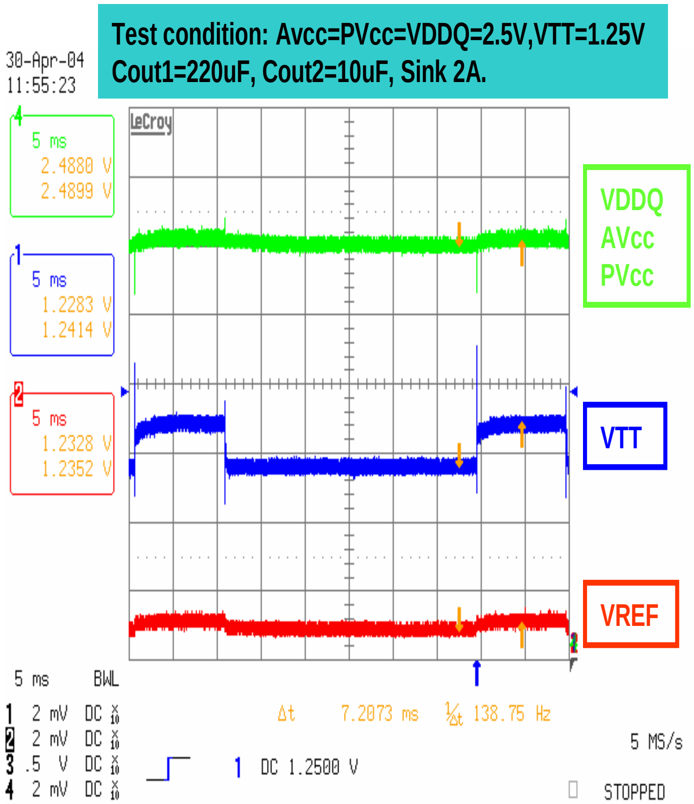


Figure 4

Typical Characteristics

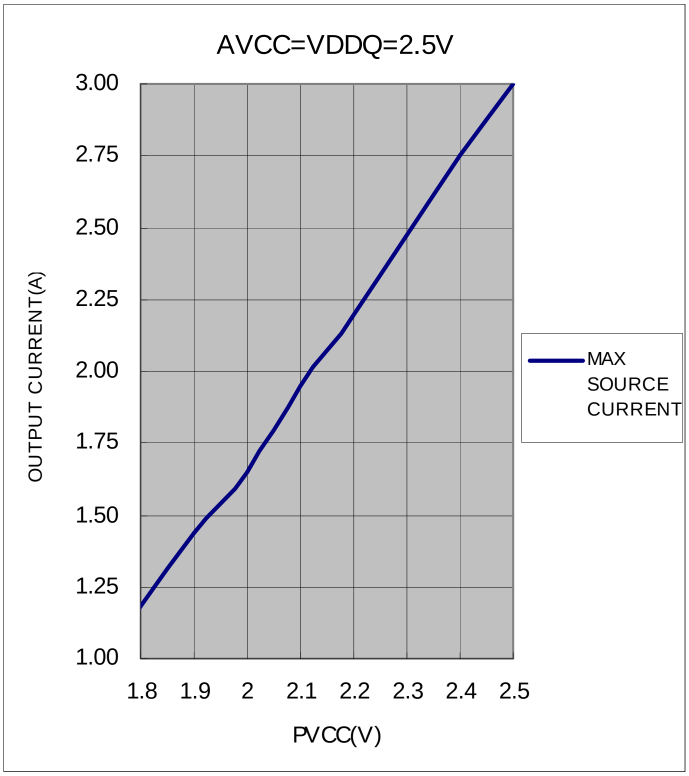


Figure 5

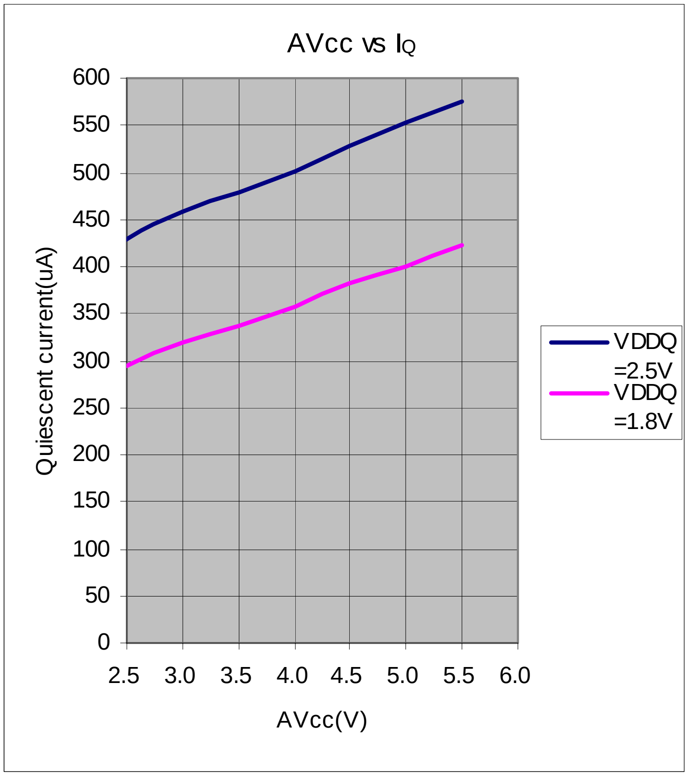


Figure 6

Typical Characteristics (Cont.)

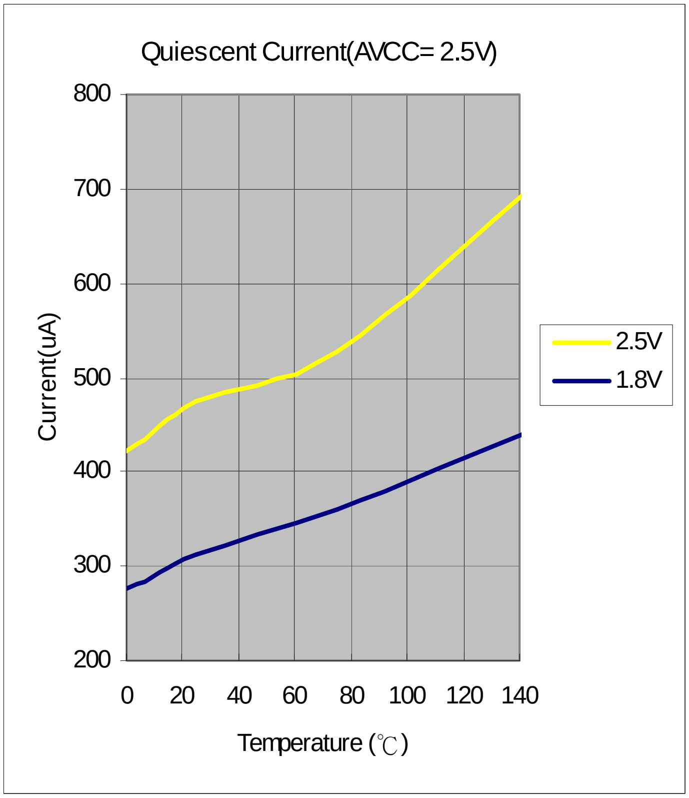


Figure 7

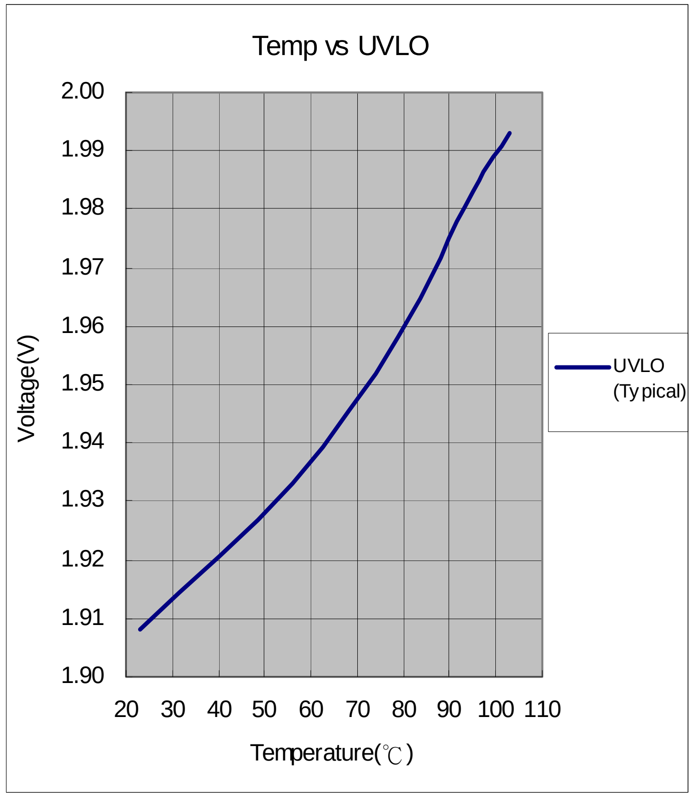


Figure 8

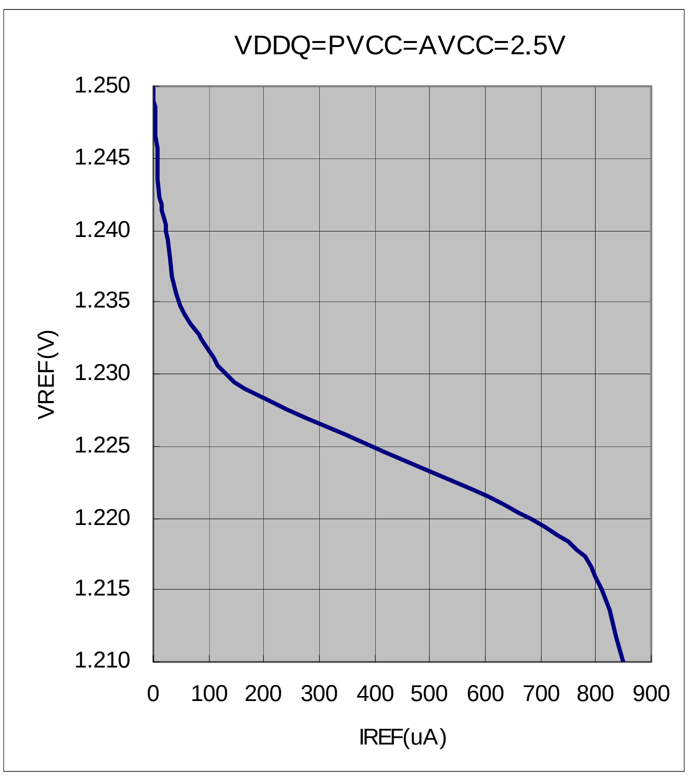


Figure 9

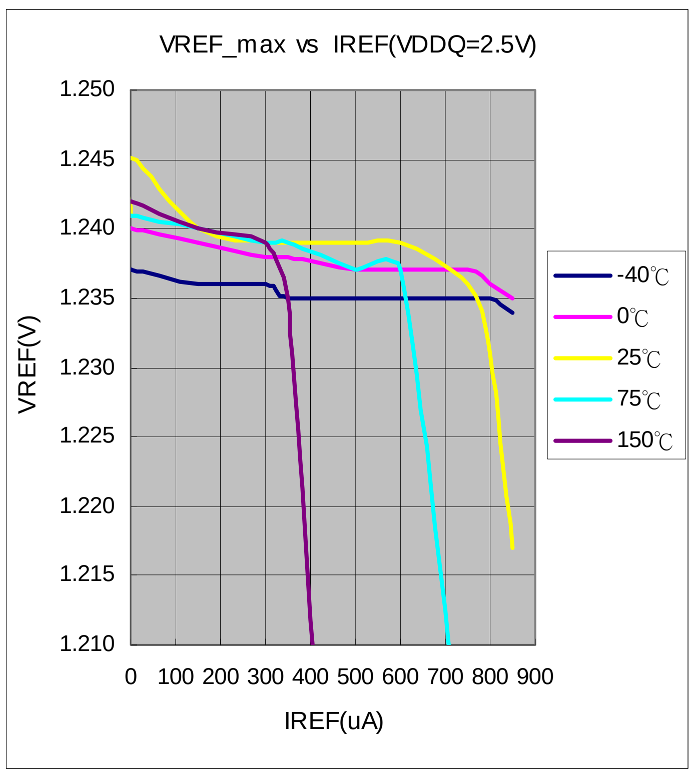


Figure 10

Typical Characteristics (Cont.)

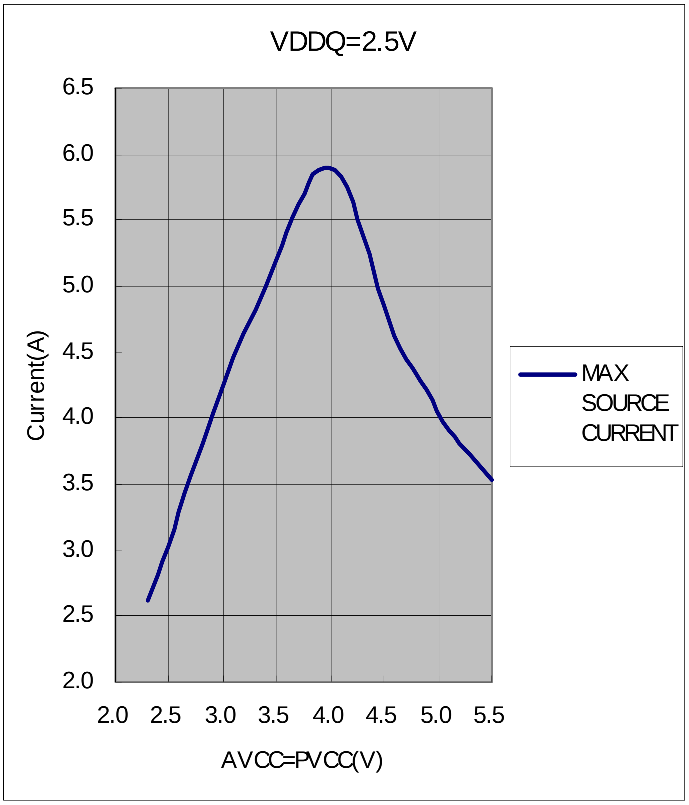


Figure 11

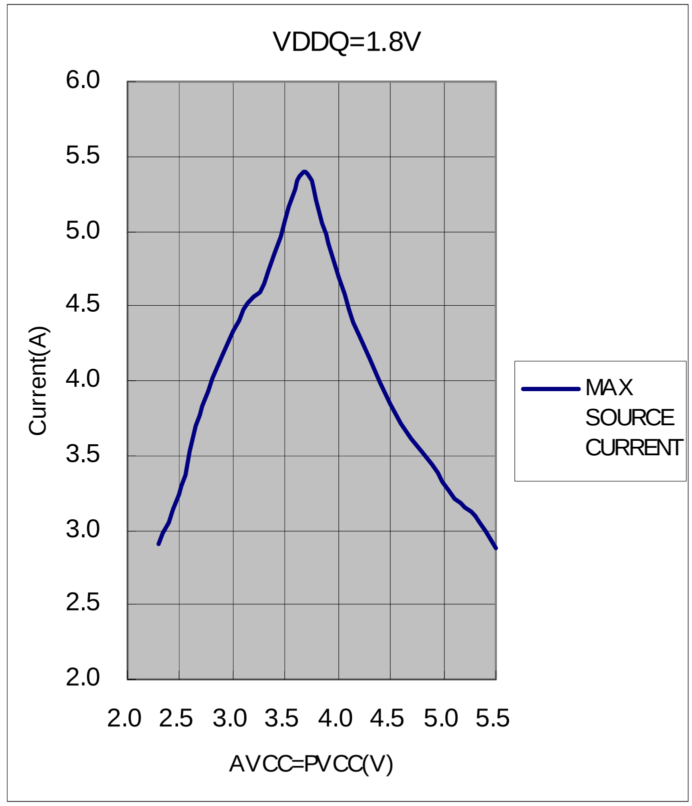


Figure 12

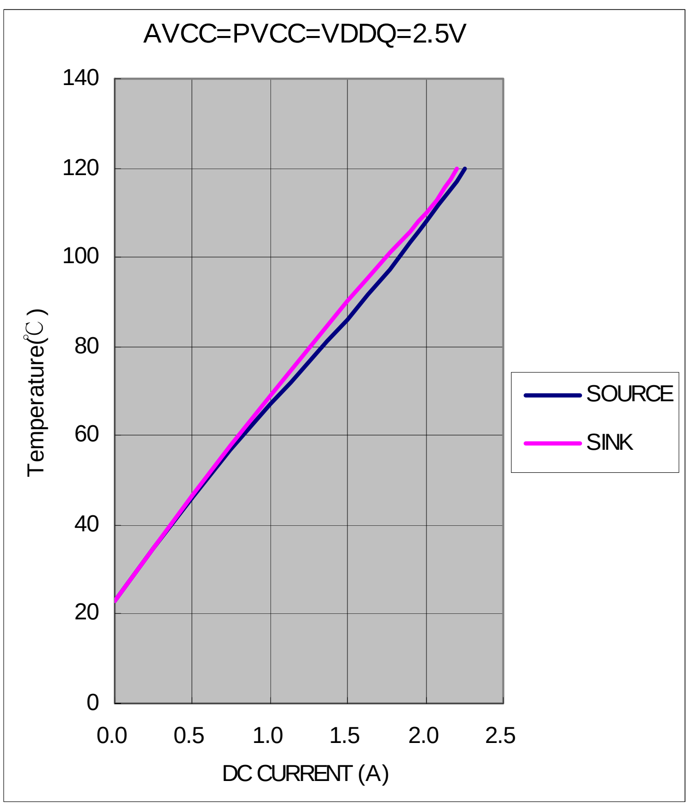
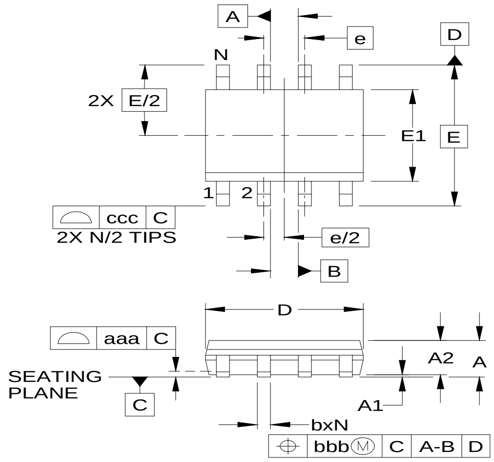
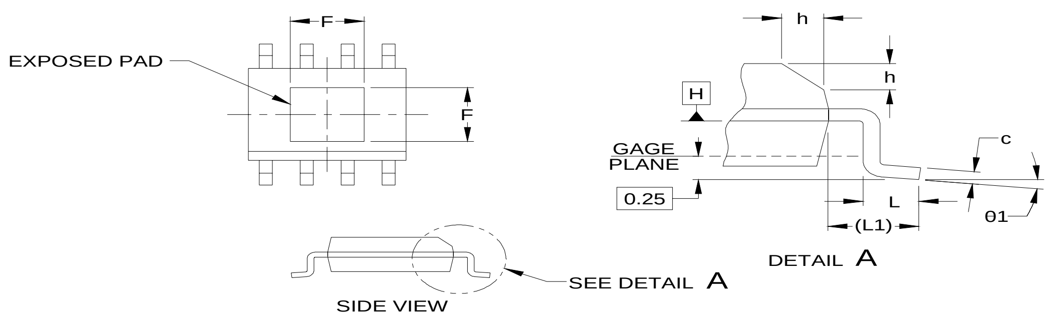


Figure 13

Outline Drawing - Power SOIC-8L



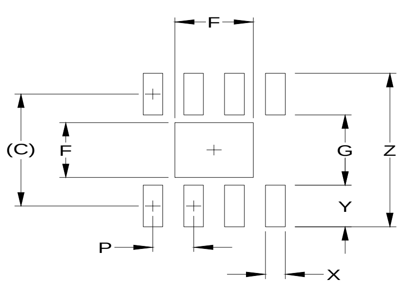
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
F	.086	.090	.094	2.19	2.29	2.39
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.05)		
N	8			8		
θ1	0	-	8	0	-	8
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Land Pattern - Power SOIC-8L



DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
F	.096	2.44
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

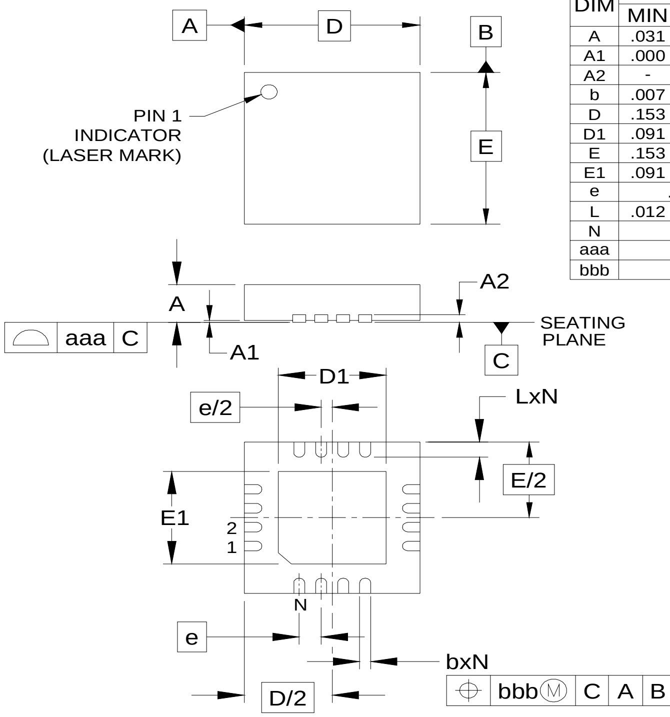
NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111   FAX (805)498-3804

Outline Drawing - MLP-16 (4 x 4 x 0.9mm)

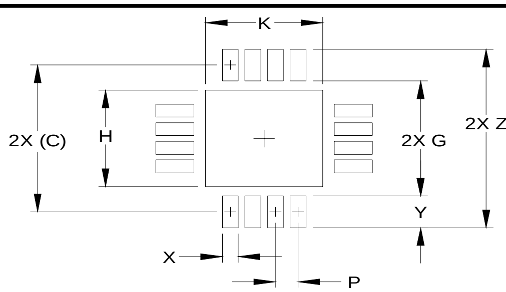


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.040	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.153	.157	.161	3.90	4.00	4.10
D1	.091	.096	.100	2.30	2.45	2.55
E	.153	.157	.161	3.90	4.00	4.10
E1	.091	.096	.100	2.30	2.45	2.55
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	16			16		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 2.9 x 2.9 mm

Land Pattern - MLP-16 (4 x 4 x 0.9mm)



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.156)	(3.95)
G	.122	3.10
H	.102	2.60
K	.102	2.60
P	.020	0.50
X	.012	0.30
Y	.033	0.85
Z	.189	4.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Contact Information

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