

FEATURES

- Member of the Texas Instruments Widebus+™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- B-Port Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- UBE™ (Universal Bus Exchanger) Allows Synchronous Data Exchange
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

NOTE: For tape-and-reel order entry, the DGG package is abbreviated to GR, and the DLR package is abbreviated to LR.

DESCRIPTION

This 9-bit, 4-port universal bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCHR16409 allows synchronous data exchange between four different buses. Data flow is controlled by the select (SEL0-SEL4) inputs. A data-flow state is stored on the rising edge of the clock (CLK) input if the select-enable ($\overline{SELEN}$) input is low. Once a data-flow state has been established, data is stored in the flip-flop on the rising edge of CLK if $\overline{SELEN}$ is high.

The data-flow control logic is designed to allow glitch-free data transmission.

The B outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω series resistors to reduce overshoot and undershoot.

When preset ($\overline{PRE}$) transitions high, the outputs are disabled immediately, without waiting for a clock pulse. To leave the high-impedance state, both $\overline{PRE}$ and $\overline{SELEN}$ must be low, and a clock pulse must be applied.

To ensure the high-impedance state during power up or power down, $\overline{PRE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCHR16409 is characterized for operation from -40°C to 85°C.

**DGG OR DL PACKAGE
(TOP VIEW)**

$\overline{PRE}$	1	56	CLK
SEL0	2	55	$\overline{SELEN}$
1A1	3	54	1B1
GND	4	53	GND
1A2	5	52	1B2
1A3	6	51	1B3
V_{CC}	7	50	V_{CC}
1A4	8	49	1B4
1A5	9	48	1B5
1A6	10	47	1B6
GND	11	46	GND
1A7	12	45	1B7
1A8	13	44	1B8
1A9	14	43	1B9
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2A9	26	31	2B9
SEL1	27	30	SEL4
SEL2	28	29	SEL3



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus+, EPIC, UBE are trademarks of Texas Instruments.

SN74ALVCHR16409
9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER
WITH 3-STATE OUTPUTS

SCES056H—SEPTEMBER 1995—REVISED OCTOBER 2004

FUNCTION TABLES

INPUTS		OUTPUT RECEIVE PORT
CLK	SEND PORT	
X	X	$B_0^{(1)}$
X	L	L
X	H	H
↑	L	L
↑	H	H
H	X	$B_0^{(1)}$
L	X	$B_0^{(1)}$

- (1) Output level before the indicated steady-state input conditions were established

DATA-FLOW CONTROL

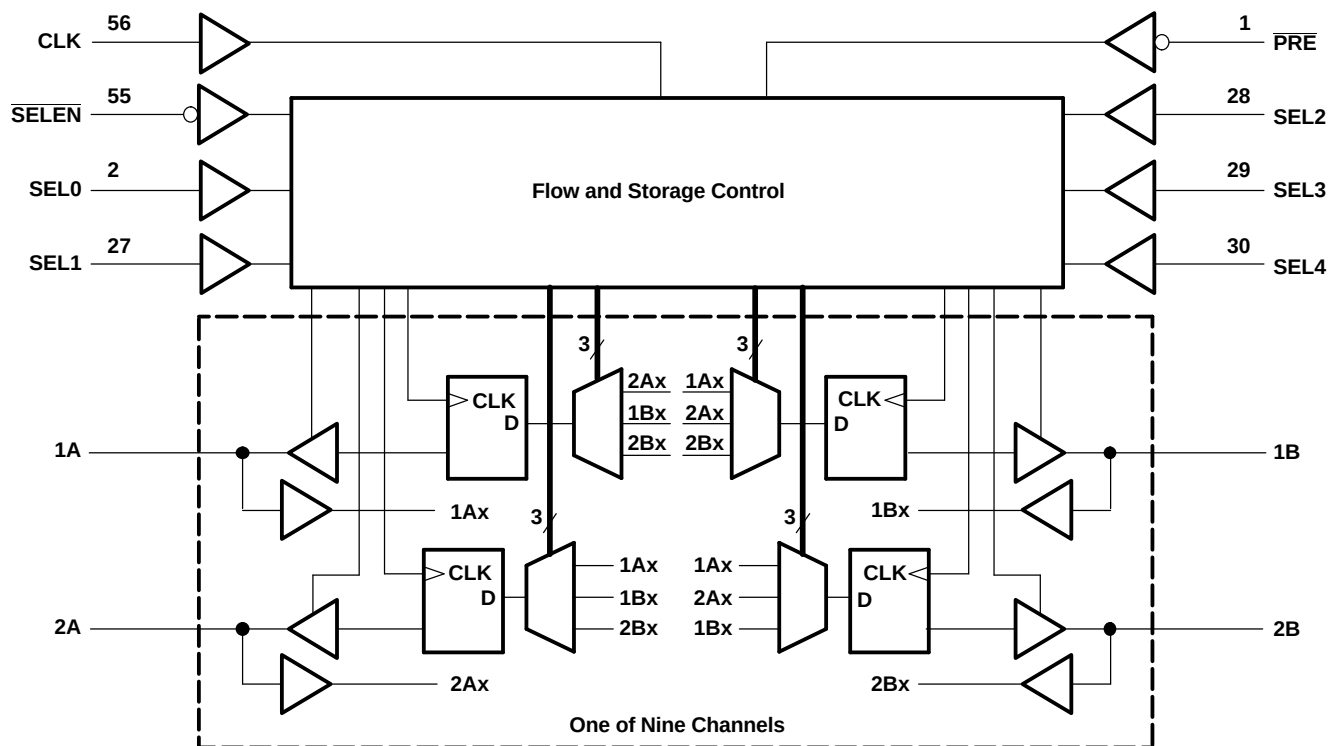
INPUTS								DATA FLOW
PRE	SELEN	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	
H	X	X	X	X	X	X	X	All outputs disabled
L	H	↑	X	X	X	X	X	No change
L	L	↑	0	0	0	0	0	None, all I/Os off
L	L	↑	0	0	0	0	1	Not used
L	L	↑	0	0	0	1	0	Not used
L	L	↑	0	0	0	1	1	Not used
L	L	↑	0	0	1	0	0	Not used
L	L	↑	0	0	1	0	1	Not used
L	L	↑	0	0	1	1	0	Not used
L	L	↑	0	0	1	1	1	Not used
L	L	↑	0	1	0	0	0	2A to 1A and 1B to 2B
L	L	↑	0	1	0	0	1	2A to 1A
L	L	↑	0	1	0	1	0	2B to 1B
L	L	↑	0	1	0	1	1	2A to 1A and 2B to 1B
L	L	↑	0	1	1	0	0	1A to 2A and 1B to 2B
L	L	↑	0	1	1	0	1	1A to 2A
L	L	↑	0	1	1	1	0	1B to 2B
L	L	↑	0	1	1	1	1	1A to 2A and 2B to 1B
L	L	↑	1	0	0	0	0	1A to 1B and 2B to 2A
L	L	↑	1	0	0	0	1	1A to 1B
L	L	↑	1	0	0	1	0	2A to 2B
L	L	↑	1	0	0	1	1	1A to 1B and 2A to 2B
L	L	↑	1	0	1	0	0	1B to 1A and 2A to 2B
L	L	↑	1	0	1	0	1	1B to 1A
L	L	↑	1	0	1	1	0	2B to 2A
L	L	↑	1	0	1	1	1	1B to 1A and 2B to 2A
L	L	↑	1	1	0	0	0	2B to 1A and 2A to 1B
L	L	↑	1	1	0	0	1	1B to 2A
L	L	↑	1	1	0	1	0	2B to 1A
L	L	↑	1	1	0	1	1	2B to 1A and 1B to 2A
L	L	↑	1	1	1	0	0	1A to 2B and 1B to 2A
L	L	↑	1	1	1	0	1	1A to 2B
L	L	↑	1	1	1	1	0	2A to 1B
L	L	↑	1	1	1	1	1	1A to 2B and 2A to 1B

SN74ALVCHR16409

9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES056H–SEPTEMBER 1995–REVISED OCTOBER 2004

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
V _I	Input voltage range	Except I/O ports ⁽²⁾	-0.5	4.6	V
		I/O ports ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	
V _O	Output voltage range ⁽²⁾⁽³⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	-50		mA
I _{OK}	Output clamp current	V _O < 0	-50		mA
I _O	Continuous output current		±50		mA
Continuous current through each V _{CC} or GND			±100		mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DGG package	81		°C/W
		DL package	74		
T _{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V		-2	mA
		V _{CC} = 2.3 V		-6	
		V _{CC} = 2.7 V		-8	
		V _{CC} = 3 V		-12	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		2	mA
		V _{CC} = 2.3 V		6	
		V _{CC} = 2.7 V		8	
		V _{CC} = 3 V		12	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74ALVCHR16409
9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER
WITH 3-STATE OUTPUTS

SCES056H–SEPTEMBER 1995–REVISED OCTOBER 2004

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OH}		$I_{OH} = -100 \mu A$	1.65 V to 3.6 V	$V_{CC} - 0.2$			V
		$I_{OH} = -2 \text{ mA}$	1.65 V	1.2			
		$I_{OH} = -4 \text{ mA}$	2.3 V	1.9			
		$I_{OH} = -6 \text{ mA}$	2.3 V	1.7			
			3 V	2.4			
		$I_{OH} = -8 \text{ mA}$	2.7 V	2			
		$I_{OH} = -12 \text{ mA}$	3 V	2			
V_{OL}		$I_{OL} = 100 \mu A$	1.65 V to 3.6 V			0.2	V
		$I_{OL} = 2 \text{ mA}$	1.65 V			0.45	
		$I_{OL} = 4 \text{ mA}$	2.3 V			0.4	
		$I_{OL} = 6 \text{ mA}$	2.3 V			0.55	
			3 V			0.55	
		$I_{OL} = 8 \text{ mA}$	2.7 V			0.6	
		$I_{OL} = 12 \text{ mA}$	3 V			0.8	
I_I		$V_I = V_{CC}$ or GND	3.6 V			± 5	μA
$I_{I(\text{hold})}$		$V_I = 0.58 \text{ V}$	1.65 V	25			μA
		$V_I = 1.07 \text{ V}$		-25			
		$V_I = 0.7 \text{ V}$	2.3 V	45			
		$V_I = 1.7 \text{ V}$		-45			
		$V_I = 0.8 \text{ V}$	3 V	75			
		$V_I = 2 \text{ V}$		-75			
		$V_I = 0 \text{ to } 3.6 \text{ V}^{(2)}$	3.6 V			± 500	
$I_{OZ}^{(3)}$		$V_O = V_{CC}$ or GND	3.6 V			± 10	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μA
ΔI_{CC}		One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V		4		pF
C_{iO}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V		8		pF

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

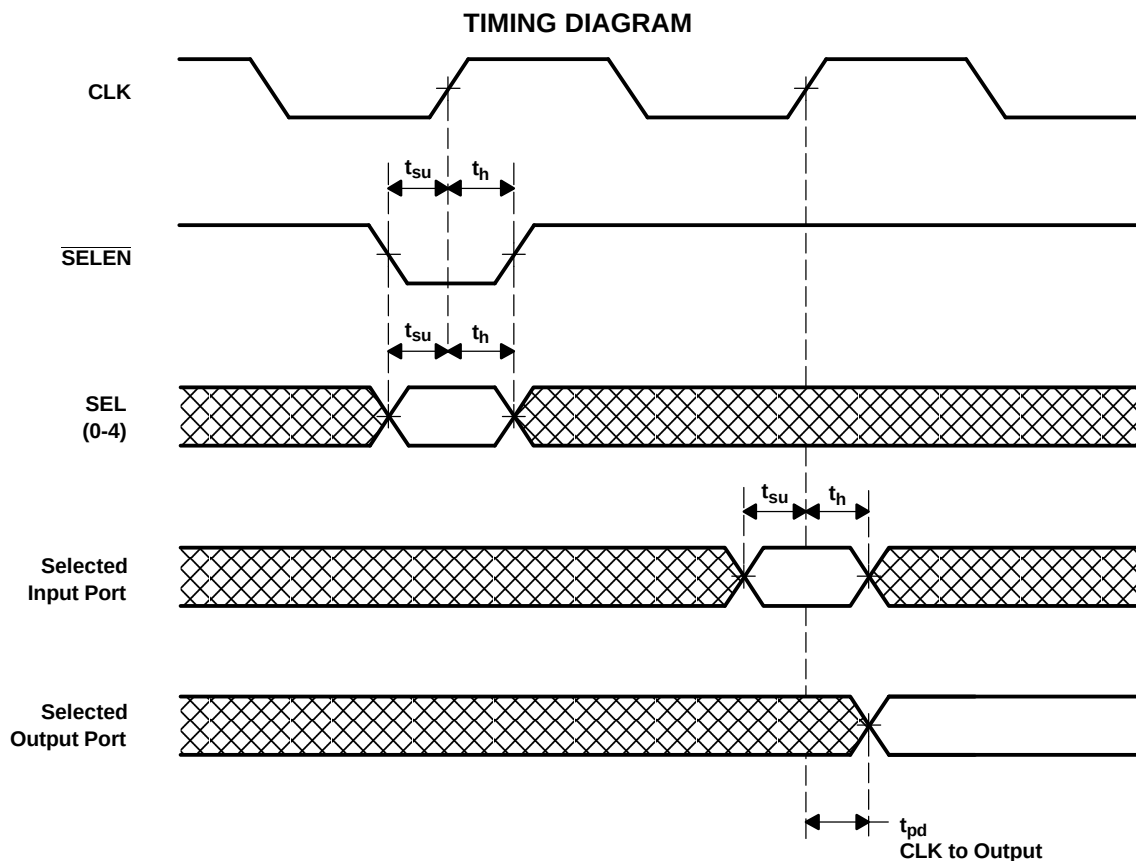
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

			V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		(1)		120		120		120		MHz
t _w	Pulse duration, CLK high or low		(1)		4.2		4.2		3		ns
t _{su}	Setup time	A or B before CLK↑	(1)		1.9		1.9		1.4		ns
		SEL before CLK↑	(1)		5.1		4.2		3.5		
		$\overline{\text{SELEN}}$ before CLK↑	(1)		2.5		2.5		1.8		
		$\overline{\text{PRE}}$ before CLK↑	(1)		1		1		0.7		
t _h	Hold time	A or B after CLK↑	(1)		0.8		0.8		1		ns
		SEL after CLK↑	(1)		0		0		0		
		$\overline{\text{SELEN}}$ after CLK↑	(1)		0.5		0.5		0.8		

(1) This information was not available at the time of publication.



SN74ALVCHR16409

9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES056H–SEPTEMBER 1995–REVISED OCTOBER 2004

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			(1)		120		120		120		MHz
t _{pd}	CLK	A or B		(1)	1.5	6.9	7		1.5	6.2	ns
t _{en}	CLK	A or B		(1)	2.4	7.8	7.6		2	6.8	ns
t _{dis}	CLK	A or B		(1)	2.3	7.1	6.4		2	6.1	ns
	$\overline{\text{PRE}}$			(1)	2.8	7.7	7		2.5	6.4	

(1) This information was not available at the time of publication.

OPERATING CHARACTERISTICS

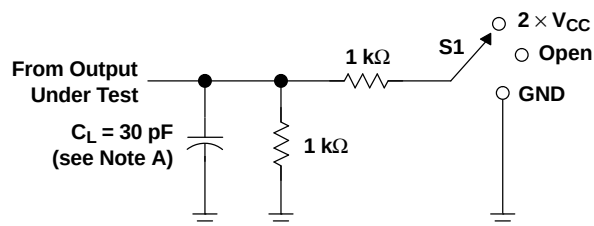
T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	All outputs enabled	C _L = 50 pF, f = 10 MHz	(1)	60	60	pF
		All outputs disabled		(1)	60	60	

(1) This information was not available at the time of publication.

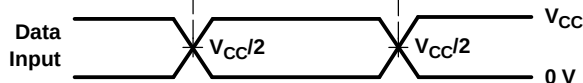
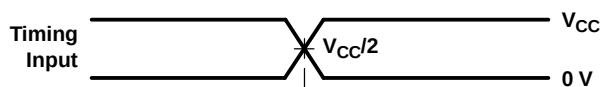
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8 \text{ V}$

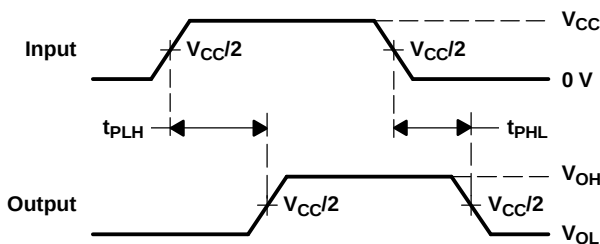


LOAD CIRCUIT

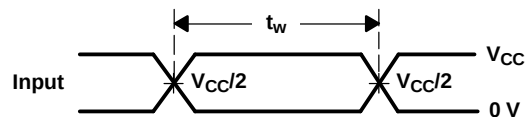
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



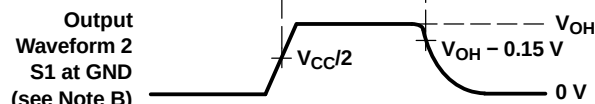
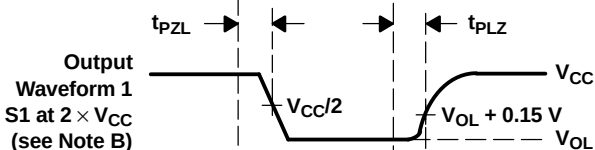
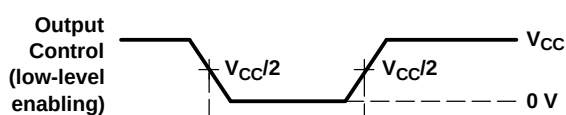
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



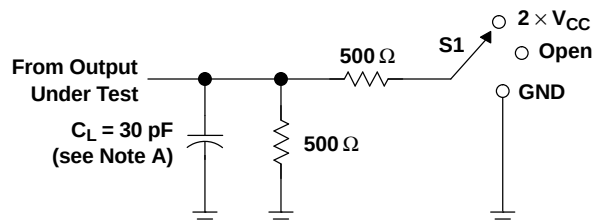
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

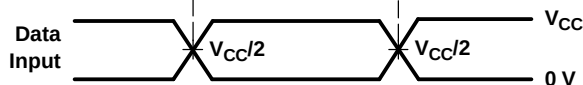
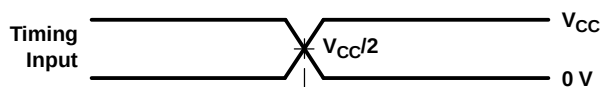
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

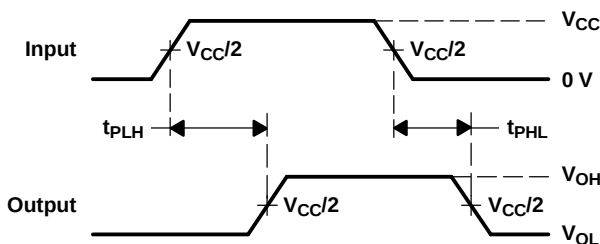


LOAD CIRCUIT

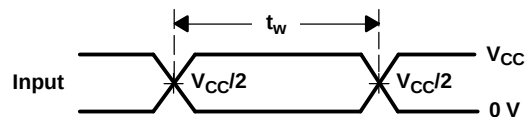
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



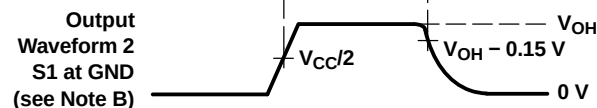
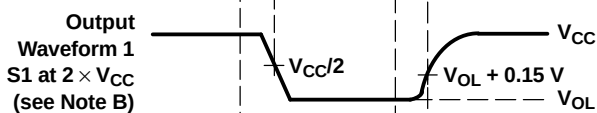
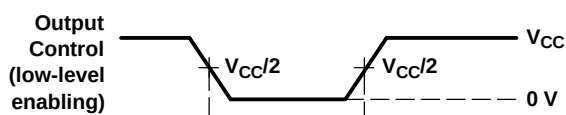
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



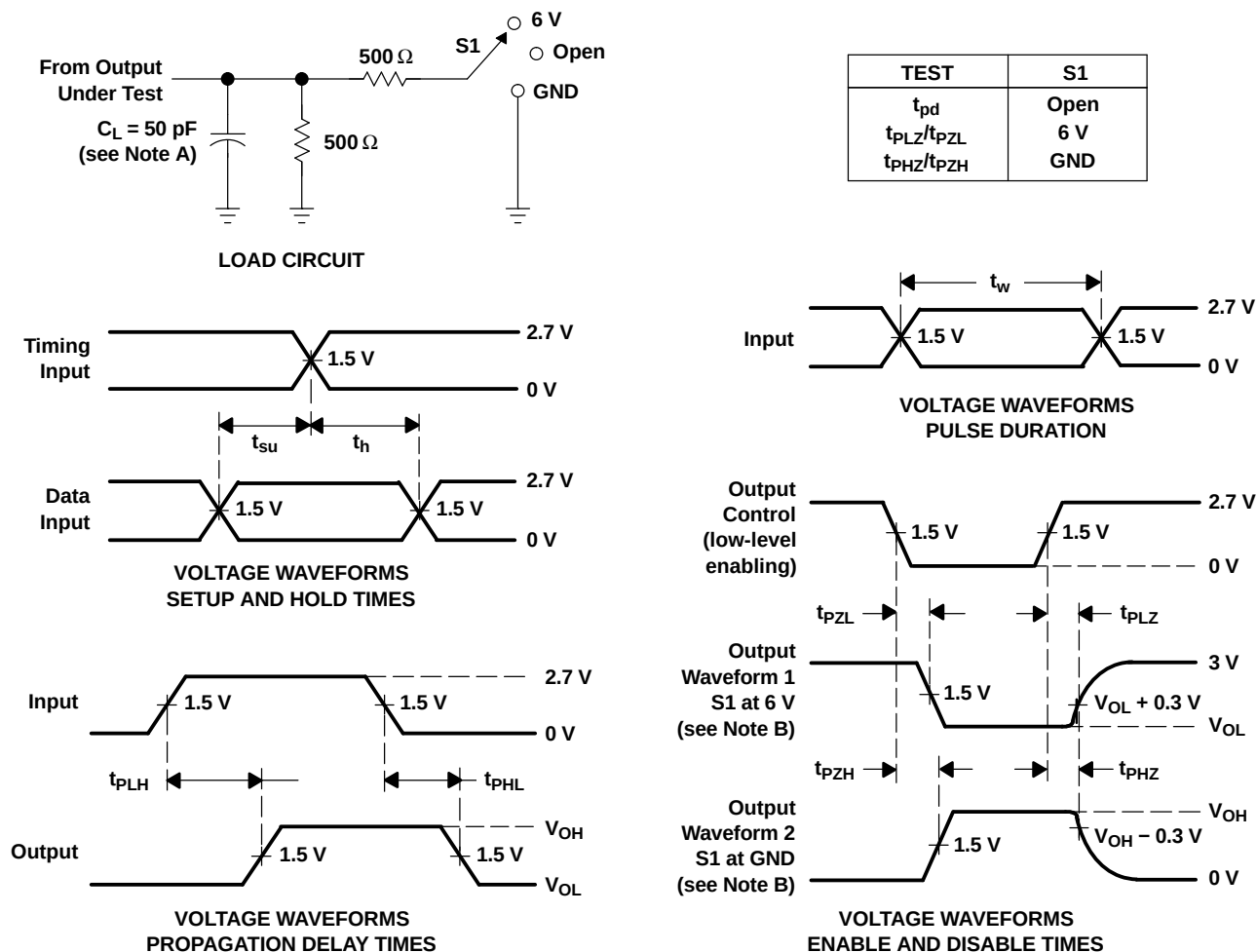
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$



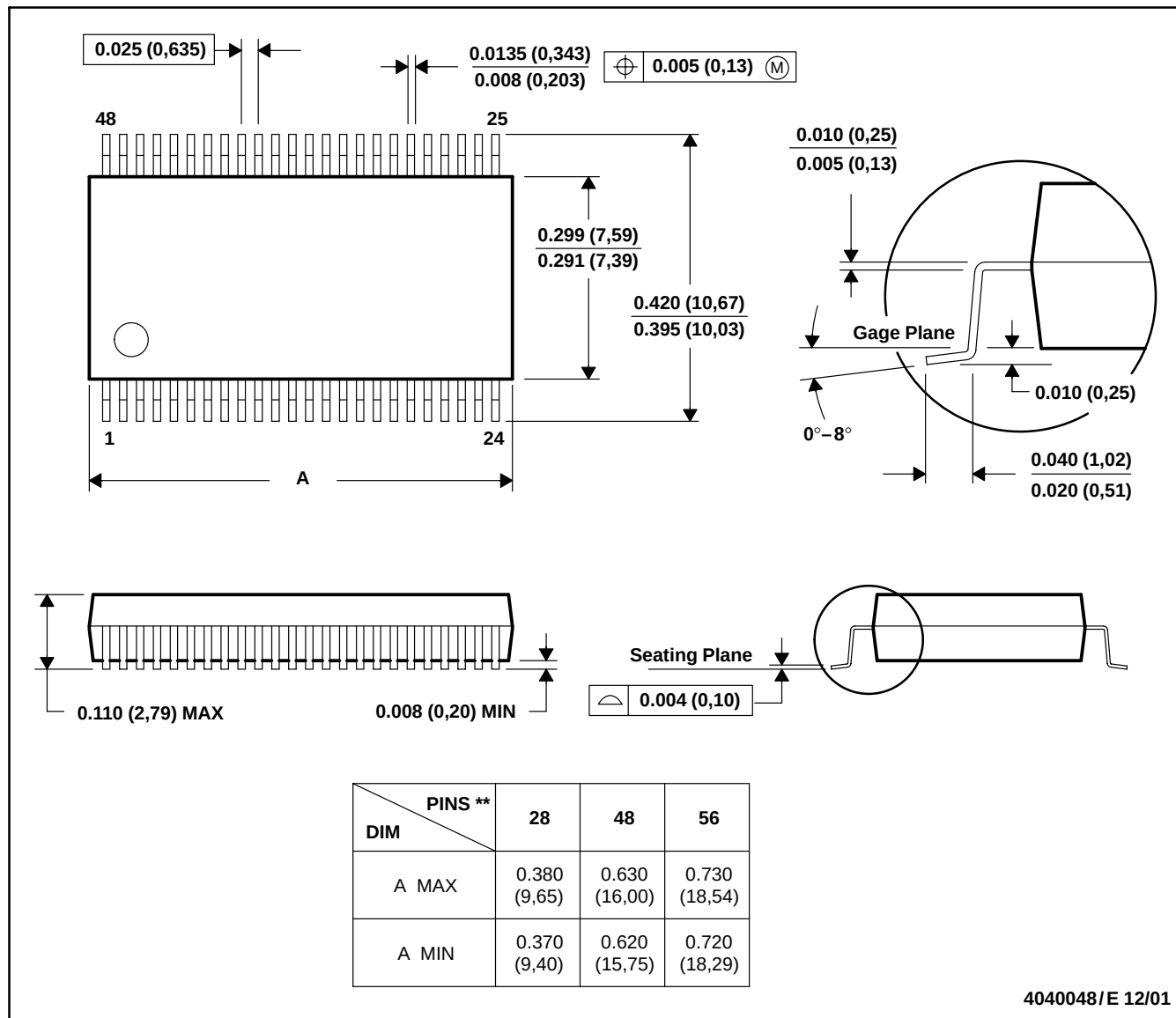
- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

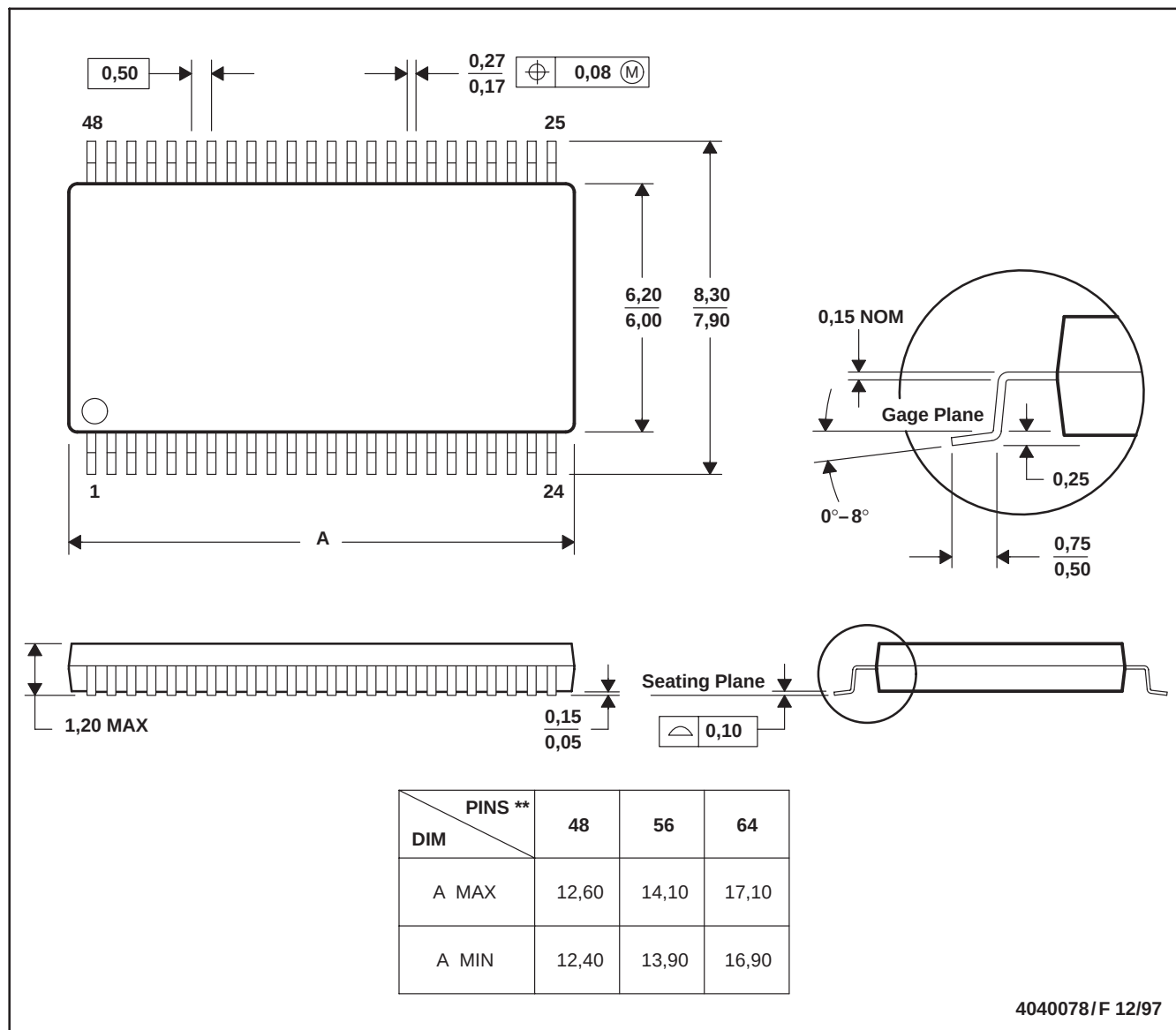


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated