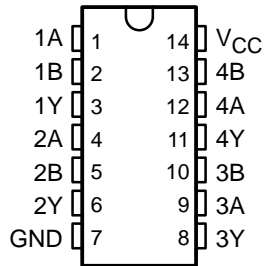


# SN54HCT32, SN74HCT32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

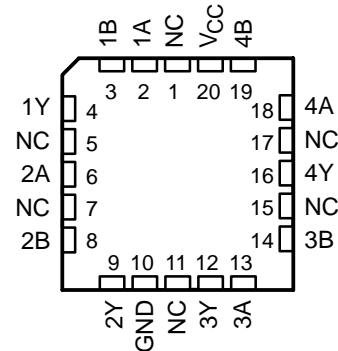
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- Operating Voltage Range of 4.5 V to 5.5 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20-μA Max  $I_{CC}$
- Typical  $t_{pd} = 13$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Inputs Are TTL-Voltage Compatible

SN54HCT32 ... J OR W PACKAGE  
SN74HCT32 ... D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HCT32 ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'HCT32 devices contain four independent 2-input OR gates. They perform the Boolean function  $Y = \overline{A} \cdot \overline{B}$  or  $Y = A + B$  in positive logic.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74HCT32N	SN74HCT32N
	SOIC – D	Tube	SN74HCT32D	HCT32
		Tape and reel	SN74HCT32DR	
	SOP – NS	Tape and reel	SN74HCT32NSR	HCT32
	SSOP – DB	Tape and reel	SN74HCT32DBR	HT32
	TSSOP – PW	Tube	SN74HCT32PW	HT32
Tape and reel		SN74HCT32PWR		
–55°C to 125°C	CDIP – J	Tube	SNJ54HCT32J	SNJ54HCT32J
	CFP – W	Tube	SNJ54HCT32W	SNJ54HCT32W
	LCCC – FK	Tube	SNJ54HCT32FK	SNJ54HCT32FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L



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**TEXAS  
INSTRUMENTS**

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SN54HCT32, SN74HCT32  
QUADRUPLE 2-INPUT POSITIVE-OR GATES

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	−0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, $T_{stg}$	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54HCT32			SN74HCT32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		2	2			V
$V_{IL}$	Low-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		0.8	0.8			V
$V_I$	Input voltage	0	$V_{CC}$		0	$V_{CC}$		V
$V_O$	Output voltage	0	$V_{CC}$		0	$V_{CC}$		V
$\Delta t/\Delta v$	Input transition rise/fall time	500			500			ns
$T_A$	Operating free-air temperature	−55	125		−40	85		°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT32		SN74HCT32		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 µA	4.5 V	4.4	4.499		4.4		4.4		V
		I <sub>OH</sub> = -4 mA		3.98	4.3		3.7		3.84		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 µA	4.5 V		0.001	0.1		0.1		0.1	V
		I <sub>OL</sub> = 4 mA			0.17	0.26		0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		5.5 V			2		40		20	µA
ΔI <sub>CC</sub> <sup>†</sup>	One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>		5.5 V		1.4	2.4		3		2.9	mA
C <sub>i</sub>			4.5 V to 5.5 V		3	10		10		10	pF

<sup>†</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT32		SN74HCT32		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	4.5 V		15	24		35		30	ns
			5.5 V		13	22		32		27	
t <sub>t</sub>		Y	4.5 V		9	15		22		19	ns
			5.5 V		8	14		20		17	

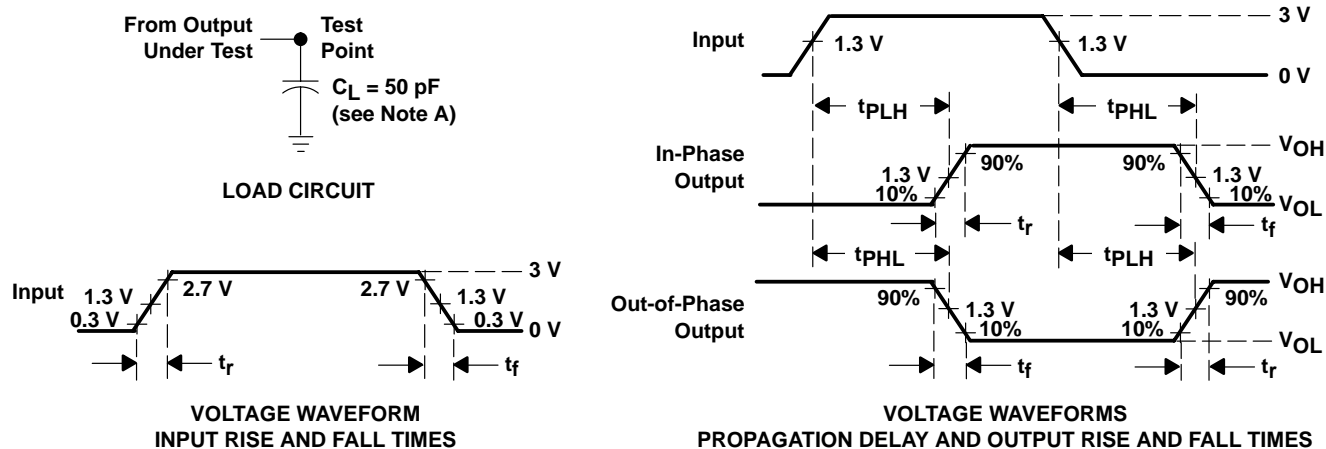
operating characteristics, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per gate	No load	20	pF

# SN54HCT32, SN74HCT32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

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## PARAMETER MEASUREMENT INFORMATION

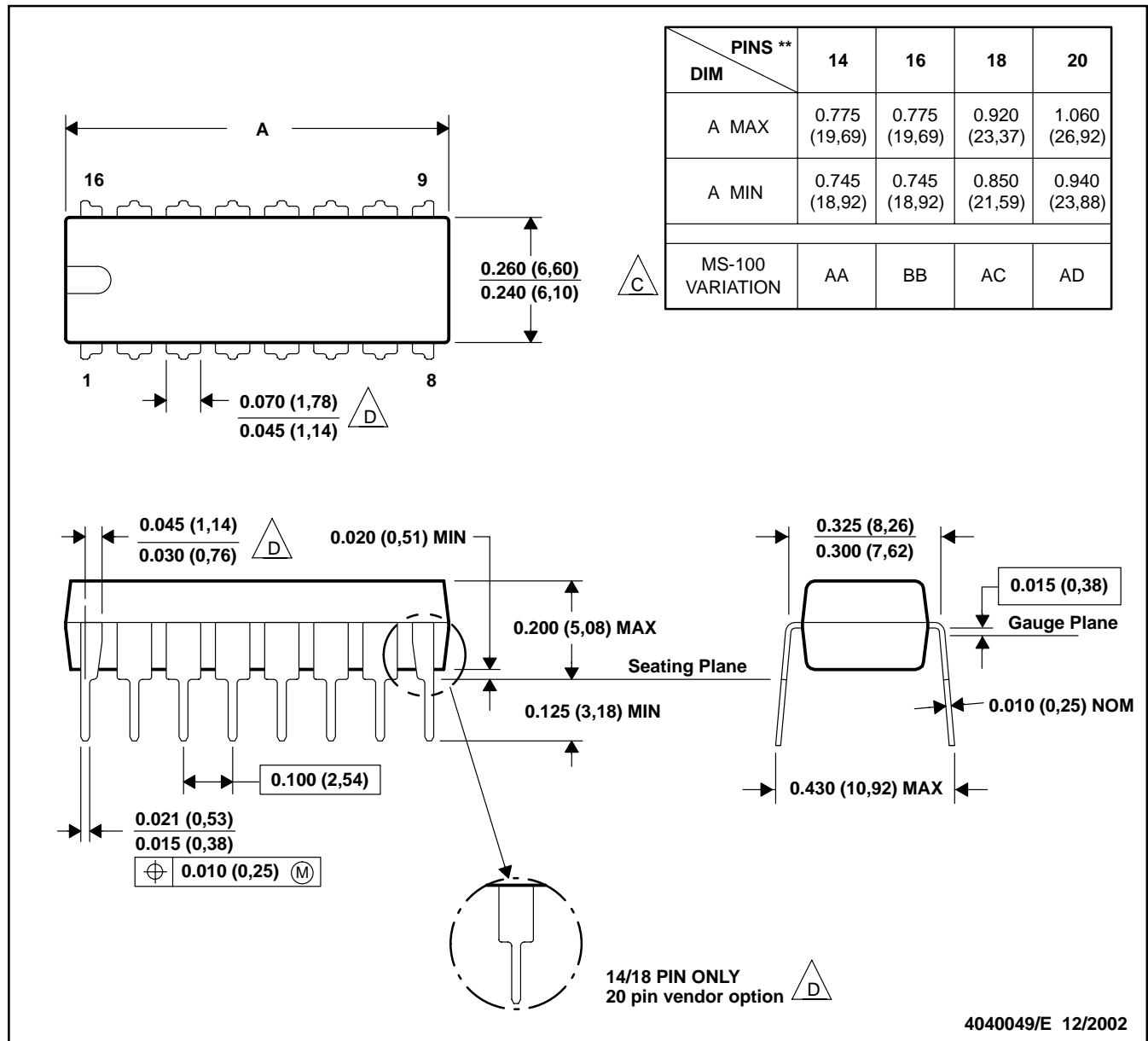


- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. The outputs are measured one at a time with one input transition per measurement.
  - D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

**N (R-PDIP-T\*\*)**

16 PINS SHOWN

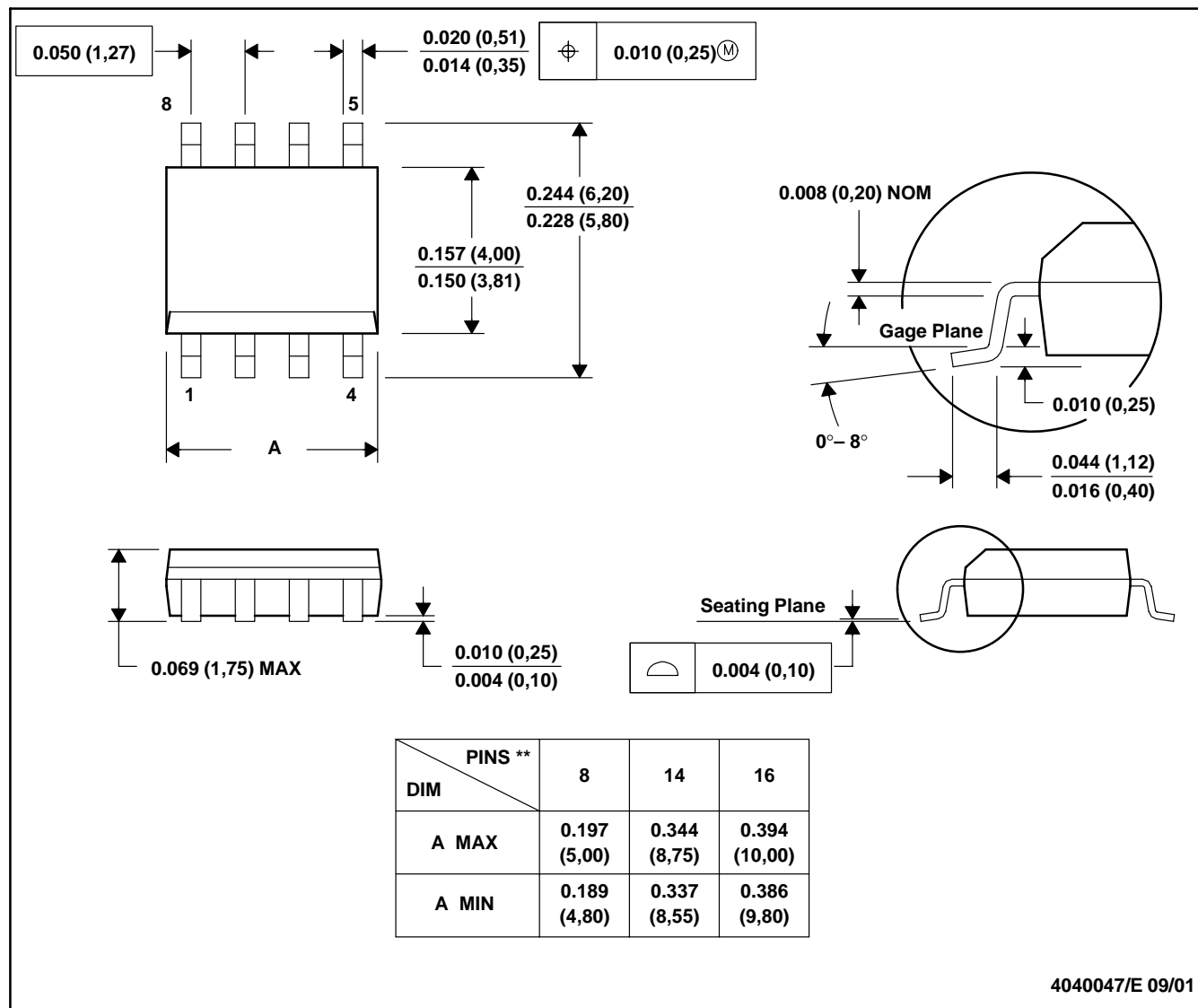
**PLASTIC DUAL-IN-LINE PACKAGE**

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

(C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

(D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

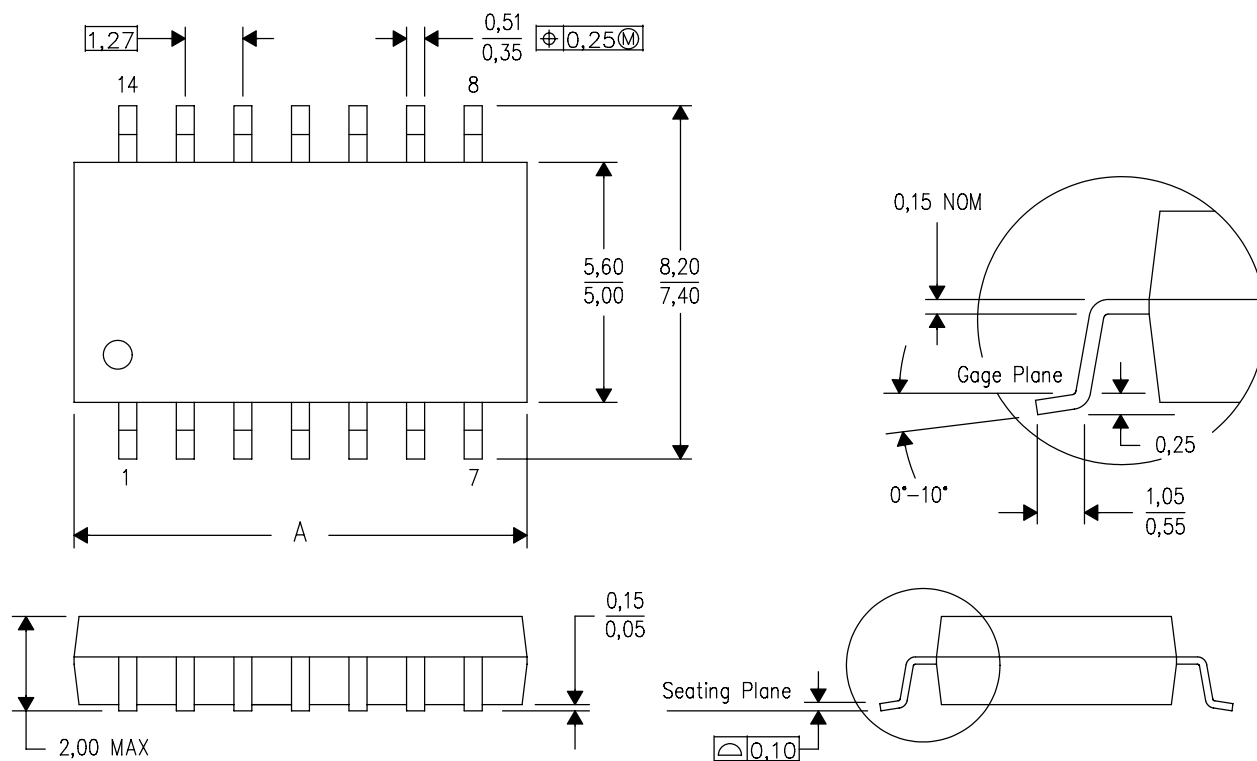
**D (R-PDSO-G\*\*)****PLASTIC SMALL-OUTLINE PACKAGE****8 PINS SHOWN**

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

NS (R-PDSO-G\*\*)

14-PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



PINS **	14	16	20	24
DIM				
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150



## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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