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P1 98.2

MOS FIELD EFFECT POWER TRANSISTOR

2SK1758

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

The 2SK1758 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 4.2 \Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 1 \text{ A}$)
- Low C_{iss} $C_{iss} = 360 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

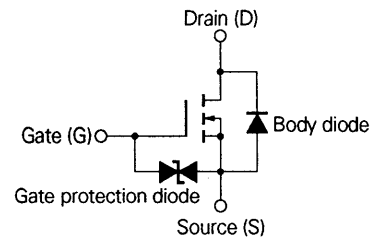
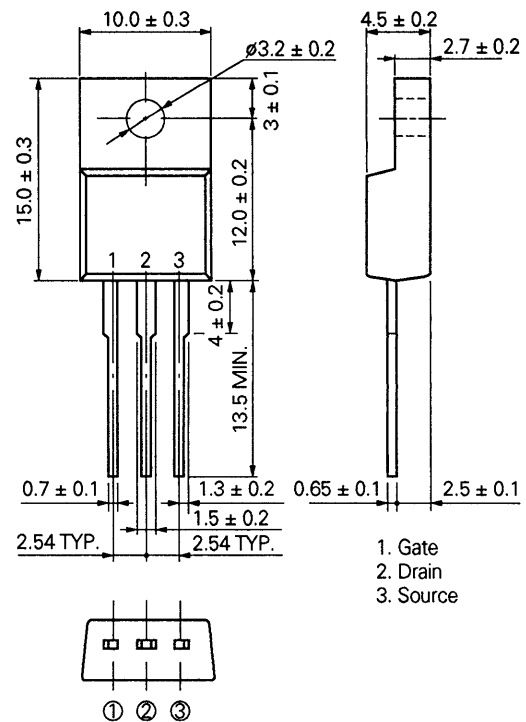
Drain to Source Voltage	V_{DSS}	600	V
Gate to Source Voltage	V_{GSS}	± 30	V
Drain Current (DC)	$I_{D(DC)}$	± 2.0	A
Drain Current (pulse)	$I_{D(pulse)}^*$	± 8.0	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_{T1}	30	W
Total Power Dissipation ($T_a = 25^\circ\text{C}$)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current	I_{AS}^{**}	3.0	A
Single Avalanche Energy	E_{AS}^{**}	96	mJ

* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

** Starting $T_{ch} = 25^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0$

PACKAGE DIMENSIONS

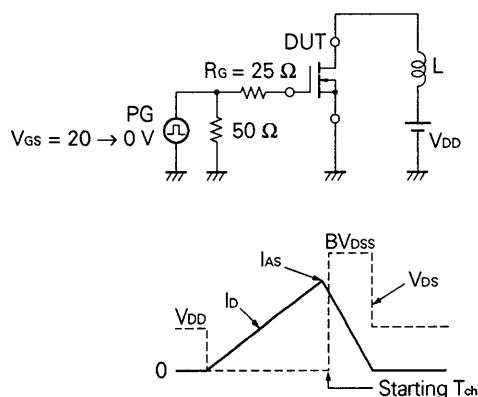
(in millimeters)



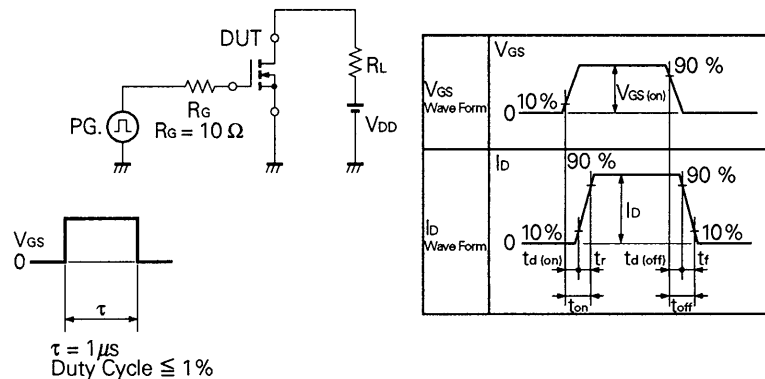
ELECTRICAL CHARACTERISTICS ($T_a = 25\text{ }^{\circ}\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		2.8	4.2	Ω	$V_{GS} = 10\text{ V}$, $I_D = 1\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.0		4.0	V	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	0.5	1.3		S	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ A}$
Drain Leakage Current	I_{DSS}			100	μA	$V_{DS} = 600\text{ V}$, $V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 30\text{ V}$, $V_{DS} = 0$
Input Capacitance	C_{iss}		360		pF	$V_{DS} = 10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$
Output Capacitance	C_{oss}		130		pF	
Reverse Transfer Capacitance	C_{res}		50		pF	
Turn-On Delay Time	$t_{d(on)}$		5		ns	$V_{GS(on)} = 10\text{ V}$ $V_{DD} = 150\text{ V}$ $I_D = 1\text{ A}$, $R_G = 10\text{ }\Omega$ $R_L = 150\text{ }\Omega$
Rise Time	t_r		6		ns	
Turn-Off Delay Time	$t_{d(off)}$		60		ns	
Fall Time	t_f		20		ns	
Total Gate Charge	Q_G		17		nC	$V_{GS} = 10\text{ V}$ $I_F = 2\text{ A}$ $V_{DD} = 400\text{ V}$
Gate to Source Charge	Q_{GS}		3		nC	
Gate to Drain Charge	Q_{GD}		10		nC	
Diode Forward Voltage	$V_{F(S-D)}$		0.85		V	$I_F = 2\text{ A}$, $V_{GS} = 0$
Reverse Recovery Time	t_{rr}		270		ns	$I_F = 2\text{ A}$, $V_{GS} = 0$ $di/dt = 50\text{ A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}		1.4		μC	

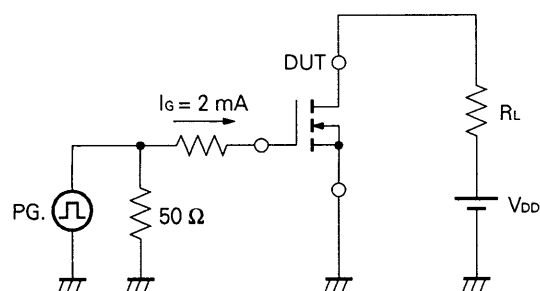
Test Circuit 1: Avalanche Capability



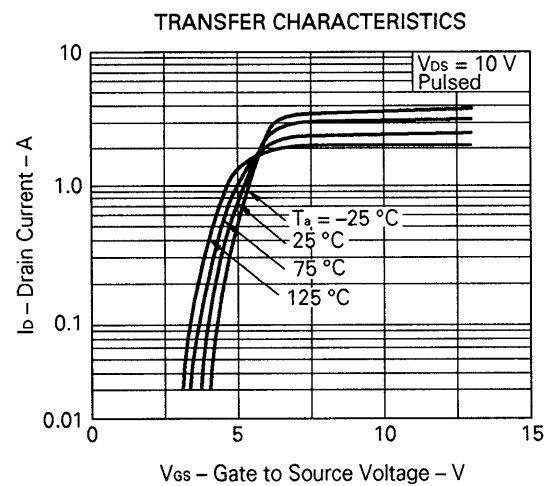
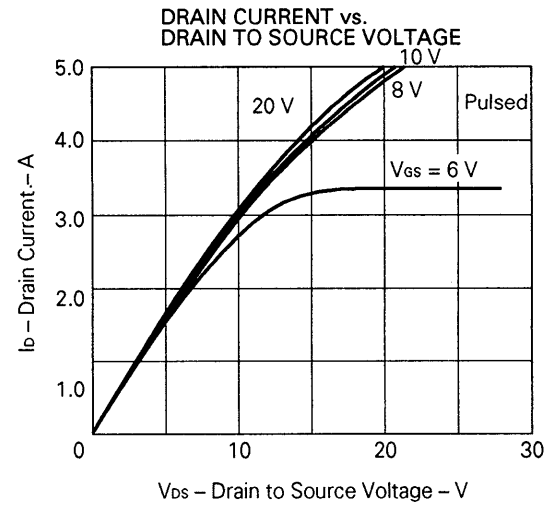
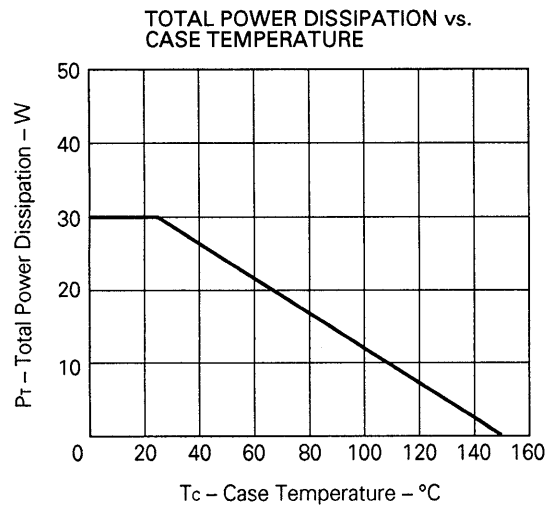
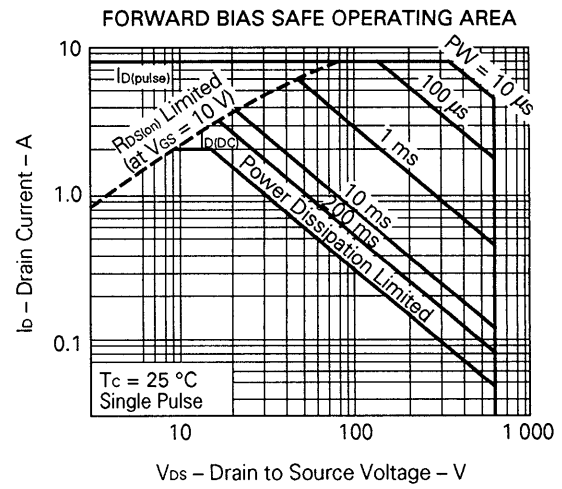
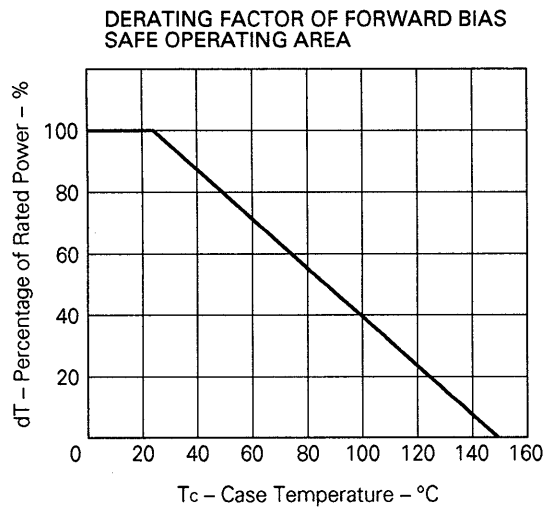
Test Circuit 2: Switching Time



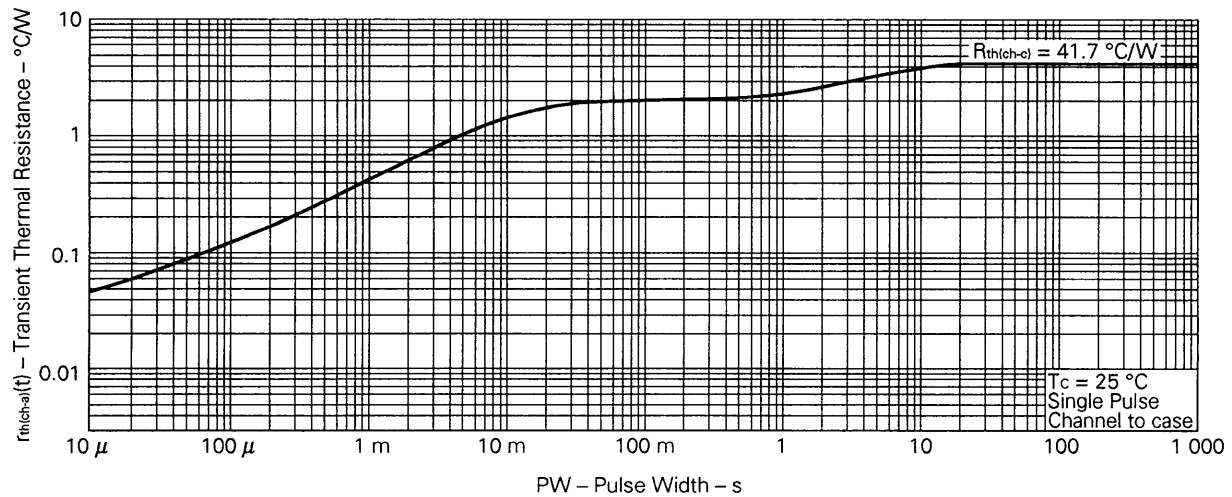
Test Circuit 3: Gate Charge



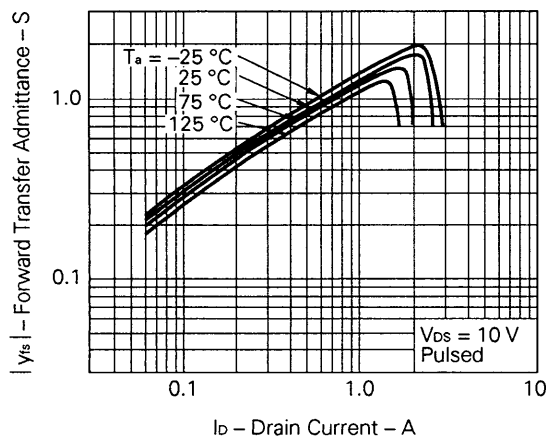
TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)



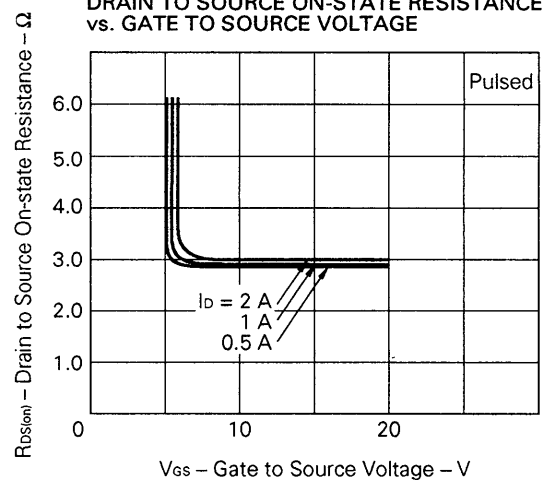
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



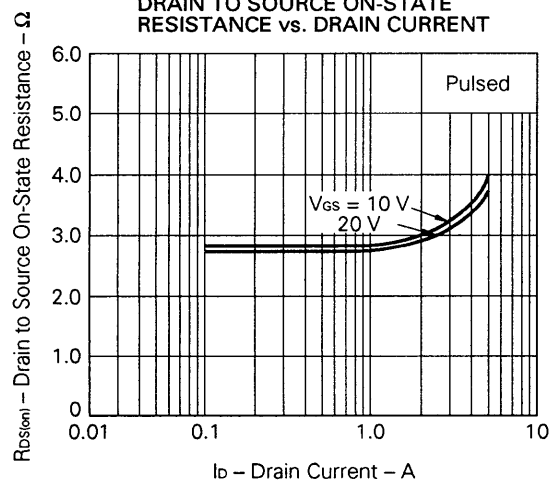
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



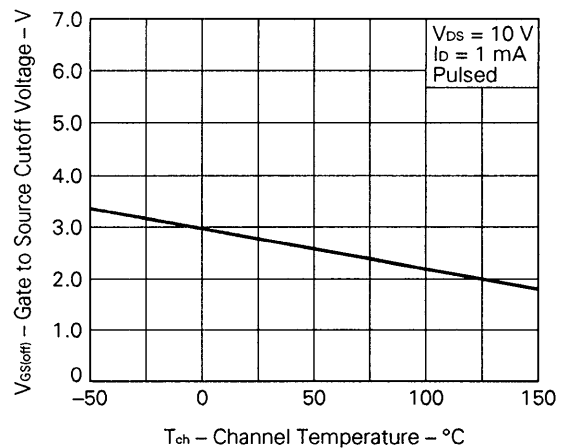
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

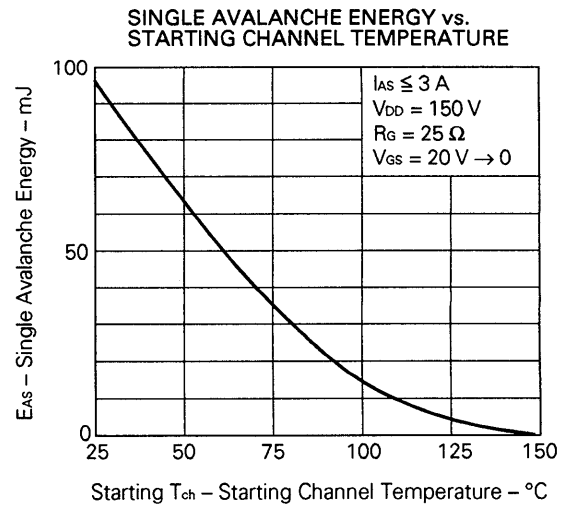
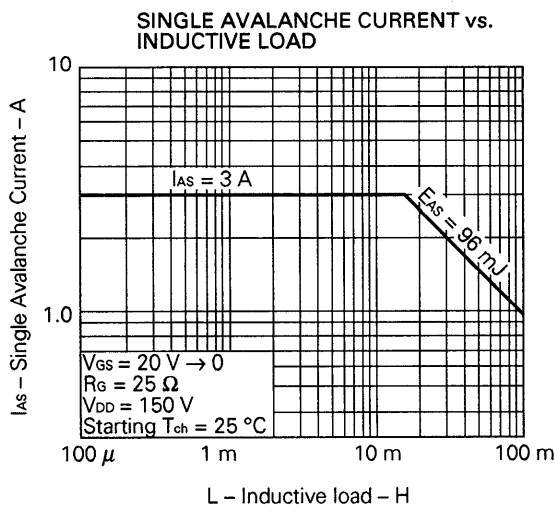
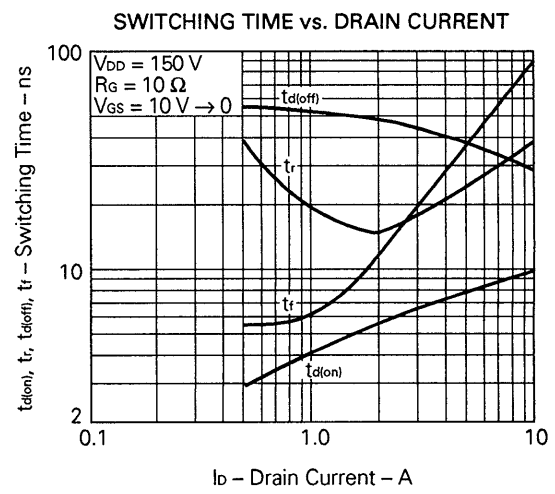
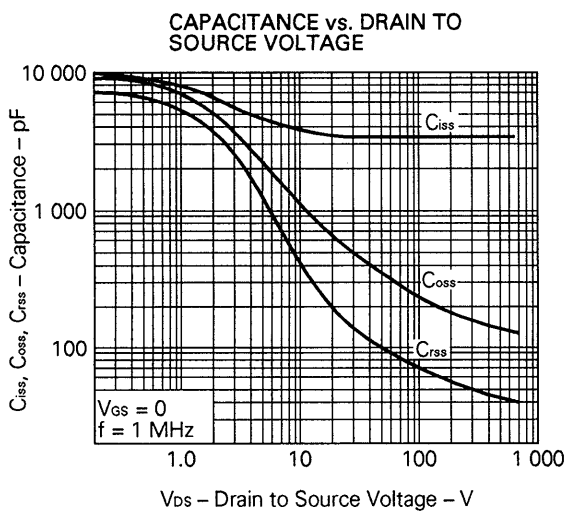
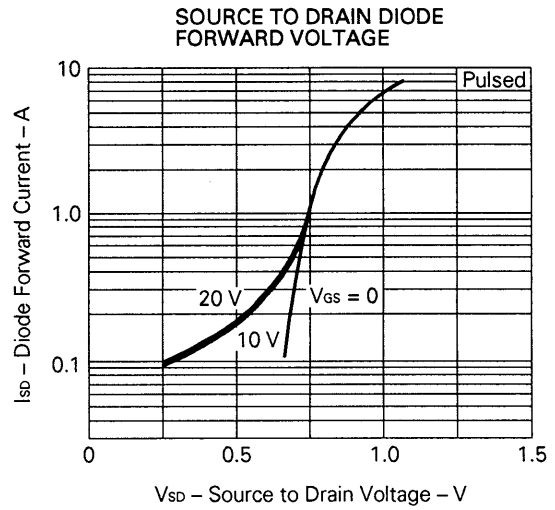
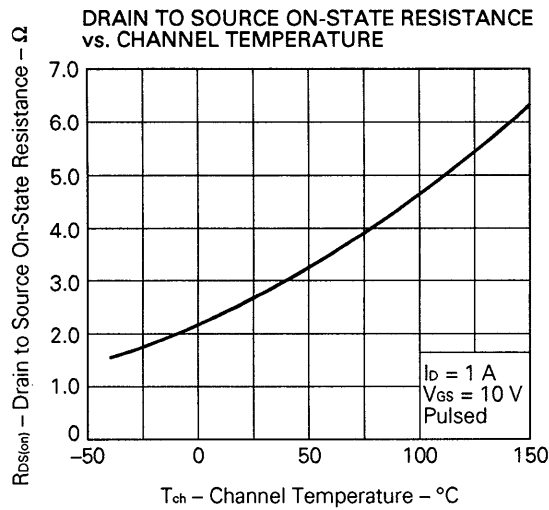


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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