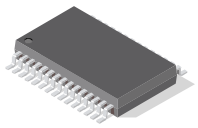



# CCD VERTICAL DRIVER FOR DIGITAL CAMERAS

## FEATURES

- **CCD Vertical Driver:**
  - **Three Field CCD Support**
  - **Two Field CCD Support**
- **Output Drivers:**
  - **3 Levels Driver (V-Transfer) x 5**
  - **2 Levels Driver (V-Transfer) x 3**
  - **2 Levels Driver (E-Shutter) x 1**
- **Drive Capability:**
  - **450 pF to 1890 pF With 60 Ω to 240 Ω**
- **Input Phase:**
  - **3 State (V-Transfer) x 5**
  - **2 State (V-Transfer) x 3**
  - **2 State (E-Shutter) x 1**
- **Portable Operation:**
  - **Input Interface: 2.7 V to 5.5 V**
- **Power Supply:**
  - **VDD 2.7 V to 5.5 V**
  - **VL –5 V to –9 V**
  - **VM GND**
  - **VH 11.5V to 15.5 V**

## APPLICATIONS

- **Digital Camera**
- **Video Camera**

## DESCRIPTION

The VSP1900 is a CCD vertical clock driver with electric-shutter support. This device is composed of eight vertical transfer channels, which support both 3-field CCD and 2-field CCD operation. The VSP1900 contributes low power consumption and parts number reduction in the system.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DESIGNATOR | OPERATING TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|
| VSP1900 | TSSOP30 | DBT | –25°C to 85°C | VSP1900 | VSP1900 | Tube (60 units/tube) |
| | | | | | | Tape and reel |

(1) For the most current specification and package information, refer to our web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | | UNITS |
|---|---|---|
| Supply voltage | VDD | GND –0.3 V to 7 V |
| | VL | GND to –10 V |
| | VH | VL + 26 V |
| Input voltage, $V_{IN}$ | | GND –0.3 V to (VDD + 0.3 V) |
| Ambient temperature under bias | | –25°C to 85°C |
| Storage temperature, $T_{stg}$ | | –55°C to 150°C |
| Junction temperature | | 150°C |
| Package temperature (IR reflow, peak) | | 235°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

free-air temperature range unless otherwise noted

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, VDD | 2.7 | | 5.5 | V |
| Supply voltage, VL | –5 | | –9 | V |
| Supply voltage, VH | 11.5 | | 15.5 | V |
| Input voltage, VIN | GND – 0.3 to (VDD + 0.3) | | | V |

## TRUTH TABLE

| INPUT | | | | OUTPUT | | |
|---|---|---|---|---|---|---|
| V1N<br>V3AN<br>V3BN<br>V5AN<br>V5BN | CH1N<br>CH2N<br>CH3N<br>CH4N<br>CH5N | V2N<br>V4N<br>V6N | SUBN | V1<br>V3A<br>V3B<br>V5A<br>V5B | V2<br>V4<br>V6 | SUB |
| L | L | X | X | VH | X | X |
| L | H | X | X | VM | X | X |
| H | L | X | X | Z | X | X |
| H | H | X | X | VL | X | X |
| X | X | L | X | X | VM | X |
| X | X | H | X | X | VL | X |
| X | X | X | L | X | X | VH |
| X | X | X | H | X | X | VL |

NOTE: Z = High impedance X = Don't care

## ELECTRICAL CHARACTERISTICS

all specifications at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | DC power consumption | | | 5.3 | | mW |
| | Switching power consumption | VSP2267 (TG) with loading diagram | | 550 | | mW |
| **DC CHARACTERISTICS** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.7VDD | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.2VDD | V |
| $I_{IN}$ | Input current | $V_{IN}$ = GND to 5 V (without pullup / pulldown resistor) | –10 | 0 | 10 | µA |
| | | $V_{IN}$ = GND to 5 V (pullup / pulldown resistor) | –625 | 0 | 625 | |
| $I_H$ | Operating supply current | | | 0.1 | 0.2 | mA |
| $I_{DD}$ | | | | 1 | | |
| $I_L$ | | | | 0.125 | | |
| $I_{OL}$ | Output current | V1, V2, V3A, V3B, V4, V5A, V5B, V6 = –8.1 V | 10 | | | mA |
| $I_{OM1}$ | | V1, V2, V3A, V3B, V4, V5A, V5B, V6 = –0.2 V | | | –5 | |
| $I_{OM2}$ | | V1, V3A, V3B, V5A, V5B = 0.2 V | 5 | | | |
| $I_{OH}$ | | V1, V3A, V3B, V5A, V5B = 14.55 V | | | –7.2 | |
| $I_{OSL}$ | | SUB = –8.1 V | 5.4 | | | |
| $I_{OSH}$ | | SUB = 14.55 V | | | –4 | |

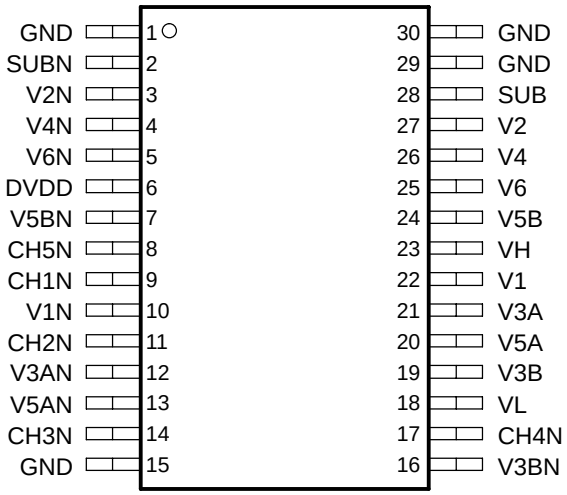
## SWITCHING CHARACTERISTICS

all specifications at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{d(PLM)}$ | Propagation delay time | | | 15 | 100 | ns |
| $t_{d(PMH)}$ | | | | 20 | 100 | |
| $t_{d(PLH)}$ | | | | 20 | 100 | |
| $t_{d(PML)}$ | | | | 15 | 50 | |
| $t_{d(PHM)}$ | | | | 30 | 50 | |
| $t_{d(PHL)}$ | | | | 30 | 50 | |
| $t_{r(TLM)}$ | Rise time | VL → VM | | | 300 | ns |
| $t_{r(TMH)}$ | | VM → VH | | | 300 | |
| $t_{r(TLH)}$ | | VL → VH | | | 300 | |
| $t_{f(TML)}$ | Fall time | VM → VL | | | 300 | ns |
| $t_{f(THM)}$ | | VH → VM | | | 300 | |
| $t_{f(THL)}$ | | VH → VL | | | 300 | |
| $V_{n(CLH)}$ | Output noise voltage | | | | | V |
| $V_{n(CLL)}$ | | | | | | |
| $V_{n(CMH)}$ | | | | | 2 | |
| $V_{n(CML)}$ | | | | | | |
| $V_{n(CHL)}$ | | | | | | |

## PIN ASSIGNMENTS

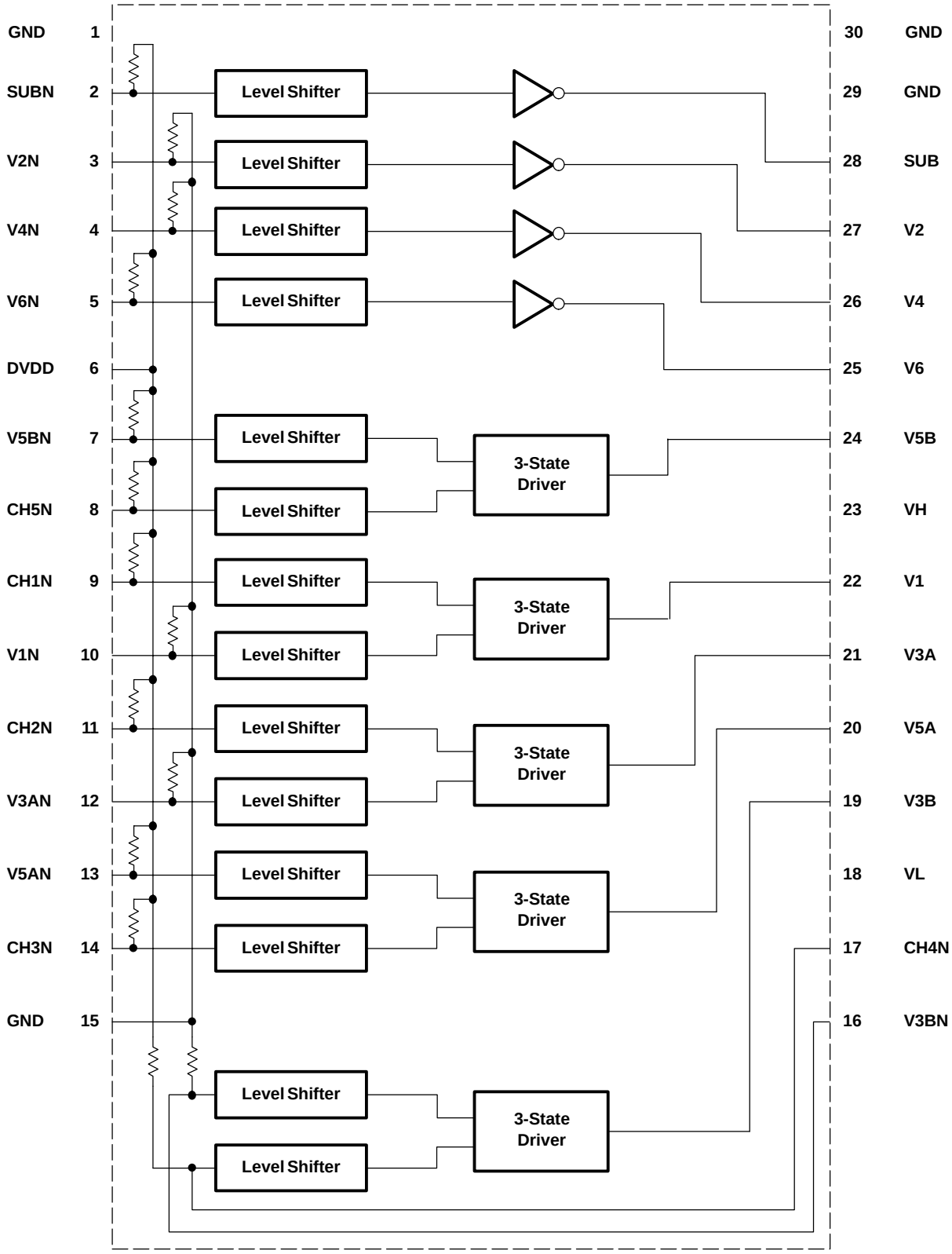
**DBT PACKAGE**
**(TOP VIEW)**



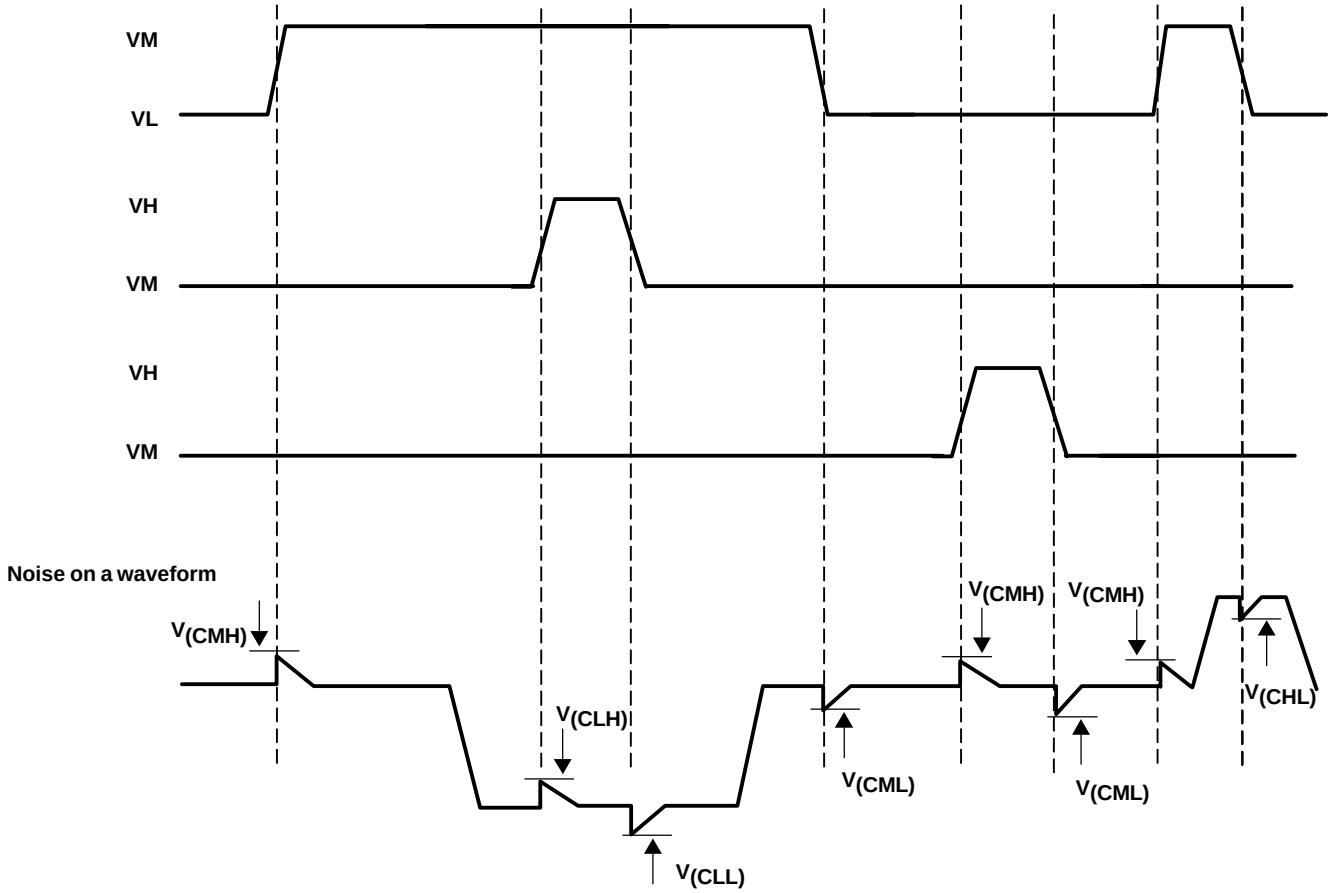

### Terminal Functions

| TERMINAL NAME | TERMINAL NO. | TYPE | DESCRIPTIONS |
|---|---|---|---|
| GND | 1 | P | Ground |
| SUBN | 2 | DI | CCD substrate clock SUB input |
| V2N | 3 | DI | Vertical transfer clock 2 input |
| V4N | 4 | DI | Vertical transfer clock 4 input |
| V6N | 5 | DI | Vertical transfer clock 6 input |
| DVDD | 6 | P | Digital power supply |
| V5BN | 7 | DI | Vertical transfer clock 5B input |
| CH5N | 8 | DI | Read out clock 5 input |
| CH1N | 9 | DI | Read out clock 1 input |
| V1N | 10 | DI | Vertical transfer clock 1 input |
| CH2N | 11 | DI | Read out clock 2 input |
| V3AN | 12 | DI | Vertical transfer clock 3A input |
| V5AN | 13 | DI | Vertical transfer clock 5A input |
| CH3N | 14 | DI | Read out clock 3 input |
| GND | 15 | P | Ground |
| V3BN | 16 | DI | Vertical transfer clock 3B input |
| CH4N | 17 | DI | Read out clock 4 input |
| VL | 18 | P | Digital power supply |
| V3B | 19 | DO | Vertical transfer clock 3B output |
| V5A | 20 | DO | Vertical transfer clock 5A output |
| V3A | 21 | DO | Vertical transfer clock 3A output |
| V1 | 22 | DO | Vertical transfer clock 1 output |
| VH | 23 | P | Digital power supply |
| V5B | 24 | DO | Vertical transfer clock 5B output |
| V6 | 25 | DO | Vertical transfer clock 6 output |
| V4 | 26 | DO | Vertical transfer clock 4 output |
| V2 | 27 | DO | Vertical transfer clock 2 output |
| SUB | 28 | DO | CCD substrate clock SUB output |
| GND | 29 | P | Ground |
| GND | 30 | P | Ground |

## FUNCTIONAL BLOCK DIAGRAM



## SWITCHING WAVEFORM



## LOADING DIAGRAM

| | | |
|---|---|---|
| Vertical clock series resistor | R1, R2, R4, R6 | 60 Ω |
| | R3A, R5A | 240 Ω |
| | R3B, R5B | 80 Ω |
| Vertical clock to GND | CΦV1 | 1280 pF |
| | CΦV3A, CΦV3B | 640 pF |
| | CΦV5A, CΦV5B | 640 pF |
| | CΦV2, CΦV4, CΦV6 | 400 pF |
| Between vertical clock | CΦV12 | 510 pF |
| | CΦV23A, CΦV23B | 50 pF |
| | CΦV45A, CΦV45B | 50 pF |
| | CΦV3A4, CΦV3B4 | 260 pF |
| | CΦV5A6, CΦV5B6 | 260 pF |
| | CΦV61 | 100 pF |
| Substrate clock to GND | CΦVSUB | 1000 pF |
| Vertical clock GND resistor | R GND | 18 Ω |

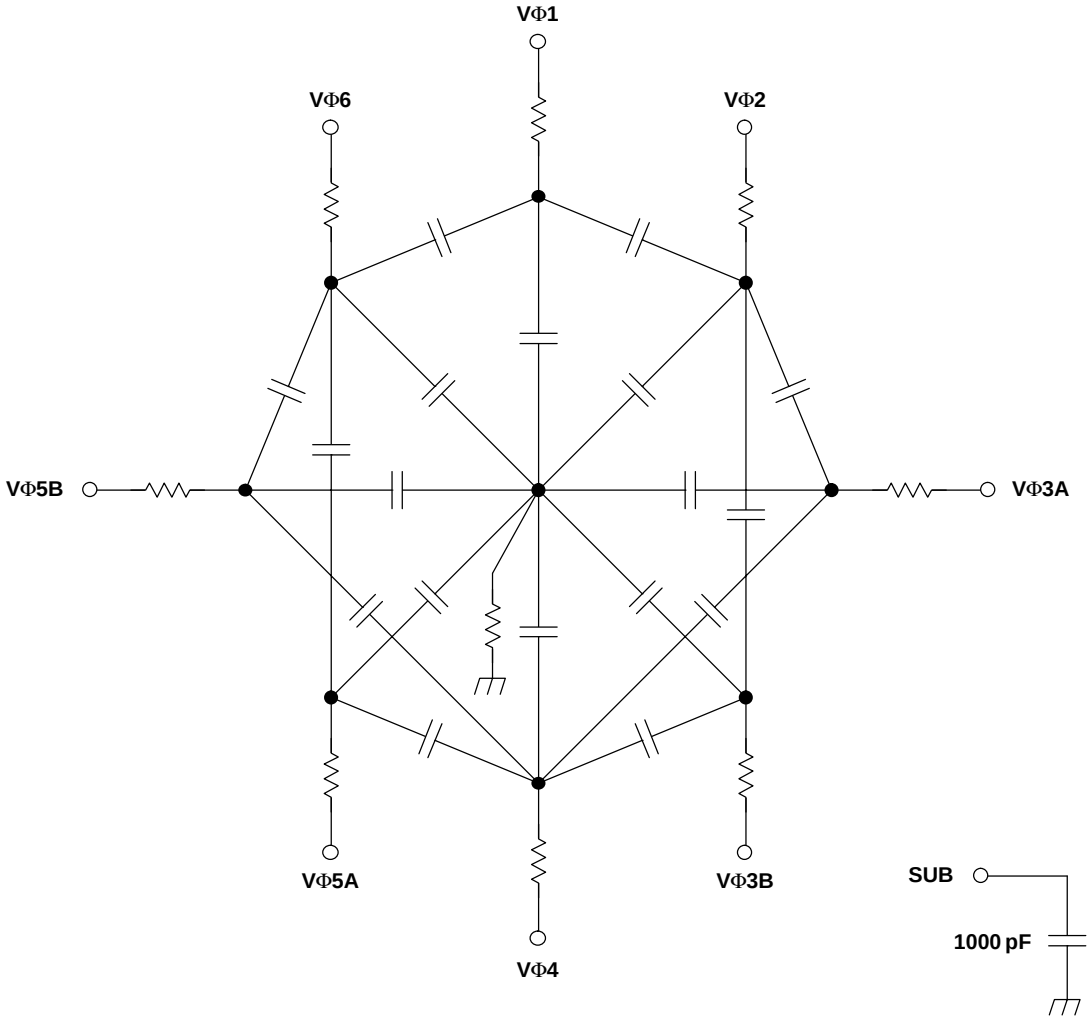



**Figure 1. VSP1900 Loading Diagram**

## DESCRIPTION

The VSP1900 is a CCD vertical clock driver with electric shutter. The VSP1900 is composed of five 3-state and three 2-state vertical transfer channels, which support both 3 field and 2 field CCD operation. The VSP1900 contributes low power consumption and parts number reduction in the system.

## OPERATION

### Power On/Off Sequence

This is the same as the CCD power up sequence, when power on, VDD powers on first VH, VM power on second, and VL powers on later. When powering off, VL powers off first, VH, VM power of second, and VDD powers off later.

### Vertical Transfer Signal

The VSP1900 receives signals from TG (CCD timing generator). The input signal is converted into CCD operation voltage level by the level shifter. The level shifter circuits connect to a 2-state or 3-state driver, which is connected to the CCD input pin. While using a 2-field CCD, one of the 3-state drivers is used as a 2-state driver. The CH#N pin is pulled up internally, so that the VH level does not appear on the output pin.

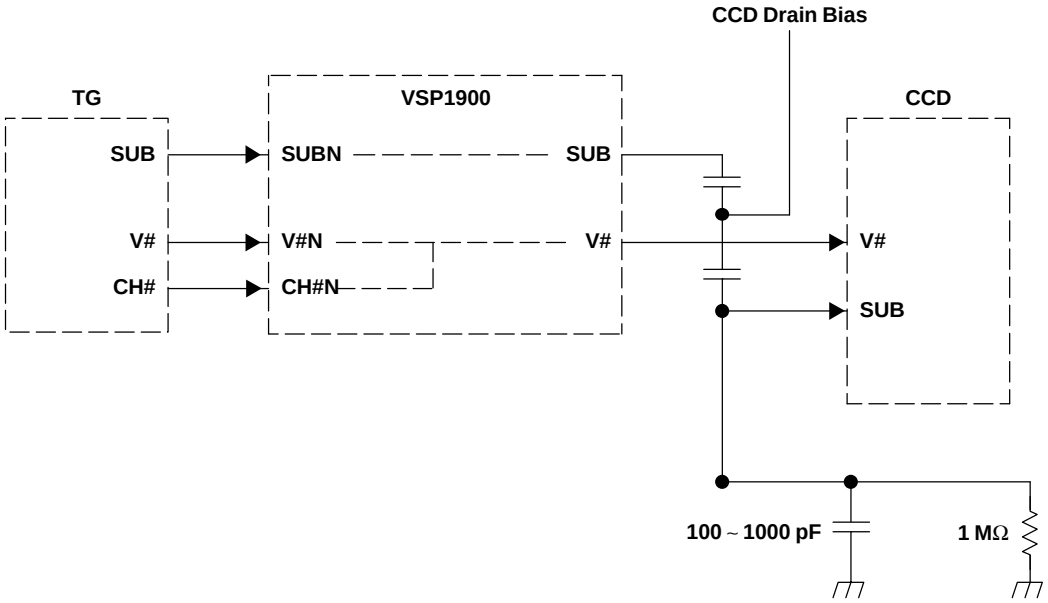
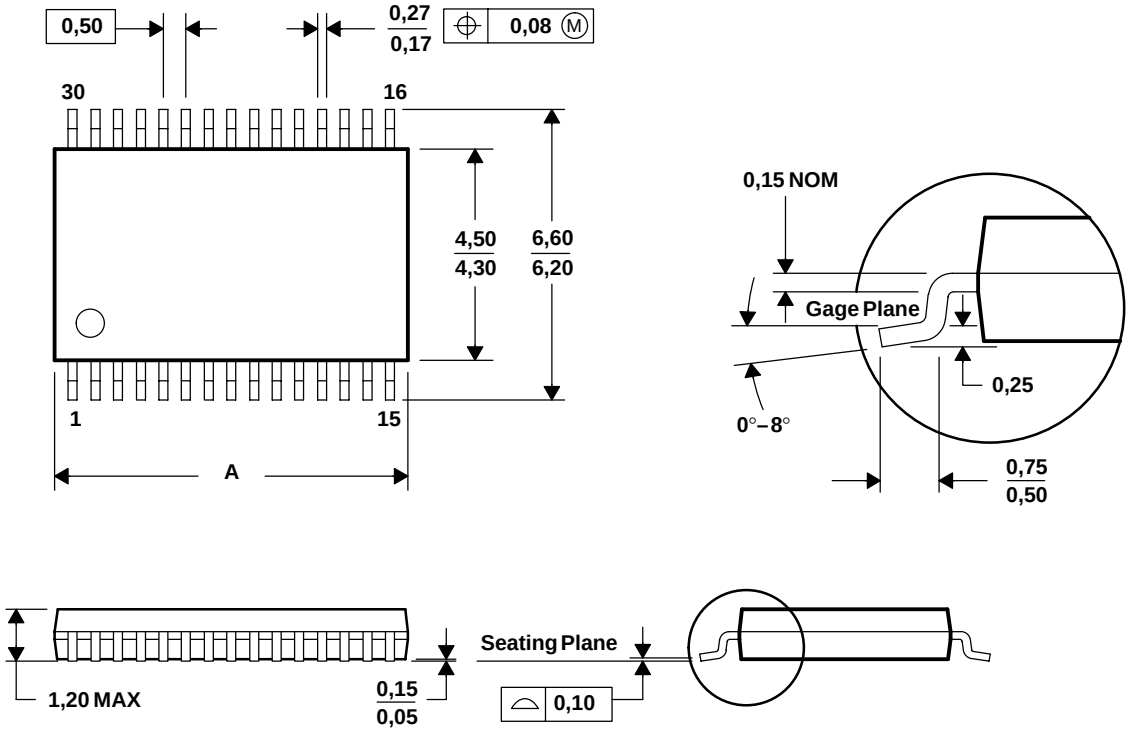



**Figure 2. FVSP1900 Circuit Application**

## MECHANICAL DATA

**DBT (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**30 PINS SHOWN**




| DIM \ PINS ** | 20 | 24 | 28 | 30 | 38 | 44 | 50 |
|---|---|---|---|---|---|---|---|
| A MAX | 5,10 | 6,60 | 7,90 | 7,90 | 9,80 | 11,10 | 12,60 |
| A MIN | 4.90 | 6,40 | 7,70 | 7,70 | 9,60 | 10,90 | 12,40 |

**4073252/E 02/02**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153

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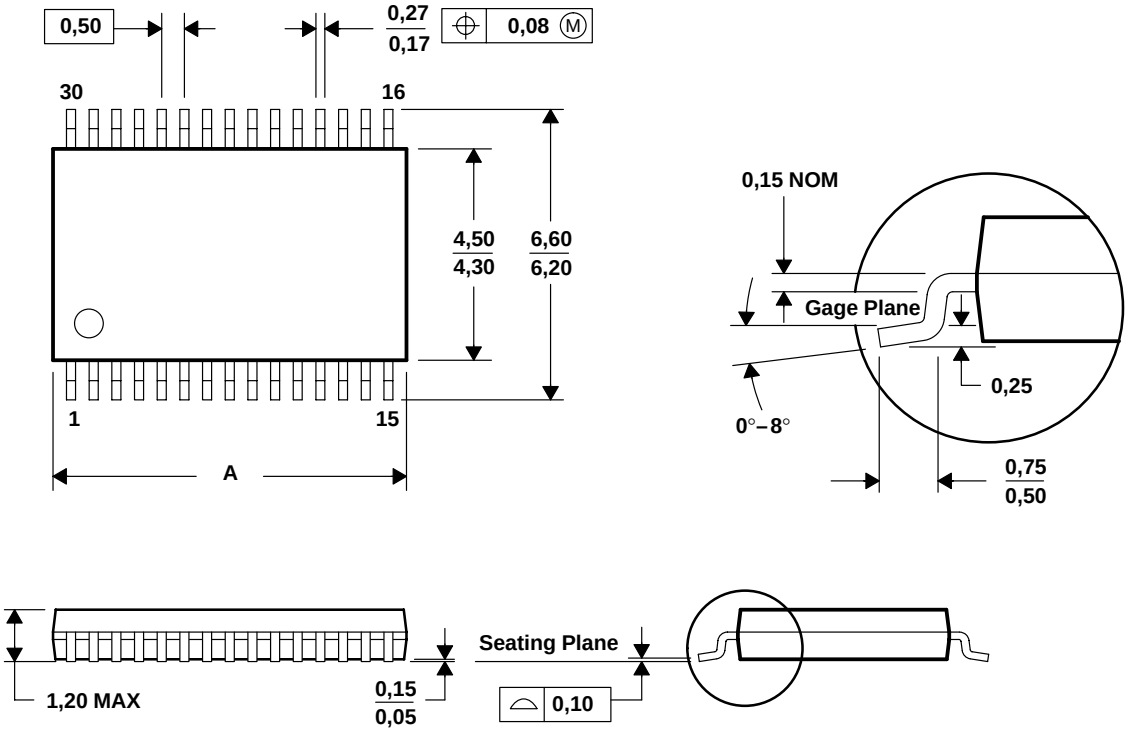
**DBT (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**30 PINS SHOWN**




| DIM \ PINS ** | 20 | 24 | 28 | 30 | 38 | 44 | 50 |
|---|---|---|---|---|---|---|---|
| A MAX | 5,10 | 6,60 | 7,90 | 7,90 | 9,80 | 11,10 | 12,60 |
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