XC9500 In-System Programmable CPLD Automotive IQ Family

DS120-1 (v1.2) October 18, 2004

Product Specification

Features

- System frequency up to 55 MHz
- Guaranteed to meet full electrical specifications over T_A = –40 to +125°C
- 5V in-system programmable
  - Endurance of 10,000 program/erase cycles
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
  - Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
  - Programmable power reduction mode in each macrocell
  - Slew rate control on individual outputs
  - User programmable ground pin capability
  - Extended pattern security features for design protection
  - High-drive 24 mA outputs
  - 3.3V or 5V I/O capability
  - CMOS 5V Fast FLASH™ technology
  - Supports parallel programming of multiple XC9500 devices
- Refer to XC9500 Family data sheet [September 15, 1999 (version 5.0)] for architecture description
- Refer to XC9536 data sheet [December 4, 1998 (version 5.0)] and XC9572XL data sheet [December 4, 1998 (version 3.0)] for pin tables

Family Overview

The XC9500 CPLD Automotive IQ family provides advanced in-system programming and test capabilities for high performance, general purpose logic integration. All devices are in-system programmable for a minimum of 10,000 program/erase cycles. Extensive IEEE 1149.1 (JTAG) boundary-scan support is also included on all family members.

As shown in Table 1, logic density of the XC9500 devices ranges from 800 to 1,600 usable gates with 36 and 72 registers, respectively. Multiple package options and associated I/O capacity are shown in Table 2. The XC9500 family is fully pin-compatible allowing easy design migration across multiple density options in a given package footprint.

The XC9500 architectural features address the requirements of in-system programmability. Enhanced pin-locking capability avoids costly board rework. An expanded JTAG instruction set allows version control of programming patterns and in-system debugging. In-system programming throughout the full device operating range and a minimum of 10,000 program/erase cycles provide worry-free reconfigurations and system field upgrades.

Advanced system features include output slew rate control and user-programmable ground pins to help reduce system noise. I/Os may be configured for 3.3V or 5V operation. All outputs provide 24 mA drive.

Table 1: **XC9500 Device Automotive Family**

	XC9536	XC9572
Macrocells	36	72
Usable Gates	800	1,600
Registers	36	72
T_{PD} (ns)	5	7.5
T_{SU} (ns)	3.5	4.5
T_{CO} (ns)	4.0	4.5
f_{CNT} (MHz)(1)	100	125
f_{SYSTEM} (MHz)(2)	100	83.3

Notes:
1. f_{CNT} = Operating frequency for 16-bit counters.
2. f_{SYSTEM} = Internal operating frequency for general purpose system designs spanning multiple FBs.

Table 2: **Available Packages and Device I/O Pins (not including dedicated JTAG pins)**

	XC9536	XC9572
44-Pin VQFP	34	-
100-Pin TQFP	-	72

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to 7.0	V
V_{IN}	Input voltage relative to GND	–0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} + 0.5	V
T_J	Junction temperature	+150	°C
T_A	Operating temperature	–40°C to +125°C	°C
T_{STG}	Storage temperature (ambient)	–65 to +150	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operation Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffers	4.5	5.5	V
V_{CCIO}	Supply voltage for output drivers for 5V operation	4.5	5.5	V
	Supply voltage for output drivers for 3.3V operation	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	V_{CCINT} + 0.5	V
V_O	Output voltage	0	V_{CCIO}	V

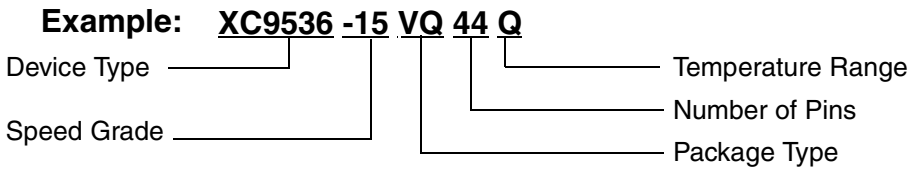
Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
T_{DR}	Data Retention	20	-	Years
N_{PE}	Program/Erase Cycles (Endurance)	10,000	-	Cycles

DC Characteristic Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{OH}	Output high voltage for 5V outputs	I_{OH} = –4.0 mA, V_{CC} = Min		2.4	-	V
	Output high voltage for 3.3V outputs	I_{OH} = –3.2 mA, V_{CC} = Min		2.4	-	V
V_{OL}	Output low voltage for 5V outputs	I_{OL} = 24 mA, V_{CC} = Min		-	0.5	V
	Output low voltage for 3.3V outputs	I_{OL} = 10 mA, V_{CC} = Min		-	0.4	V
I_{IL}	Input leakage current	V_{CC} = Max. V_{IN} = GND or V_{CC}		-	±10	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max, V_{IN} = GND or V_{CC}		-	±10	µA
C_{IN}	I/O capacitance	V_{IN} = GND, f = 1.0 MHz		-	10	pF
I_{CC}	Operating supply current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	XC9536	30 (Typical)		mA
			XC9572	65 (Typical)		

Ordering Information



Device Ordering Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range(1)
XC9536-15VQ44Q	15 ns	VQ44	44-pin	Thin Quad Flat Pack (VQFP)	Q
XC9572-15TQ100Q	15 ns	TQ100	100-pin	Very Thin Quad Flat Pack (TQFP)	Q

Notes:
1. Q = Automotive: T_A = –40° to +125°C

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
1.0	11/26/02	Initial Xilinx release.
1.1	02/03/03	Added reference to XC9500, XC9536, and XC9572 data sheets.
1.2	10/18/04	Added "Not to be used in new designs" watermark; moved to "Mature Products"