# DATA SHEET

# 74LVC2G07
## Buffers with open-drain outputs

Product specification
Supersedes data of 2004 Mar 19

2004 Sep 08

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# Buffers with open-drain outputs 74LVC2G07

## FEATURES

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V).
- –24 mA output drive ($V_{CC}$ = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

## DESCRIPTION

The 74LVC2G07 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

Input can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

Schmitt trigger action at all inputs makes the circuit tolerant for slower input rise and fall time.

This device is fully specified for partial power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC2G07 provides two non-inverting buffers.

The output of the device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PLZ}/t_{PZL}$ | propagation delay input nA to output nY | $V_{CC}$ = 1.8 V; $C_L$ = 30 pF; $R_L$ = 1 kΩ | 3.5 | ns |
| | | $V_{CC}$ = 2.5 V; $C_L$ = 30 pF; $R_L$ = 500 Ω | 2.4 | ns |
| | | $V_{CC}$ = 2.7 V; $C_L$ = 50 pF; $R_L$ = 500 Ω | 2.3 | ns |
| | | $V_{CC}$ = 3.3 V; $C_L$ = 50 pF; $R_L$ = 500 Ω | 2.6 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 50 pF; $R_L$ = 500 Ω | 1.5 | ns |
| $C_I$ | input capacitance | | 2.5 | pF |
| $C_{PD}$ | power dissipation capacitance per gate | $V_{CC}$ = 3.3 V; notes 1 and 2 | 6.5 | pF |

**Notes**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
   $f_i$ = input frequency in MHz;
   $f_o$ = output frequency in MHz;
   $C_L$ = output load capacitance in pF;
   $V_{CC}$ = supply voltage in Volts;
   N = total load switching outputs;
   $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is $V_I$ = GND to $V_{CC}$.

## FUNCTION TABLE

See note 1.

| INPUT | OUTPUT |
|---|---|
| **nA** | **nY** |
| L | L |
| H | Z |

**Note**

1. H = HIGH voltage level;
   L = LOW voltage level;
   Z = high-impedance OFF-state.

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | | | | |
|---|---|---|---|---|---|---|
| | TEMPERATURE RANGE | PINS | PACKAGE | MATERIAL | CODE | MARKING |
| 74LVC2G07GW | –40 °C to +125 °C | 6 | SC-88 | plastic | SOT363 | V7 |
| 74LVC2G07GV | –40 °C to +125 °C | 6 | SC-74 | plastic | SOT457 | V07 |
| 74LVC2G07GM | –40 °C to +125 °C | 6 | XSON6 | plastic | SOT886 | V7 |

## PINNING

| PIN | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | 1A | data input |
| 2 | GND | ground (0 V) |
| 3 | 2A | data input |
| 4 | 2Y | data output |
| 5 | $V_{CC}$ | supply voltage |
| 6 | 1Y | data output |

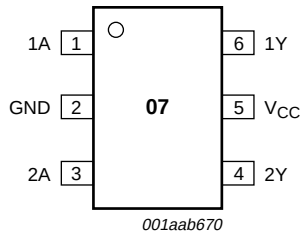
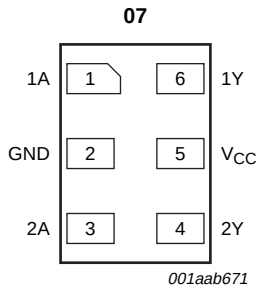



Fig.1 Pin configuration SC-88 and SC-74.




Transparent top view

Fig.2 Pin configuration XSON6.

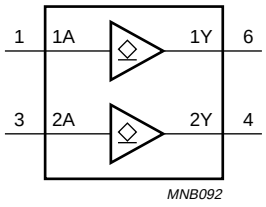



Fig.3 Logic symbol.

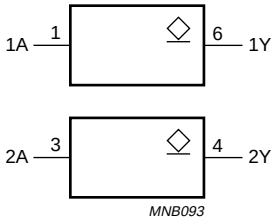



Fig.4 IEEE/IEC logic symbol.

**RECOMMENDED OPERATING CONDITIONS**

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 1.65 | 5.5 | V |
| $V_I$ | input voltage | | 0 | 5.5 | V |
| $V_O$ | output voltage | active mode | 0 | $V_{CC}$ | V |
| | | $V_{CC}$ = 0 V; Power-down mode | 0 | 5.5 | V |
| $T_{amb}$ | operating ambient temperature | | –40 | +125 | °C |
| $t_r$, $t_f$ | input rise and fall times | $V_{CC}$ = 1.65 V to 2.7 V | 0 | 20 | ns/V |
| | | $V_{CC}$ = 2.7 V to 5.5 V | 0 | 10 | ns/V |

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | –0.5 | +6.5 | V |
| $I_{IK}$ | input diode current | $V_I$ < 0 V | – | –50 | mA |
| $V_I$ | input voltage | note 1 | –0.5 | +6.5 | V |
| $I_{OK}$ | output diode current | $V_O$ < 0 V | – | –50 | mA |
| $V_O$ | output voltage | active mode; notes 1 and 2 | –0.5 | +6.5 | V |
| | | Power-down mode; notes 1 and 2 | –0.5 | +6.5 | V |
| $I_O$ | output source or sink current | $V_O$ = 0 V to 6.5 V | – | 50 | mA |
| $I_{CC}$, $I_{GND}$ | $V_{CC}$ or GND current | | – | ±100 | mA |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $P_{tot}$ | power dissipation | $T_{amb}$ = –40 °C to +125 °C | – | 300 | mW |

**Notes**

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When $V_{CC}$ = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

**DC CHARACTERISTICS**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| | | OTHER | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = −40 °C to +85 °C**; note 1 | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 1.65 to 1.95 | $0.65 \times V_{CC}$ | – | – | V |
| | | | 2.3 to 2.7 | 1.7 | – | – | V |
| | | | 2.7 to 3.6 | 2.0 | – | – | V |
| | | | 4.5 to 5.5 | $0.7 \times V_{CC}$ | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | 1.65 to 1.95 | – | – | $0.35 \times V_{CC}$ | V |
| | | | 2.3 to 2.7 | – | – | 0.7 | V |
| | | | 2.7 to 3.6 | – | – | 0.8 | V |
| | | | 4.5 to 5.5 | – | – | $0.3 \times V_{CC}$ | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = 100 μA | 1.65 to 5.5 | – | – | 0.1 | V |
| | | $I_O$ = 4 mA | 1.65 | – | – | 0.45 | V |
| | | $I_O$ = 8 mA | 2.3 | – | – | 0.3 | V |
| | | $I_O$ = 12 mA | 2.7 | – | – | 0.4 | V |
| | | $I_O$ = 24 mA | 3.0 | – | – | 0.55 | V |
| | | $I_O$ = 32 mA | 4.5 | – | – | 0.55 | V |
| $I_{LI}$ | input leakage current | $V_I$ = 5.5 V or GND | 1.65 to 5.5 | – | ±0.1 | ±5 | μA |
| $I_{OZ}$ | output OFF-state current | $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND | 5.5 | – | ±0.1 | ±10 | μA |
| $I_{off}$ | power OFF leakage current | $V_I$ or $V_O$ = 5.5 V | 0 | – | ±0.1 | ±10 | μA |
| $I_{CC}$ | quiescent supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A | 5.5 | – | 0.1 | 10 | μA |
| $\Delta I_{CC}$ | additional quiescent supply current per pin | $V_I = V_{CC}$ − 0.6 V; $I_O$ = 0 A | 2.3 to 5.5 | – | 5 | 500 | μA |

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| | | OTHER | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = −40 °C to +125 °C** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 1.65 to 1.95 | $0.65 \times V_{CC}$ | – | – | V |
| | | | 2.3 to 2.7 | 1.7 | – | – | V |
| | | | 2.7 to 3.6 | 2.0 | – | – | V |
| | | | 4.5 to 5.5 | $0.7 \times V_{CC}$ | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | 1.65 to 1.95 | – | – | $0.35 \times V_{CC}$ | V |
| | | | 2.3 to 2.7 | – | – | 0.7 | V |
| | | | 2.7 to 3.6 | – | – | 0.8 | V |
| | | | 4.5 to 5.5 | – | – | $0.3 \times V_{CC}$ | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = 100 μA | 1.65 to 5.5 | – | – | 0.1 | V |
| | | $I_O$ = 4 mA | 1.65 | – | – | 0.70 | V |
| | | $I_O$ = 8 mA | 2.3 | – | – | 0.45 | V |
| | | $I_O$ = 12 mA | 2.7 | – | – | 0.60 | V |
| | | $I_O$ = 24 mA | 3.0 | – | – | 0.80 | V |
| | | $I_O$ = 32 mA | 4.5 | – | – | 0.80 | V |
| $I_{LI}$ | input leakage current | $V_I$ = 5.5 V or GND | 1.65 to 5.5 | – | – | ±20 | μA |
| $I_{OZ}$ | output OFF-state current | $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND | 5.5 | – | – | ±10 | μA |
| $I_{off}$ | power OFF leakage current | $V_I$ or $V_O$ = 5.5 V | 0 | – | – | ±20 | μA |
| $I_{CC}$ | quiescent supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A | 5.5 | – | – | 40 | μA |
| $\Delta I_{CC}$ | additional quiescent supply current per pin | $V_I = V_{CC}$ – 0.6 V; $I_O$ = 0 A | 2.3 to 5.5 | – | – | 5000 | μA |

**Note**

1. All typical values are measured at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.

## AC CHARACTERISTICS

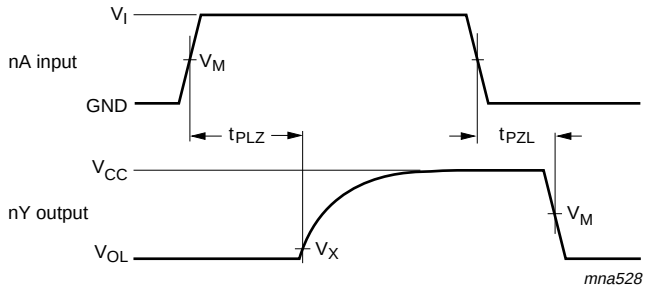
GND = 0 V.

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| | | WAVEFORMS | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = −40 °C to +85 °C**; note 1 | | | | | | | |
| $t_{PLZ}/t_{PZL}$ | propagation delay input nA to output nY | see Figs 5 and 6 | 1.65 to 1.95 | 1.0 | 3.5 | 6.7 | ns |
| | | | 2.3 to 2.7 | 0.5 | 2.4 | 4.3 | ns |
| | | | 2.7 | 1.0 | 2.3 | 4.2 | ns |
| | | | 3.0 to 3.6 | 0.5 | 2.6 | 3.7 | ns |
| | | | 4.5 to 5.5 | 0.5 | 1.5 | 2.9 | ns |
| **$T_{amb}$ = −40 °C to +125 °C** | | | | | | | |
| $t_{PLZ}/t_{PZL}$ | propagation delay input nA to output nY | see Figs 5 and 6 | 1.65 to 1.95 | 1.0 | 3.5 | 8.4 | ns |
| | | | 2.3 to 2.7 | 0.5 | 2.4 | 5.5 | ns |
| | | | 2.7 | 1.0 | 2.3 | 5.3 | ns |
| | | | 3.0 to 3.6 | 0.5 | 2.6 | 4.7 | ns |
| | | | 4.5 to 5.5 | 0.5 | 1.5 | 3.7 | ns |

**Note**

1. All typical values are measured at $T_{amb}$ = 25 °C and at $V_{CC}$ = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

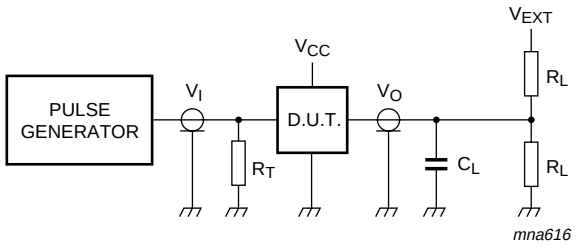
## AC WAVEFORMS




| $V_{CC}$ | $V_M$ | $V_X$ | INPUT | |
|---|---|---|---|---|
| | | | $V_I$ | $t_r = t_f$ |
| 1.65 V to 1.95 V | $0.5 \times V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{CC}$ | ≤ 2.0 ns |
| 2.3 V to 2.7 V | $0.5 \times V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{CC}$ | ≤ 2.0 ns |
| 2.7 V | 1.5 V | $V_{OL}$ + 0.3 V | 2.7 V | ≤ 2.5 ns |
| 3.0 V to 3.6 V | 1.5 V | $V_{OL}$ + 0.3 V | 2.7 V | ≤ 2.5 ns |
| 4.5 V to 5.5 V | $0.5 \times V_{CC}$ | $V_{OL}$ + 0.3 V | $V_{CC}$ | ≤ 2.5 ns |

$V_{OL}$ and $V_{OH}$ are typical output voltage drop that occur with the output load.

Fig.5 Input nA to output nY propagation delays.




| $V_{CC}$ | $V_I$ | $C_L$ | $R_L$ | $V_{EXT}$ |
|---|---|---|---|---|
| | | | | $t_{PZL}/t_{PLZ}$ |
| 1.65 V to 1.95 V | $V_{CC}$ | 30 pF | 1 kΩ | $2 \times V_{CC}$ |
| 2.3 V to 2.7 V | $V_{CC}$ | 30 pF | 500 Ω | $2 \times V_{CC}$ |
| 2.7 V | 2.7 V | 50 pF | 500 Ω | 6 V |
| 3.0 V to 3.6 V | 2.7 V | 50 pF | 500 Ω | 6 V |
| 4.5 V to 5.5 V | $V_{CC}$ | 50 pF | 500 Ω | $2 \times V_{CC}$ |

Definitions for test circuit:

$R_L$ = Load resistor.

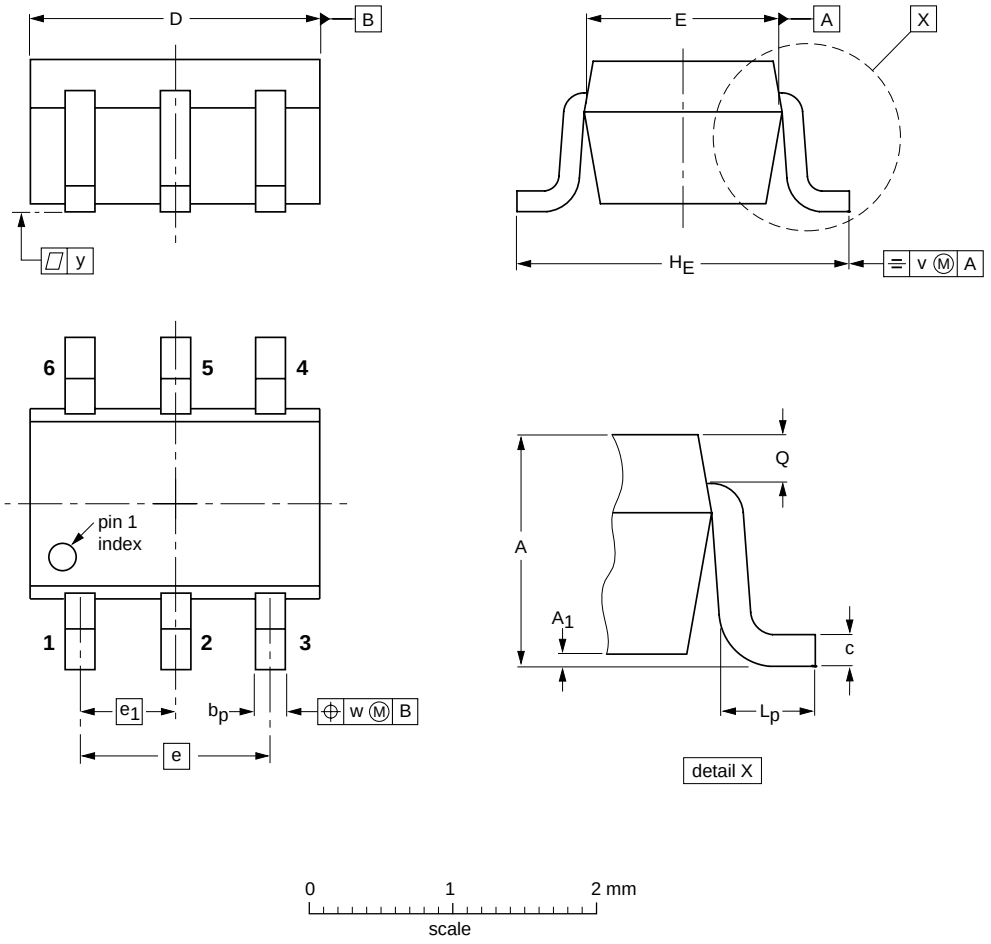
$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to the output impedance $Z_o$ of the pulse generator.

Fig.6 Load circuitry for switching times.

## PACKAGE OUTLINES

**Plastic surface mounted package; 6 leads** **SOT363**

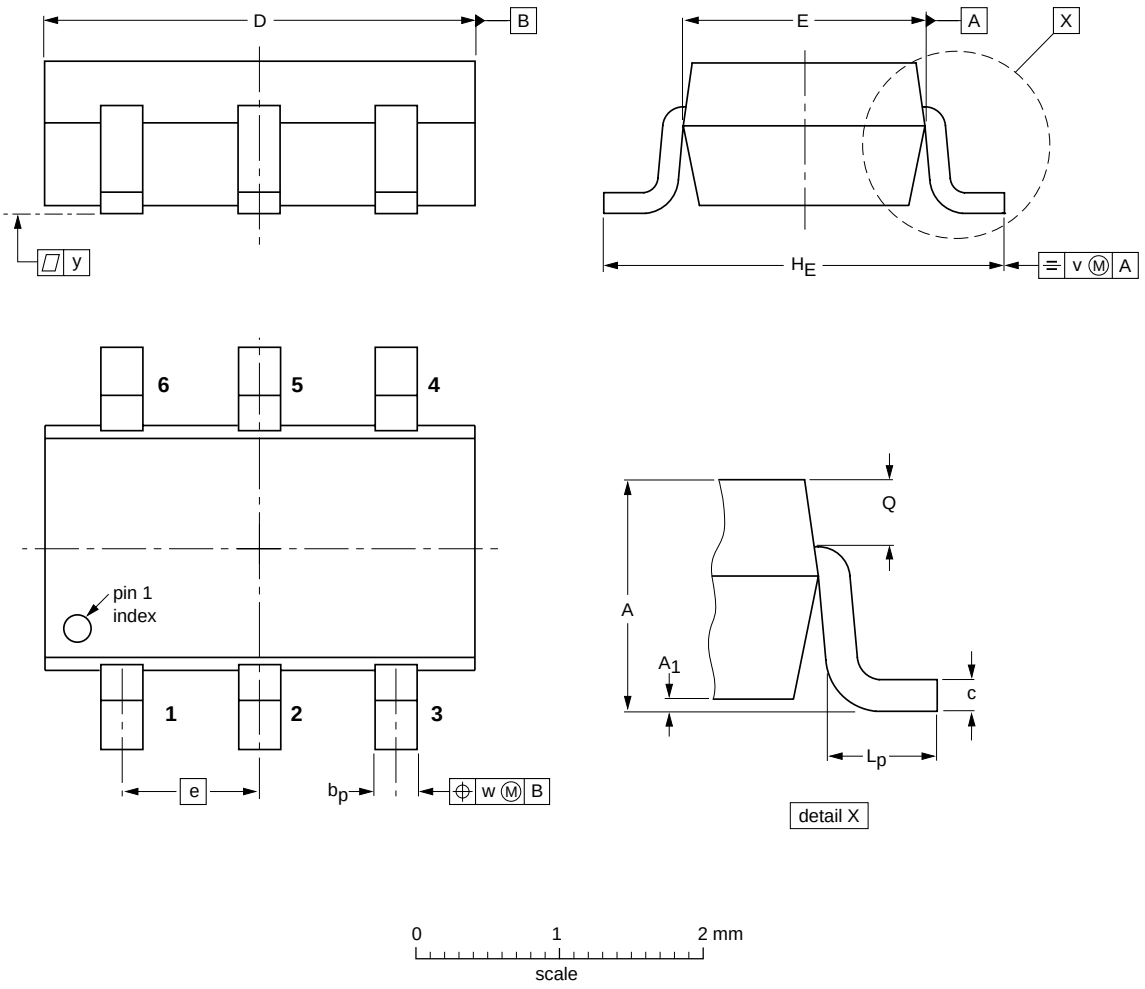



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ max | $b_p$ | c | D | E | e | $e_1$ | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.8 | 0.1 | 0.30<br>0.20 | 0.25<br>0.10 | 2.2<br>1.8 | 1.35<br>1.15 | 1.3 | 0.65 | 2.2<br>2.0 | 0.45<br>0.15 | 0.25<br>0.15 | 0.2 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT363 | | | SC-88 | | | 97-02-28 |

**Plastic surface mounted package; 6 leads** **SOT457**

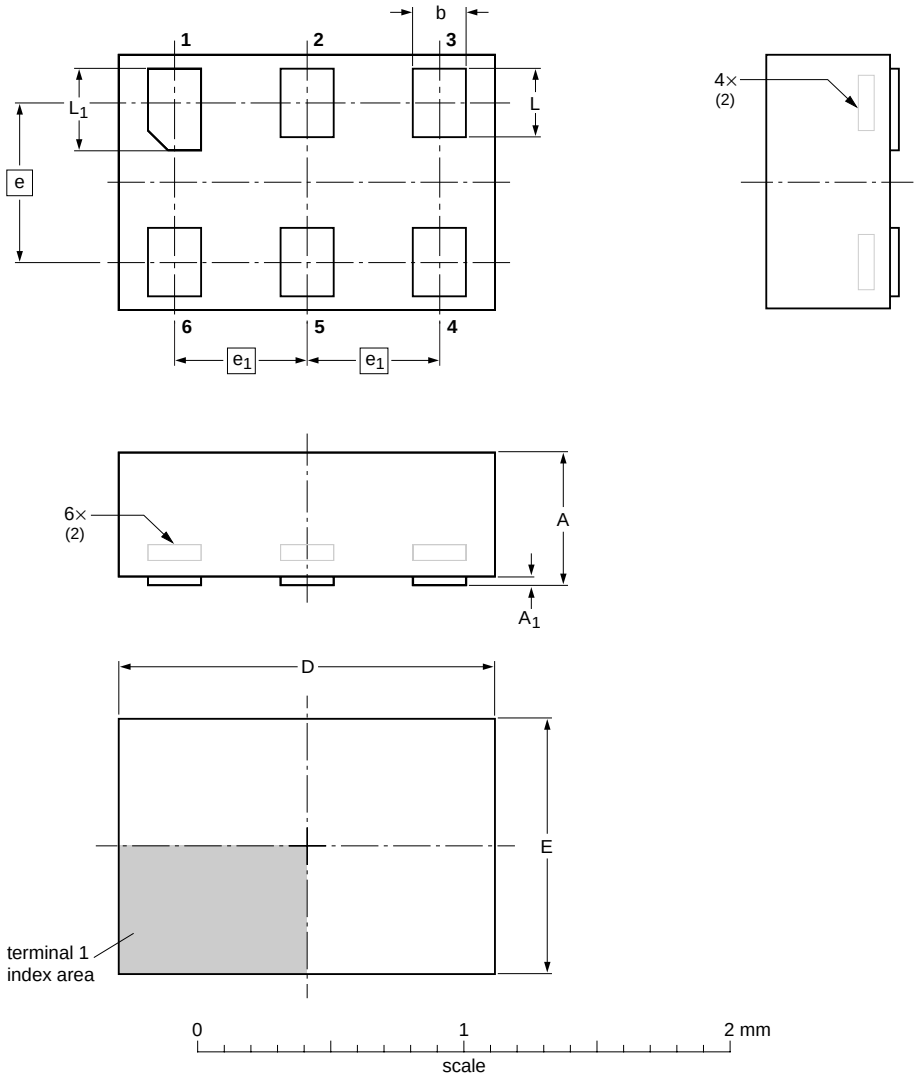



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $b_p$ | c | D | E | e | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.9 | 0.1<br>0.013 | 0.40<br>0.25 | 0.26<br>0.10 | 3.1<br>2.7 | 1.7<br>1.3 | 0.95 | 3.0<br>2.5 | 0.6<br>0.2 | 0.33<br>0.23 | 0.2 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT457 | | | SC-74 | | | ~~97-02-28~~<br>01-05-04 |

**XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm** **SOT886**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max | $A_1$ max | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|
| mm | 0.5 | 0.04 | 0.25<br>0.17 | 1.5<br>1.4 | 1.05<br>0.95 | 0.6 | 0.5 | 0.35<br>0.27 | 0.40<br>0.32 |

**Notes**
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT886 | | MO-252 | | | | ~~04-07-15~~<br>04-07-22 |

**DATA SHEET STATUS**

| LEVEL | DATA SHEET STATUS(1) | PRODUCT STATUS(2)(3) | DEFINITION |
|---|---|---|---|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
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**Notes**

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