1 Megabit Static RAM
1M x 1-Bit

Features

- ☐ High speed access times
  Com'l: 12, 15, 17 and 20 ns
  Ind'l: 15, 17 and 20 ns
- ☐ Low power operation (typical)
  - PDM41027SA
    Active: 400 mW
    Standby: 150 mW
  - PDM41027LA
    Active: 350 mW
    Standby: 100 mW
- ☐ Single +5V (±10%) power supply
- ☐ TTL-compatible inputs and outputs
- ☐ Packages
  Plastic SOJ (300 mil) - TSO
  Plastic SOJ (400 mil) - SO
  Plastic TSOP - T

Description

The PDM41027 is a high-performance CMOS static RAM organized as 1,048,576 x 1-bit. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing is accomplished when the write enable ($\overline{WE}$) and the chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW.

The PDM41027 operates from a single +5V power supply and all the inputs and outputs are fully TTL-compatible. The PDM41027 comes in two versions, the standard power version PDM41027SA and a low power version the PDM41027LA. The two versions are functionally the same and only differ in their power consumption.

The PDM41027 is available in a 28-pin plastic TSOP, 300-mil plastic SOJ and a 400-mil plastic SOJ package for surface mount applications.

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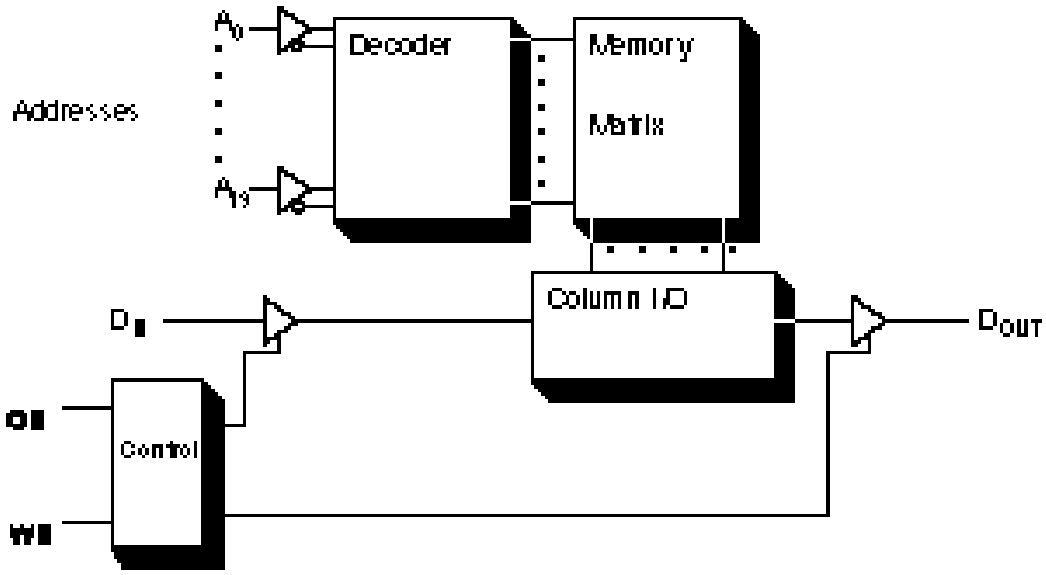
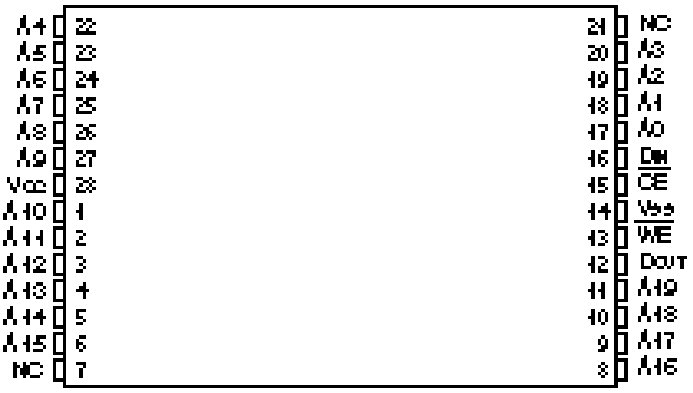
Functional Block Diagram

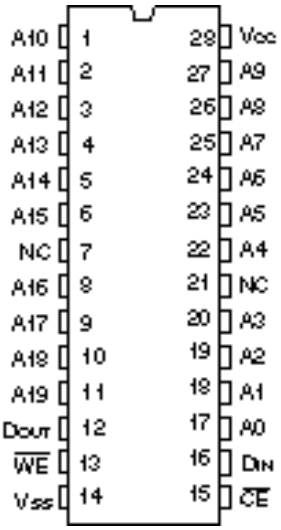


Pin Configuration

TSOP



SOJ



Pin Description

Name	Description
A19-A0	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input
$\overline{CE}$	Chip Enable Input
NC	No Connect
V_{CC}	Power (+5V)
V_{SS}	Ground

Truth Table(1)

$\overline{WE}$	$\overline{CE}$	I/O	MODE
X	H	Hi-Z	Standby
H	L	D_{OUT}	Read
L	L	D_{IN}	Write

NOTE: 1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

Absolute Maximum Ratings (1)

Symbol	Rating	Com'l.	Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to V_{SS}	–0.5 to +7.0	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
Industrial	Ambient Temperature	–40	25	85	°C
Commercial	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions		PDM41027SA		PDM41027LA		Unit
				Min.	Max.	Min.	Max.	
I_{LI}	Input Leakage Current	V_{CC} = MAX., V_{IN} = V_{SS} to V_{CC}	Com'l/ Ind.	–5	5	–5	5	µA
I_{LO}	Output Leakage Current	V_{CC} = MAX., $\overline{CE}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}	Com'l/ Ind.	–5	5	–5	5	µA
V_{IL}	Input Low Voltage			–0.5(1)	0.8	–0.5(1)	0.8	V
V_{IH}	Input High Voltage			2.2	6.0	2.2	6.0	V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA, V_{CC} = Min. I_{OL} = 10 mA, V_{CC} = Min.		— —	0.4 0.5	— —	0.4 0.5	V V
V_{OH}	Output High Voltage	I_{OH} = –4 mA, V_{CC} = Min.		2.4	—	2.4	—	V

NOTE: 1. V_{IL}(min) = –3.0V for pulse width less than 20 ns

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Power Supply Characteristics

Symbol	Parameter	Power	-10	-12		-15		-17		-20		Unit
			Com'l.	Com'l	Ind.	Com'l	Ind.	Com'l	Ind.	Com'l	Ind.	
I_{CC}	Operating Current $\overline{CE}$ = V_{IL}	SA	250	230	240	185	195	165	185	155	165	mA
	f = f_{MAX} = 1/t_{RC} V_{CC} = Max. I_{OUT} = 0 mA	LA	230	210	220	165	175	155	160	140	150	mA
I_{SB}	Standby Current $\overline{CE}$ = V_{IH}	SA	80	70	70	55	55	50	50	45	45	mA
	f = f_{MAX} = 1/t_{RC} V_{CC} = Max.	LA	75	65	65	50	50	45	50	40	40	mA
I_{SB1}	Full Standby Current $\overline{CE}$ ≥ V_{HC}	SA	20	15	25	10	15	10	15	10	15	mA
	f = 0 V_{CC} = Max., V_{IN} ≥ V_{CC} – 0.2V or ≤ 0.2V	LA	10	10	10	5	10	5	10	5	10	mA

NOTES: All values are maximum guaranteed values.
V_{LC} ≤ 0.2V, V_{HC} ≥ V_{CC} – 0.2V

Capacitance(1) (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	8	pF

NOTE:1. This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input Pulse Levels	V_{SS} to 3.0V
Input rise and fall times	3 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

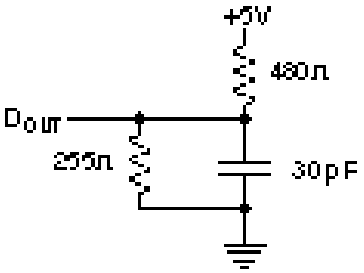


Figure 1. Output Load Equivalent

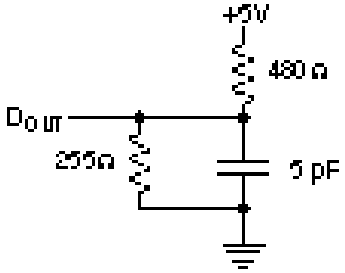


Figure 2. Output Load Equivalent (for t_{LZCE}, t_{HZCE}, t_{LZWE}, t_{HZWE})

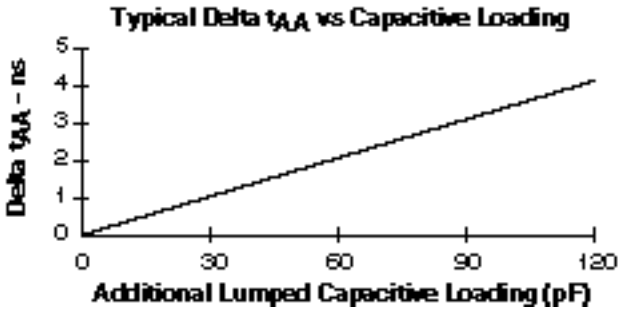
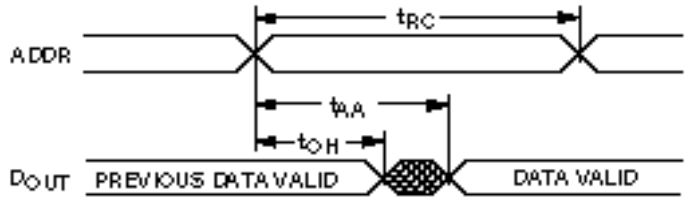
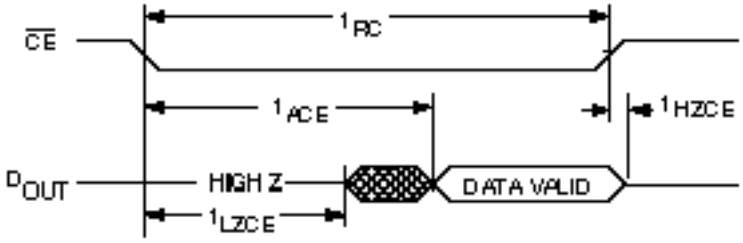


Figure 3.

Read Cycle No. 1[4,5]



Read Cycle No. 2[2,4,6]



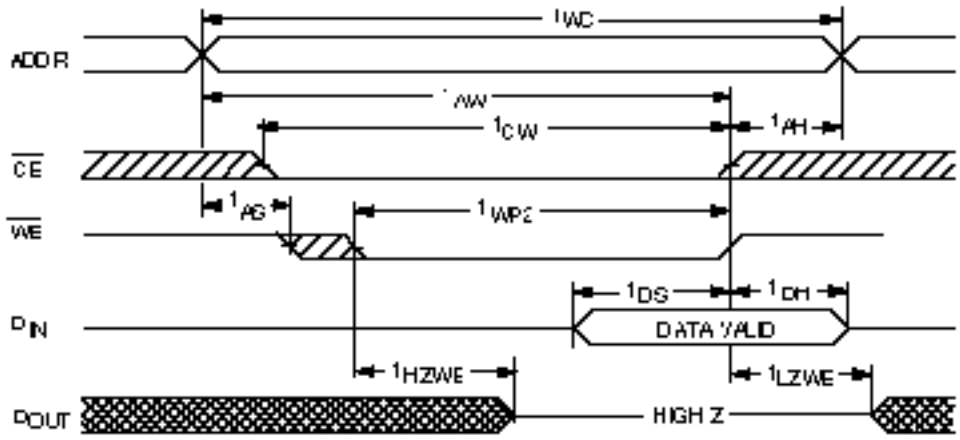
UNDEFINED

AC Electrical Characteristics

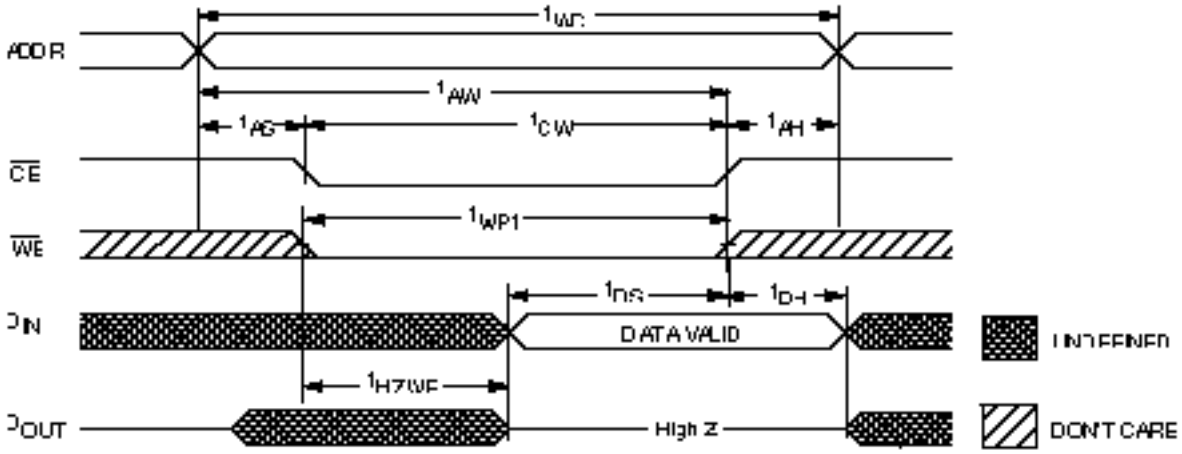
Description		-10[7]		-12[7]		-15		-17		-20		
READ Cycle	**Sym**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
READ cycle time	t_{RC}	10		12		15		17		20		ns
Address access time	t_{AA}		10		12		15		17		20	ns
Chip enable access time	t_{ACE}		10		12		15		17		20	ns
Output hold from address change	t_{OH}	3		3		3		3		3		ns
Chip enable to output in low Z[1,3]	t_{LZCE}	5		5		5		5		5		ns
Chip disable to output in high Z[1,2,3]	t_{HZCE}		6		6		7		7		8	ns
Chip enable to power up time[3]	t_{PU}	0		0		0		0		0		ns
Chip disable to power down time[3]	t_{PD}		10		12		15		17		20	ns

Notes referenced are after Data Retention Table.

Write Cycle No. 1 (Write Enable Controlled)



Write Cycle No. 2 (Chip Enable Controlled)

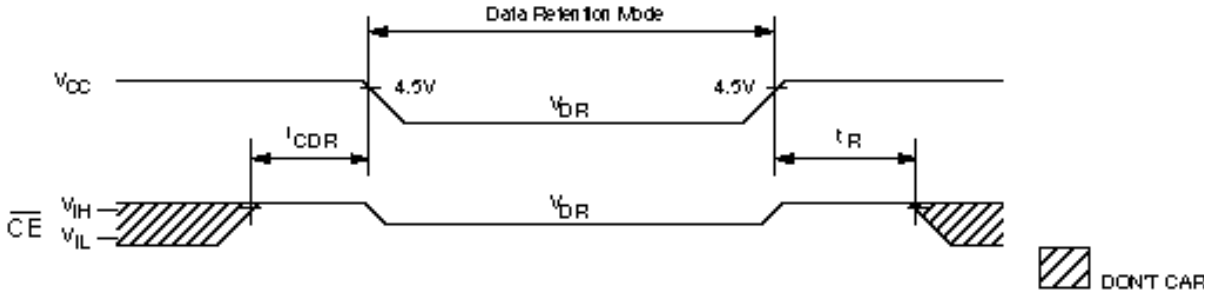


AC Electrical Characteristics

Description		-10[7]		-12[7]		-15		-17		-20		
WRITE Cycle	**Sym**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
WRITE cycle time	t_{WC}	10		12		15		17		20		ns
Chip enable active time	t_{CW}	10		10		11		12		13		ns
Address valid to end of write	t_{AW}	10		10		11		11		13		ns
Address setup time	t_{AS}	0		0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		0		ns
Write pulse width	t_{WP1}	9		10		11		12		13		ns
Write pulse width	t_{WP2}	10		11		12		13		14		ns
Data setup time	t_{DS}	7		7		7		8		8		ns
Data hold time	t_{DH}	0		0		0		0		0		ns
Write disable to output in low Z[1,3]	t_{LZWE}	0		0		0		0		0		ns
Write enable to output in high Z[1,3]	t_{HZWE}		7		7		7		8		8	ns

Notes referenced are after Data Retention Table

Low V_{CC} Data Retention Waveform



Data Retention Electrical Characteristics (LA Version Only) for JEDEC Version

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Retention Data			2	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	V_{CC} = 2V	—	95	500	µA
			V_{CC} = 3V	—	350	750	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[5]	—	—	ns

NOTES: (For three previous Electrical Characteristics tables)

1. The parameter is tested with CL = 5 pF as shown in Figure 2. Transition is measured ±200 mV from steady state voltage.
2. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}.
3. This parameter is sampled.
4. $\overline{WE}$ is HIGH for a READ cycle.
5. The device is continuously selected. Chip Enable is held in its active state.
6. The address is valid prior to or coincident with the latest occuring Chip Enable.
7. Vcc = 5V ±5%.

Ordering Information