



## 3.3V CMOS OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

**IDT74LVCH244A**

### FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015;  
> 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.65mm pitch SSOP,  
0.635mm pitch QSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ , Normal Range
- $V_{CC} = 2.3\text{V}$  to  $3.6\text{V}$ , Extended Range
- CMOS power levels ( $0.4\mu\text{W}$  typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

#### Drive Features for LVCH244A:

- High Output Drivers:  $\pm 24\text{mA}$
- Reduced system switching noise

### APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

### DESCRIPTION:

The LVCH244A octal buffer/driver is built using advanced dual metal CMOS technology. This device is organized as two 4-bit line drivers with separate output-enable ( $\overline{\text{OE}}$ ) inputs. When  $\overline{\text{OE}}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{\text{OE}}$  is high, the outputs are in the high-impedance state.

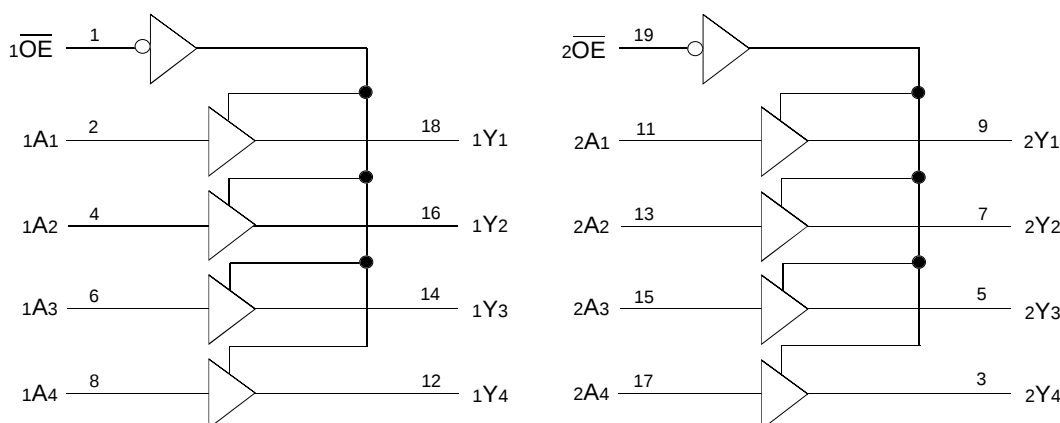
The LVCH244A has been designed with a  $\pm 24\text{mA}$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

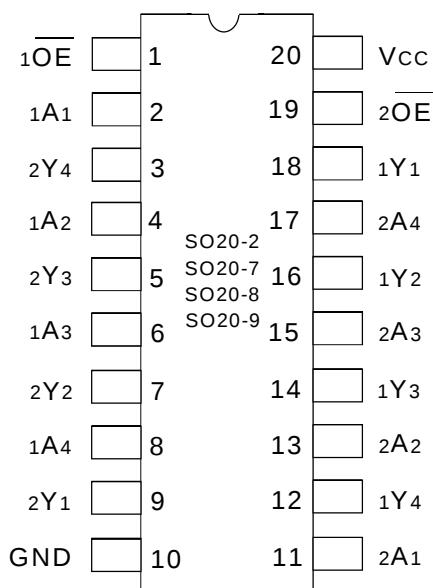
Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

The LVCH244A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SOIC/ SSOP/ QSOP/ TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

| Symbol                             | Description                                                           | Max.          | Unit |
|------------------------------------|-----------------------------------------------------------------------|---------------|------|
| V <sub>TERM</sub> <sup>(2)</sup>   | Terminal Voltage with Respect to GND                                  | – 0.5 to +6.5 | V    |
| V <sub>TERM</sub> <sup>(3)</sup>   | Terminal Voltage with Respect to GND                                  | – 0.5 to +6.5 | V    |
| T <sub>STG</sub>                   | Storage Temperature                                                   | – 65 to +150  | °C   |
| I <sub>OUT</sub>                   | DC Output Current                                                     | – 50 to +50   | mA   |
| I <sub>IK</sub><br>I <sub>OK</sub> | Continuous Clamp Current,<br>V <sub>I</sub> < 0 or V <sub>O</sub> < 0 | – 50          | mA   |
| I <sub>CC</sub><br>I <sub>SS</sub> | Continuous Current through<br>each V <sub>CC</sub> or GND             | ±100          | mA   |

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### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- All terminals except V<sub>CC</sub>.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

| Symbol           | Parameter <sup>(1)</sup> | Conditions            | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = 0V  | 4.5  | 6    | pF   |
| C <sub>OUT</sub> | Output Capacitance       | V <sub>OUT</sub> = 0V | 5.5  | 8    | pF   |
| C <sub>I/O</sub> | I/O Port Capacitance     | V <sub>IN</sub> = 0V  | 6.5  | 8    | pF   |

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### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

| Pin Names         | Description                                      |
|-------------------|--------------------------------------------------|
| x $\overline{OE}$ | Output-enable Inputs <sup>(1)</sup> (Active LOW) |
| xAx               | Data Inputs <sup>(1)</sup>                       |
| xYx               | 3-State Outputs                                  |

### NOTE:

- On LVCH these pins have “Bus-hold”. All other pins are standard inputs, outputs or I/Os.

## FUNCTION TABLE (each buffer) <sup>(1)</sup>

| Inputs            |     | Outputs |
|-------------------|-----|---------|
| x $\overline{OE}$ | xAx | xYx     |
| L                 | H   | H       |
| L                 | L   | L       |
| H                 | X   | Z       |

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  To  $+85^{\circ}\text{C}$

| Symbol                              | Parameter                                              | Test Conditions                                                          |                                          | Min. | Typ. <sup>(1)</sup> | Max.     | Unit          |
|-------------------------------------|--------------------------------------------------------|--------------------------------------------------------------------------|------------------------------------------|------|---------------------|----------|---------------|
| $V_{IH}$                            | Input HIGH Voltage Level                               | $V_{CC} = 2.3\text{V to } 2.7\text{V}$                                   |                                          | 1.7  | —                   | —        | V             |
|                                     |                                                        | $V_{CC} = 2.7\text{V to } 3.6\text{V}$                                   |                                          | 2    | —                   | —        |               |
| $V_{IL}$                            | Input LOW Voltage Level                                | $V_{CC} = 2.3\text{V to } 2.7\text{V}$                                   |                                          | —    | —                   | 0.7      | V             |
|                                     |                                                        | $V_{CC} = 2.7\text{V to } 3.6\text{V}$                                   |                                          | —    | —                   | 0.8      |               |
| $I_{IH}$<br>$I_{IL}$                | Input Leakage Current                                  | $V_{CC} = 3.6\text{V}$                                                   | $V_I = 0 \text{ to } 5.5\text{V}$        | —    | —                   | $\pm 5$  | $\mu\text{A}$ |
| $I_{OZH}$<br>$I_{OZL}$              | High Impedance Output Current<br>(3-State Output pins) | $V_{CC} = 3.6\text{V}$                                                   | $V_O = 0 \text{ to } 5.5\text{V}$        | —    | —                   | $\pm 10$ | $\mu\text{A}$ |
| $I_{OFF}$                           | Input/Output Power Off Leakage                         | $V_{CC} = 0\text{V}$ , $V_{IN}$ or $V_O \leq 5.5\text{V}$                |                                          | —    | —                   | $\pm 50$ | $\mu\text{A}$ |
| $V_{IK}$                            | Clamp Diode Voltage                                    | $V_{CC} = 2.3\text{V}$ , $I_{IN} = -18\text{mA}$                         |                                          | —    | -0.7                | -1.2     | V             |
| $V_H$                               | Input Hysteresis                                       | $V_{CC} = 3.3\text{V}$                                                   |                                          | —    | 100                 | —        | mV            |
| $I_{CCL}$<br>$I_{CCH}$<br>$I_{CCZ}$ | Quiescent Power Supply Current                         | $V_{CC} = 3.6\text{V}$                                                   | $V_{IN} = \text{GND or } V_{CC}$         | —    | —                   | 10       | $\mu\text{A}$ |
|                                     |                                                        |                                                                          | $3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$ | —    | —                   | 10       |               |
| $\Delta I_{CC}$                     | Quiescent Power Supply Current Variation               | One input at $V_{CC} - 0.6\text{V}$ ,<br>other inputs at $V_{CC}$ or GND |                                          | —    | —                   | 500      | $\mu\text{A}$ |

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### NOTES:

- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- This applies in the disabled state only.

## BUS-HOLD CHARACTERISTICS

| Symbol                   | Parameter <sup>(1)</sup>         | Test Conditions        |                                   | Min. | Typ. <sup>(2)</sup> | Max.      | Unit          |
|--------------------------|----------------------------------|------------------------|-----------------------------------|------|---------------------|-----------|---------------|
| $I_{BHH}$<br>$I_{BHL}$   | Bus-Hold Input Sustain Current   | $V_{CC} = 3.0\text{V}$ | $V_I = 2.0\text{V}$               | -75  | —                   | —         | $\mu\text{A}$ |
|                          |                                  |                        | $V_I = 0.8\text{V}$               | 75   | —                   | —         |               |
| $I_{BHH}$<br>$I_{BHL}$   | Bus-Hold Input Sustain Current   | $V_{CC} = 2.3\text{V}$ | $V_I = 1.7\text{V}$               | —    | —                   | —         | $\mu\text{A}$ |
|                          |                                  |                        | $V_I = 0.7\text{V}$               | —    | —                   | —         |               |
| $I_{BHHO}$<br>$I_{BHLO}$ | Bus-Hold Input Overdrive Current | $V_{CC} = 3.6\text{V}$ | $V_I = 0 \text{ to } 3.6\text{V}$ | —    | —                   | $\pm 500$ | $\mu\text{A}$ |

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### NOTES:

- Pins with Bus-hold are identified in the pin description.
- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.

## OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter           | Test Conditions <sup>(1)</sup> |               | Min.      | Max. | Unit |
|--------|---------------------|--------------------------------|---------------|-----------|------|------|
| VOH    | Output HIGH Voltage | VCC = 2.3V to 3.6V             | IOH = – 0.1mA | VCC – 0.2 | —    | V    |
|        |                     | VCC = 2.3V                     | IOH = – 6mA   | 2         | —    |      |
|        |                     | VCC = 2.3V                     | IOH = – 12mA  | 1.7       | —    |      |
|        |                     | VCC = 2.7V                     |               | 2.2       | —    |      |
|        |                     | VCC = 3.0V                     |               | 2.4       | —    |      |
|        |                     | VCC = 3.0V                     | IOH = – 24mA  | 2.2       | —    |      |
| VOL    | Output LOW Voltage  | VCC = 2.3V to 3.6V             | IOL = 0.1mA   | —         | 0.2  | V    |
|        |                     | VCC = 2.3V                     | IOL = 6mA     | —         | 0.4  |      |
|        |                     |                                | IOL = 12mA    | —         | 0.7  |      |
|        |                     | VCC = 2.7V                     | IOL = 12mA    | —         | 0.4  |      |
|        |                     | VCC = 3.0V                     | IOL = 24mA    | —         | 0.55 |      |

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### NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = – 40°C to +85°C.

## OPERATING CHARACTERISTICS, TA = 25°C

| Symbol | Parameter                                                        | Test Conditions     | VCC = 2.5V±0.2V | VCC = 3.3V±0.3V | Unit |
|--------|------------------------------------------------------------------|---------------------|-----------------|-----------------|------|
|        |                                                                  |                     | Typical         | Typical         |      |
| CPD    | Power Dissipation Capacitance per buffer/driver Outputs enabled  | CL = 0pF, f = 10MHz | —               | 47              | pF   |
| CPD    | Power Dissipation Capacitance per buffer/driver Outputs disabled |                     | —               | 2               | pF   |

## SWITCHING CHARACTERISTICS <sup>(1)</sup>

| Symbol       | Parameter                         | VCC = 2.5V±0.2V |      | VCC = 2.7V |      | VCC = 3.3V±0.3V |      | Unit |
|--------------|-----------------------------------|-----------------|------|------------|------|-----------------|------|------|
|              |                                   | Min.            | Max. | Min.       | Max. | Min.            | Max. |      |
| tPLH<br>tPHL | Propagation Delay<br>xAX to xYx   | —               | —    | —          | 6.9  | 1.5             | 5.9  | ns   |
| tPZH<br>tPZL | Output Enable Time<br>xOE to xYx  | —               | —    | —          | 8.6  | 1               | 7.6  | ns   |
| tPHZ<br>tPLZ | Output Disable Time<br>xOE to xYx | —               | —    | —          | 6.8  | 1.5             | 5.8  | ns   |
| tsk(0)       | Output Skew <sup>(2)</sup>        | —               | —    | —          | —    | —               | 500  | ps   |

### NOTES:

1. See test circuits and waveforms. TA = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

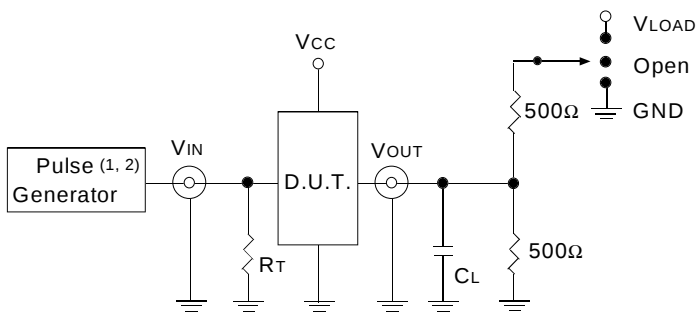
## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

| Symbol            | V <sub>CC</sub> (1) = 3.3V ± 0.3V | V <sub>CC</sub> (1) = 2.7V | V <sub>CC</sub> (2) = 2.5V ± 0.2V | Unit |
|-------------------|-----------------------------------|----------------------------|-----------------------------------|------|
| V <sub>LOAD</sub> | 6                                 | 6                          | 2 x V <sub>CC</sub>               | V    |
| V <sub>IH</sub>   | 2.7                               | 2.7                        | V <sub>CC</sub>                   | V    |
| V <sub>T</sub>    | 1.5                               | 1.5                        | V <sub>CC</sub> / 2               | V    |
| V <sub>LZ</sub>   | 300                               | 300                        | 150                               | mV   |
| V <sub>HZ</sub>   | 300                               | 300                        | 150                               | mV   |
| C <sub>L</sub>    | 50                                | 50                         | 30                                | pF   |

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### TEST CIRCUITS FOR ALL OUTPUTS



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#### DEFINITIONS:

C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.

R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

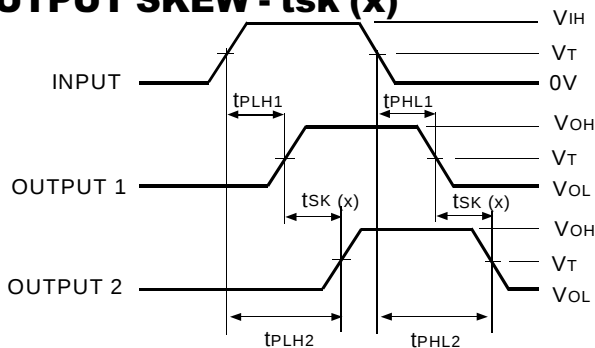
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2.5ns; t<sub>R</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2ns; t<sub>R</sub> ≤ 2ns.

### SWITCH POSITION

| Test            | Switch            |
|-----------------|-------------------|
| Open Drain      | V <sub>LOAD</sub> |
| Disable Low     |                   |
| Enable Low      |                   |
| Disable High    | GND               |
| Enable High     |                   |
| All Other tests | Open              |

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### OUTPUT SKEW - t<sub>SK</sub>(x)



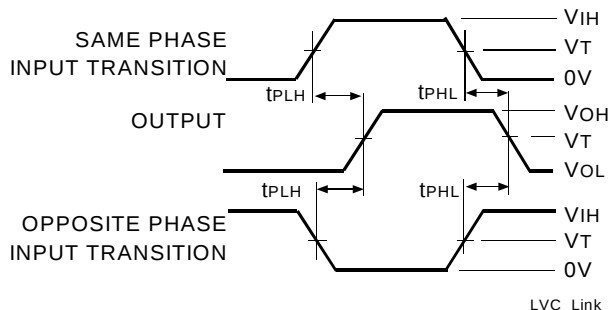
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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#### NOTES:

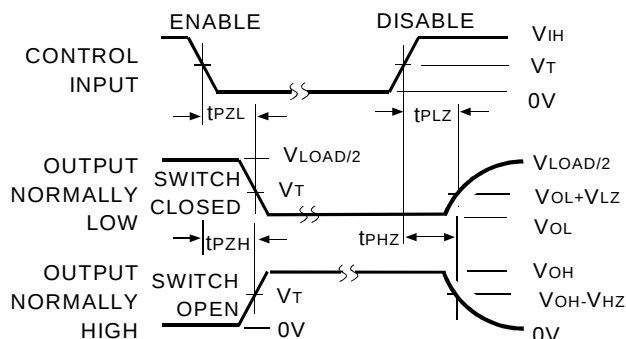
1. For t<sub>SK</sub>(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t<sub>SK</sub>(b) OUTPUT1 and OUTPUT2 are in the same bank.

### PROPAGATION DELAY



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### ENABLE AND DISABLE TIMES

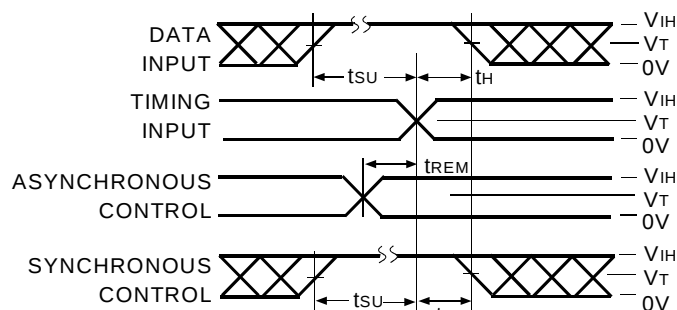


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#### NOTE:

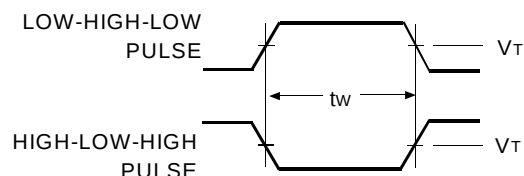
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

### SET-UP, HOLD, AND RELEASE TIMES



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### PULSE WIDTH



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## ORDERING INFORMATION

| IDT         | XX | LVC | X        | XXXX        | XX      |                                                             |
|-------------|----|-----|----------|-------------|---------|-------------------------------------------------------------|
| Temp. Range |    |     | Bus-Hold | Device Type | Package |                                                             |
|             |    |     |          |             | SO      | Small Outline IC (gull wing) (SO20-2)                       |
|             |    |     |          |             | PY      | Shrink Small Outline Package (SO20-7)                       |
|             |    |     |          |             | Q       | Quarter Size Small Outline Package (SO20-8)                 |
|             |    |     |          |             | PG      | Thin Shrink Small Outline Package (SO20-9)                  |
|             |    |     |          | 244A        |         | Octal Buffer/Driver with 3-State Outputs, $\pm 24\text{mA}$ |
|             |    |     | H        |             |         | Bus-hold                                                    |
|             |    |     |          | 74          |         | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$              |



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