

74LVC2G74-Q100

Single D-type flip-flop with set and reset;
positive edge trigger

Rev. 6 — 22 September 2025

Product data sheet

1. General description

The 74LVC2G74-Q100 is a single positive edge triggered D-type flip-flop with individual data (D), clock (CP), set (SD) and reset (RD) inputs, and complementary Q and \bar{Q} outputs. Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74LVC2G74DP-Q100	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm		SOT505-2
74LVC2G74DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm		SOT765-1

4. Marking

Table 2. Marking codes

Type number	Marking code [1]
74LVC2G74DP-Q100	V74
74LVC2G74DC-Q100	V74

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

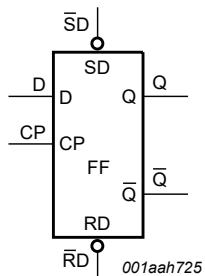


Fig. 1. Logic symbol

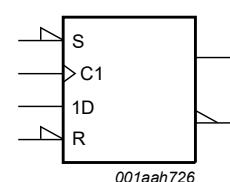


Fig. 2. IEC logic symbol

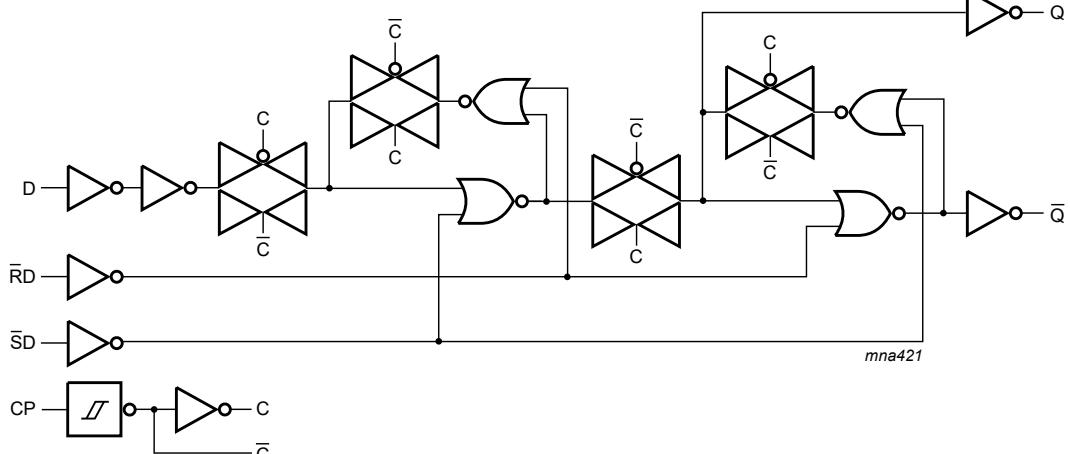
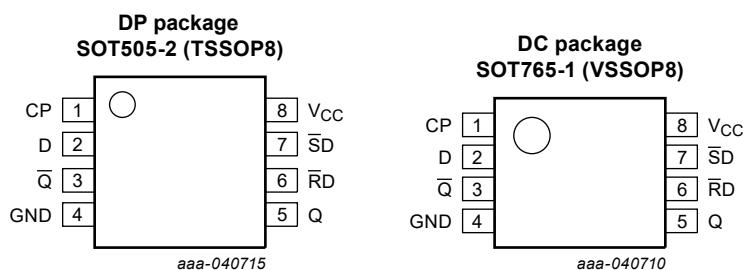


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
CP	1	clock input (LOW-to-HIGH, edge-triggered)
D	2	data input
Q	3	complement output
GND	4	ground (0 V)
Q	5	true output
RD	6	asynchronous reset-direct input (active LOW)
SD	7	asynchronous set-direct input (active LOW)
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table for asynchronous operation

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input				Output	
SD	RD	CP	D	Q	Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	L	X	Q	Q

Table 5. Function table for synchronous operation

H = HIGH voltage level; L = LOW voltage level; \uparrow = LOW-to-HIGH CP transition;

Q_{n+1} = state after the next LOW-to-HIGH CP transition.

Input				Output	
SD	RD	CP	D	Q_{n+1}	\bar{Q}_{n+1}
H	H	\uparrow	L	L	H
H	H	\uparrow	H	H	L

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		[1]	-0.5	+6.5
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
V_O	output voltage	Active mode	[1]	-0.5	$V_{CC} + 0.5$
		Power-down mode; $V_{CC} = 0$ V	[1]	-0.5	+6.5
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2]	-	250
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT505-2 (TSSOP8) package: P_{tot} derates linearly with 4.6 mW/K above 96 °C.

For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.

9. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	10	ns/V

10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 µA; V _{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V _{CC} - 0.1	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	1.54	-	0.95	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.9	2.15	-	1.7	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	2.50	-	1.9	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.3	2.62	-	2.0	-	V
		I _O = -32 mA; V _{CC} = 4.5 V	3.8	4.11	-	3.4	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 µA; V _{CC} = 1.65 V to 5.5 V	-	-	0.10	-	0.10	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	0.07	0.45	-	0.70	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	0.12	0.30	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	0.17	0.40	-	0.60	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	0.33	0.55	-	0.80	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	0.39	0.55	-	0.80	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	±0.1	±1	-	±1	µA
I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	±0.1	±2	-	±2	µA
I _{CC}	supply current	V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A	-	0.1	4	-	4	µA
ΔI _{CC}	additional supply current	per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V	-	5	500	-	500	µA
C _I	input capacitance		-	4.0	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Fig. 6](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	CP to Q, \bar{Q} ; see Fig. 4 [2]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.5	6.0	13.4	1.5	13.4	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	3.5	7.1	1.0	7.1	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	3.5	7.1	1.0	7.1	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	3.5	5.9	1.0	5.9	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.0	2.5	4.1	1.0	4.1	ns
		SD to Q, \bar{Q} ; see Fig. 5 [2]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.5	6.0	12.9	1.5	12.9	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	3.5	7.0	1.0	7.0	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	3.5	7.0	1.0	7.0	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	3.0	5.9	1.0	5.9	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.0	2.5	4.1	1.0	4.1	ns
		$\bar{R}D$ to Q, \bar{Q} ; see Fig. 5 [2]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.5	5.0	12.9	1.5	12.9	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	3.5	7.0	1.0	7.0	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	3.5	7.0	1.0	7.0	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	3.0	5.9	1.0	5.9	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.0	2.5	4.1	1.0	4.1	ns
t_w	pulse width	CP HIGH or LOW; see Fig. 4						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	6.2	-	-	6.2	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2.7	-	-	2.7	-	ns
		$V_{CC} = 2.7 \text{ V}$	2.7	-	-	2.7	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.7	1.3	-	2.7	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	ns
		SD and $\bar{R}D$ LOW; see Fig. 5						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	6.2	-	-	6.2	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2.7	-	-	2.7	-	ns
		$V_{CC} = 2.7 \text{ V}$	2.7	-	-	2.7	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.7	1.6	-	2.7	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	ns
t_{rec}	recovery time	SD or $\bar{R}D$; see Fig. 5						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.9	-	-	1.9	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.4	-	-	1.4	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.3	-	-	1.3	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	+1.2	-3.0	-	+1.2	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.0	-	-	1.0	-	ns

Single D-type flip-flop with set and reset; positive edge trigger

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t _{su}	set-up time	D to CP; see Fig. 4						
		V _{CC} = 1.65 V to 1.95 V	2.9	-	-	2.9	-	ns
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	ns
		V _{CC} = 2.7 V	1.7	-	-	1.7	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.3	0.5	-	1.3	-	ns
		V _{CC} = 4.5 V to 5.5 V	1.1	-	-	1.1	-	ns
t _h	hold time	D to CP; see Fig. 4						
		V _{CC} = 1.65 V to 1.95 V	1.5	-	-	1.5	-	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	-	-	1.0	-	ns
		V _{CC} = 2.7 V	1.0	-	-	1.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	0.6	-	1.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	1.0	-	-	1.0	-	ns
f _{max}	maximum frequency	CP; see Fig. 4						
		V _{CC} = 1.65 V to 1.95 V	80	-	-	80	-	MHz
		V _{CC} = 2.3 V to 2.7 V	175	-	-	175	-	MHz
		V _{CC} = 2.7 V	175	-	-	175	-	MHz
		V _{CC} = 3.0 V to 3.6 V	175	280	-	175	-	MHz
		V _{CC} = 4.5 V to 5.5 V	200	-	-	200	-	MHz
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; V _{CC} = 3.3 V [3]	-	15	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

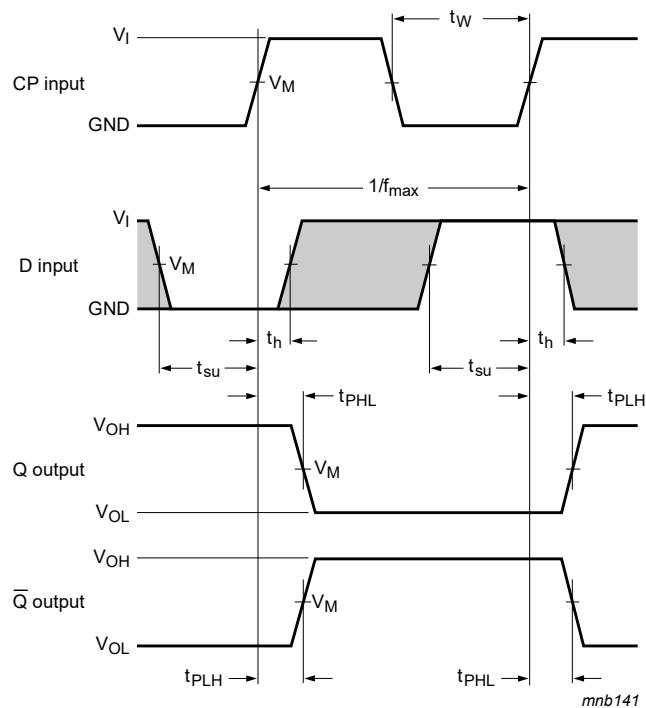
$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz;

C_L = output load capacitance in pF; V_{CC} = supply voltage in V;

N = number of inputs switching; $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit



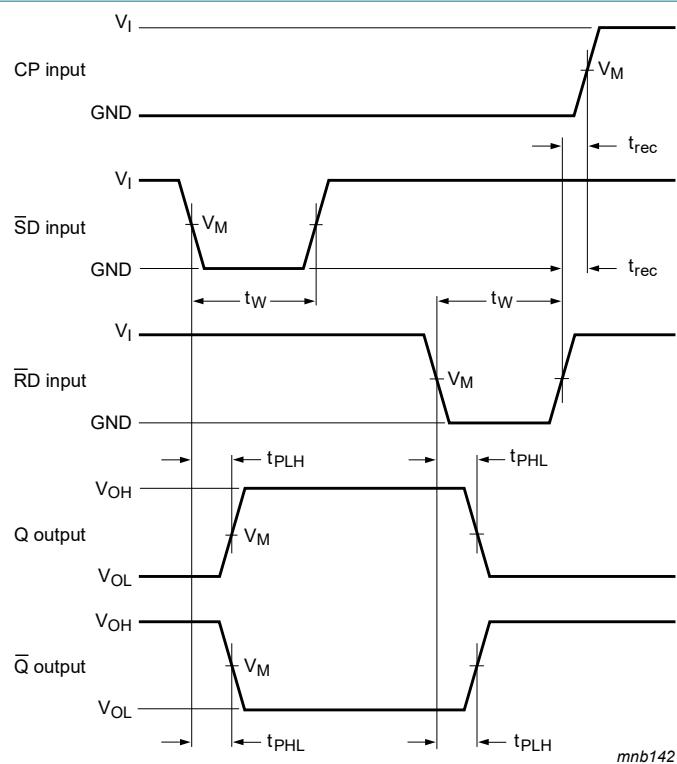
Measurement points are given in [Table 10](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The clock input (CP) to output (Q, \bar{Q}) propagation delays, the clock pulse width, the D to CP set-up time, the CP to D hold time and the CP maximum frequency

Single D-type flip-flop with set and reset; positive edge trigger



Measurement points are given in [Table 10](#).

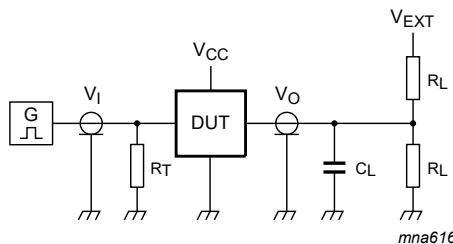
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. The set (SD) and reset (RD) input to output (Q, Q̄) propagation delays, the set and reset pulse widths and the RD to CP recovery time

Table 10. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

Single D-type flip-flop with set and reset; positive edge trigger



Test data is given in [Table 11](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 6. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}			
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}	
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open	GND	$2V_{CC}$	
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2V_{CC}$	
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V	
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V	
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$	

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

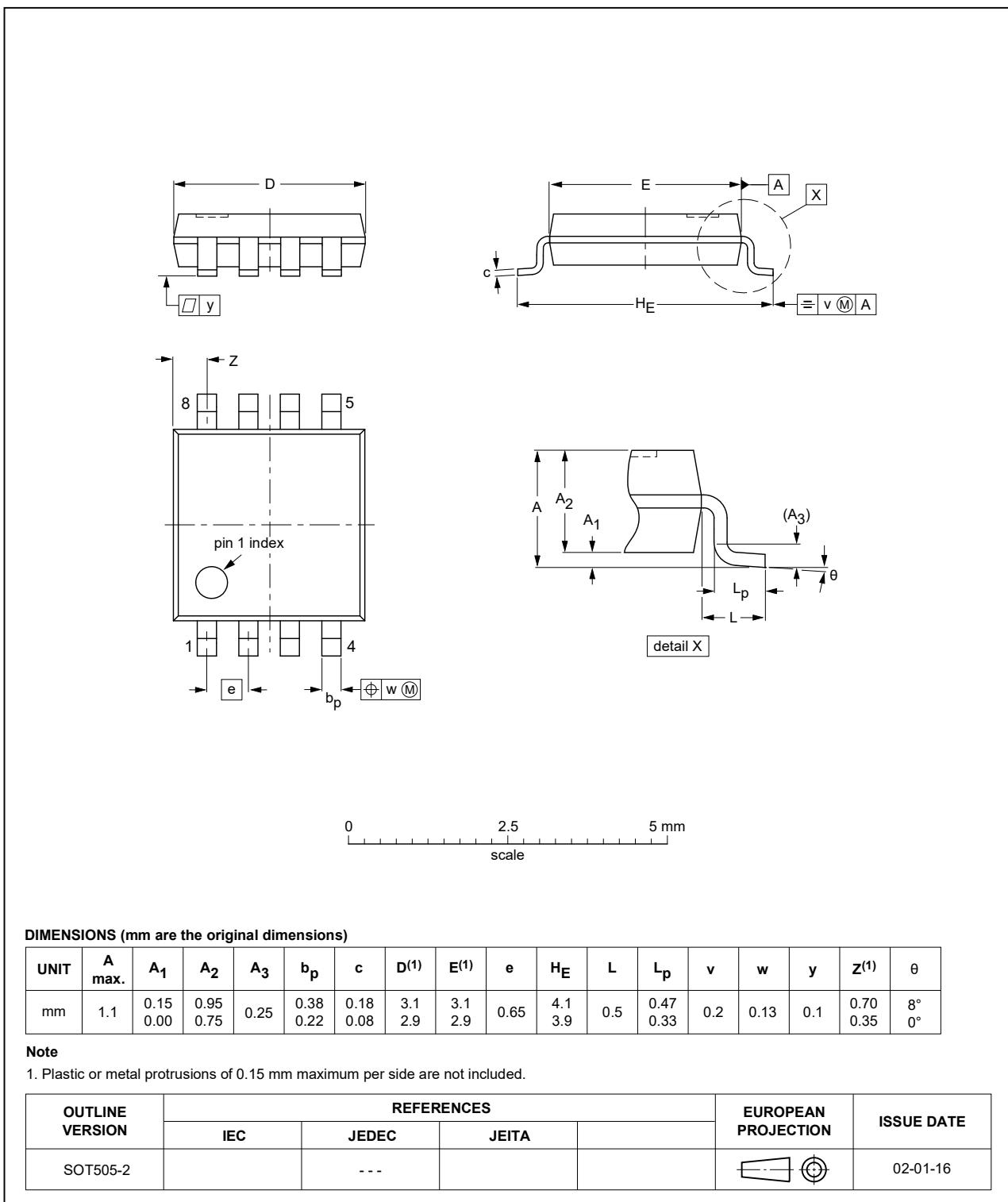


Fig. 7. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

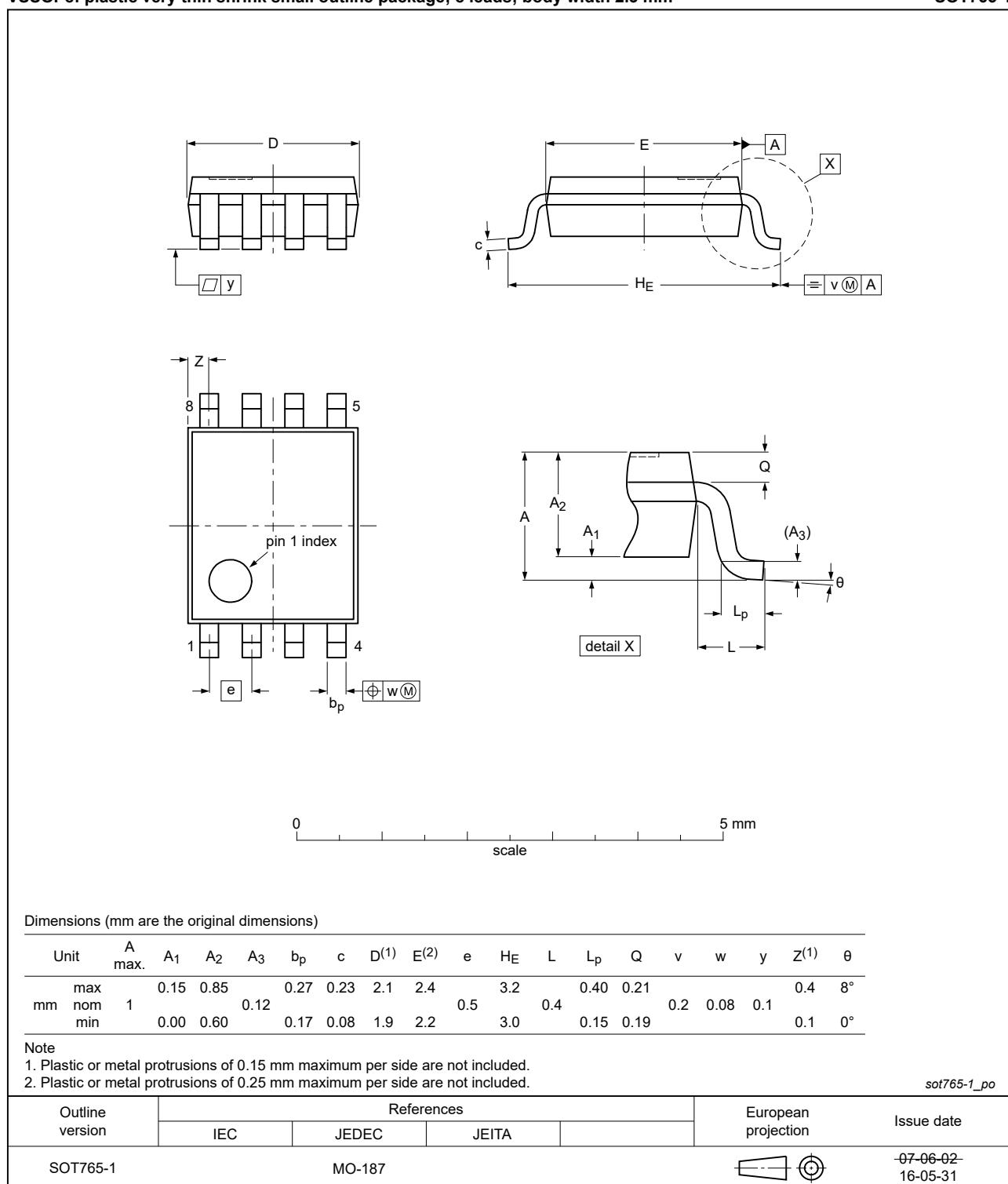


Fig. 8. Package outline SOT765-1 (VSSOP8)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G74_Q100 v.6	20250922	Product data sheet	-	74LVC2G74_Q100 v.5
Modifications:	<ul style="list-style-type: none"> Updates made to Table 4. 			
74LVC2G74_Q100 v.5	20230822	Product data sheet	-	74LVC2G74_Q100 v.4
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74LVC2G74_Q100 v.4	20210421	Product data sheet	-	74LVC2G74_Q100 v.3
Modifications:	<ul style="list-style-type: none"> Section 1 and Section 2 updated. Section 8: P_{tot} total power dissipation and its derating values updated. 			
74LVC2G74_Q100 v.3	20181003	Product data sheet	-	74LVC2G74_Q100 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74LVC2G74_Q100 v.2	20161214	Product data sheet	-	74LVC2G74_Q100 v.1
Modifications:	<ul style="list-style-type: none"> Table 8: The maximum limits for leakage current and supply current have changed. 			
74LVC2G74_Q100 v.1	20121224	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

Definitions

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