

## Features

- Fast Read Access Time – 70 ns
- Low Power CMOS Operation
  - 100  $\mu$ A Max Standby
  - 30 mA Max Active at 5 MHz
- JEDEC Standard Packages
  - 32-lead PDIP
  - 32-lead PLCC
  - 32-lead TSOP
- 5V  $\pm$  10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming Algorithm – 100  $\mu$ s/Byte (Typical)
- CMOS and TTL Compatible Inputs and Outputs
- Industrial Temperature Range
- Green (Pb/Halide-free) Packaging Option

## 1. Description

The AT27C040 chip is a low-power, high-performance, 4,194,304-bit one-time programmable read-only memory (OTP EPROM) organized as 512K by 8 bits. The AT27C040 requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 70 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

Atmel's scaled CMOS technology provides low active power consumption, and fast programming. Power consumption is typically 8 mA in active mode and less than 10  $\mu$ A in standby mode.

The AT27C040 is available in a choice of industry-standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC and TSOP packages. The device features two-line control ( $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ ) to eliminate bus contention in high-speed systems.

Atmel's AT27C040 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100  $\mu$ s/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry-standard programming equipment to select the proper programming algorithms and voltages.



**4-Megabit  
(512K x 8)  
OTP EPROM**

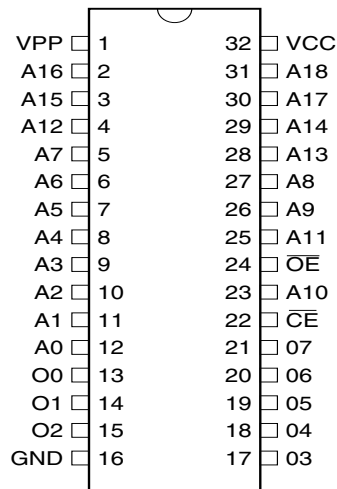
**AT27C040**



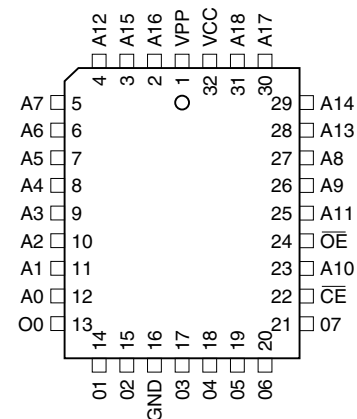
## 2. Pin Configurations

Pin Name	Function
A0 - A18	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

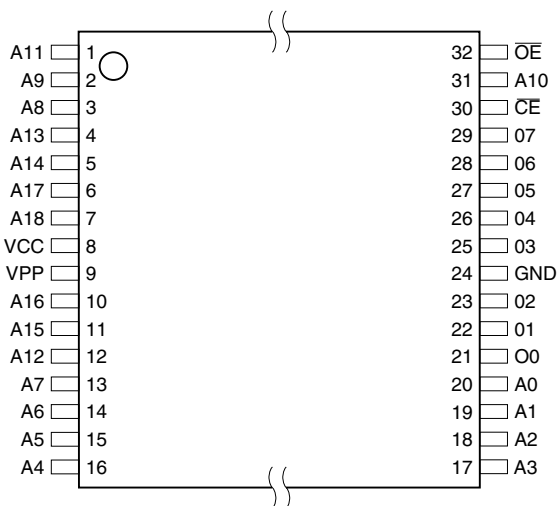
### 2.1 32-lead PDIP Top View



### 2.3 32-lead PLCC Top View



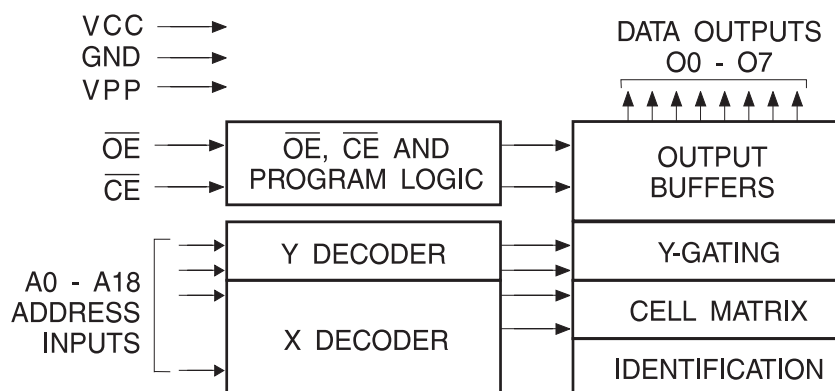
### 2.2 32-lead TSOP Top View



### 3. Switching Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device non-conformance. At a minimum, a 0.1  $\mu\text{F}$  high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the  $V_{CC}$  and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7  $\mu\text{F}$  bulk electrolytic capacitor should be utilized, again connected between the  $V_{CC}$  and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

### 4. Block Diagram



### 5. Absolute Maximum Ratings\*

Temperature Under Bias .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-2.0V to +7.0V
Voltage on A9 with Respect to Ground .....	-2.0V to +14.0V
$V_{PP}$ Supply Voltage with Respect to Ground .....	-2.0V to +14.0V

**\*NOTICE:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## 6. Operating Modes

Mode/Pin	$\overline{CE}$	$\overline{OE}$	Ai	V <sub>PP</sub>	Outputs
Read	V <sub>IL</sub>	V <sub>IL</sub>	Ai	X <sup>(1)</sup>	D <sub>OUT</sub>
Output Disable	X	V <sub>IH</sub>	X	X	High Z
Standby	V <sub>IH</sub>	X	X	X	High Z
Rapid Program <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	Ai	V <sub>PP</sub>	D <sub>IN</sub>
PGM Verify	X	V <sub>IL</sub>	Ai	V <sub>PP</sub>	D <sub>OUT</sub>
PGM Inhibit	V <sub>IH</sub>	V <sub>IH</sub>	X	V <sub>PP</sub>	High Z
Product Identification <sup>(4)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	A9 = V <sub>H</sub> <sup>(3)</sup> A0 = V <sub>IH</sub> or V <sub>IL</sub> A1 - A18 = V <sub>IL</sub>	X	Identification Code

- Notes:
1. X can be V<sub>IL</sub> or V<sub>IH</sub>.
  2. Refer to Programming Characteristics
  3. V<sub>H</sub> = 12.0 ± 0.5V.
  4. Two identifier bytes may be selected. All Ai inputs are held low (V<sub>IL</sub>), except A9 which is set to V<sub>H</sub> and A0 which is toggled low (V<sub>IL</sub>) to select the Manufacturer's Identification byte and high (V<sub>IH</sub>) to select the Device Code byte.

## 7. DC and AC Operating Conditions for Read Operation

	AT27C040-70	AT27C040-90
Industrial Operating Temperature (Case)	-40°C - 85°C	-40°C - 85°C
V <sub>CC</sub> Power Supply	5V ± 10%	5V ± 10%

## 8. DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0V to V <sub>CC</sub>		±1	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0V to V <sub>CC</sub>		±5	μA
I <sub>PP1</sub> <sup>(2)</sup>	V <sub>PP</sub> <sup>(1)</sup> Read/Standby Current	V <sub>PP</sub> = V <sub>CC</sub>		10	μA
I <sub>SB</sub>	V <sub>CC1</sub> <sup>(1)</sup> Standby Current	I <sub>SB1</sub> (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		100	μA
		I <sub>SB2</sub> (TTL), $\overline{CE} = 2.0$ to V <sub>CC</sub> + 0.5V		1	mA
I <sub>CC</sub>	V <sub>CC</sub> Active Current	f = 5 MHz, I <sub>OUT</sub> = 0 mA, $\overline{CE} = V_{IL}$		30	mA
V <sub>IL</sub>	Input Low Voltage		-0.6	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4		V

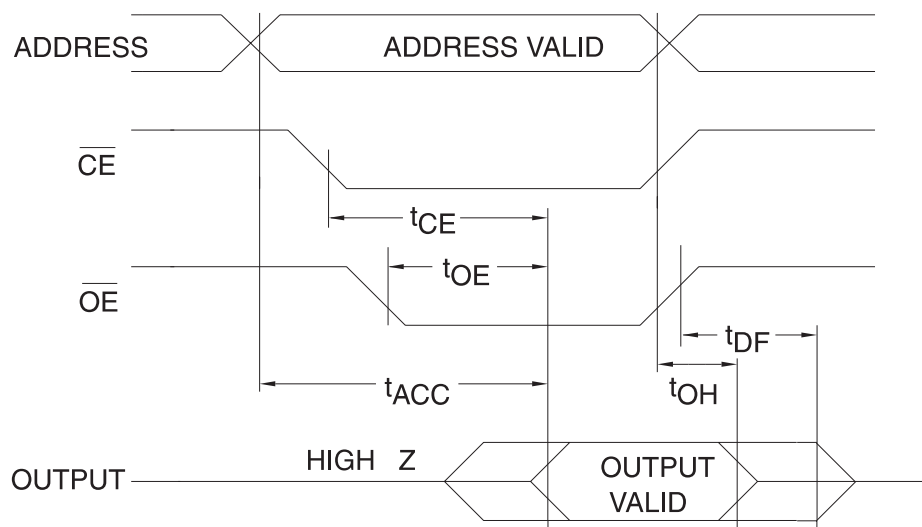
- Notes:
1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.
  2. V<sub>PP</sub> may be connected directly to V<sub>CC</sub>, except during programming. The supply current would then be the sum of I<sub>CC</sub> and I<sub>PP</sub>.

## 9. AC Characteristics for Read Operation

Symbol	Parameter	Condition	AT27C040				Units
			-70		-90		
			Min	Max	Min	Max	
t <sub>ACC</sub> <sup>(1)</sup>	Address to Output Delay	$\overline{CE} = \overline{OE}$ = V <sub>IL</sub>		70		90	ns
t <sub>CE</sub> <sup>(1)</sup>	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		70		90	ns
t <sub>OE</sub> <sup>(1)</sup>	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		30		35	ns
t <sub>DF</sub> <sup>(1)</sup>	$\overline{OE}$ or $\overline{CE}$ High to Output Float, Whichever Occurred First			20		20	ns
t <sub>OH</sub>	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ , Whichever Occurred First		0		0		ns

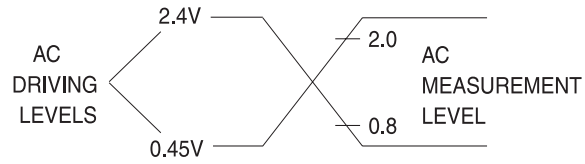
Note: 1. See AC Waveforms for Read Operation

## 10. AC Waveforms for Read Operation<sup>(1)</sup>

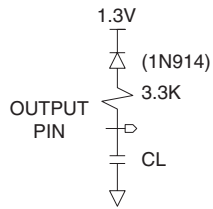


- Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
  2.  $\overline{OE}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
  3.  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the address is valid without impact on  $t_{ACC}$ .
  4. This parameter is only sampled and is not 100% tested.
  5. Output float is defined as the point when data is no longer driven.

## 11. Input Test Waveforms and Measurement Levels



## 12. Output Test Load



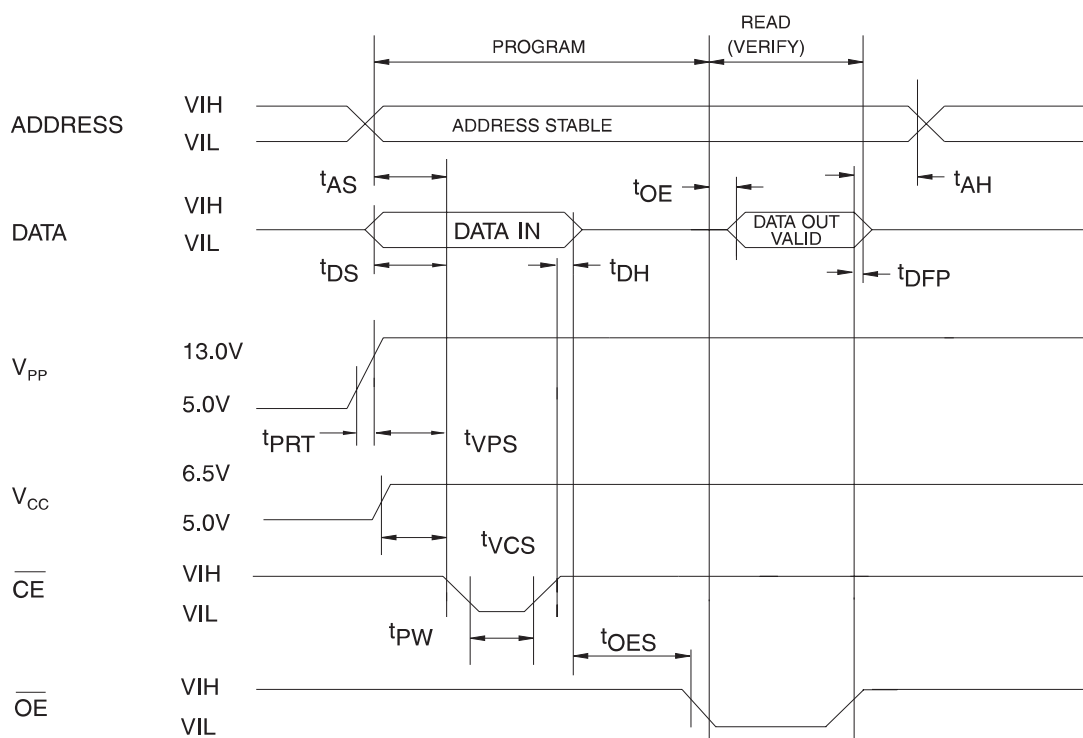
## 13. Pin Capacitance

$f = 1 \text{ MHz}$ ,  $T = 25^\circ\text{C}$  <sup>(1)</sup>

Symbol	Typ	Max	Units	Conditions
$C_{\text{IN}}$	4	8	pF	$V_{\text{IN}} = 0\text{V}$
$C_{\text{OUT}}$	8	12	pF	$V_{\text{OUT}} = 0\text{V}$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

## 14. Programming Waveforms<sup>(1)</sup>



- Notes:
1. The Input Timing Reference is 0.8V for  $V_{IL}$  and 2.0V for  $V_{IH}$ .
  2.  $t_{OE}$  and  $t_{DFP}$  are characteristics of the device but must be accommodated by the programmer.
  3. When programming the AT27C040 a 0.1  $\mu F$  capacitor is required across  $V_{PP}$  and ground to suppress spurious voltage transients.

## 15. DC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{V}$ ,  $V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
$I_{LI}$	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		$\pm 10$	$\mu\text{A}$
$V_{IL}$	Input Low Level		-0.6	0.8	V
$V_{IH}$	Input High Level		2.0	$V_{CC} + 0.7$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1 \text{ mA}$		0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -400 \mu\text{A}$	2.4		V
$I_{CC2}$	$V_{CC}$ Supply Current (Program and Verify)			40	mA
$I_{PP2}$	$V_{PP}$ Supply Current	$\overline{CE} = V_{IL}$		20	mA
$V_{ID}$	A9 Product Identification Voltage		11.5	12.5	V

## 16. AC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{V}$ ,  $V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Limits		Units
			Min	Max	
$t_{AS}$	Address Setup Time	Input Rise and Fall Times: (10% to 90%) 20 ns	2		$\mu\text{s}$
$t_{OES}$	$\overline{OE}$ Setup Time		2		$\mu\text{s}$
$t_{DS}$	Data Setup Time		2		$\mu\text{s}$
$t_{AH}$	Address Hold Time		0		$\mu\text{s}$
$t_{DH}$	Data Hold Time	Input Pulse Levels: 0.45V to 2.4V	2		$\mu\text{s}$
$t_{DFP}$	$\overline{OE}$ High to Output Float Delay <sup>(2)</sup>		0	130	ns
$t_{VPS}$	$V_{PP}$ Setup Time	Input Timing Reference Level: 0.8V to 2.0V	2		$\mu\text{s}$
$t_{VCS}$	$V_{CC}$ Setup Time		2		$\mu\text{s}$
$t_{PW}$	$\overline{CE}$ Program Pulse Width <sup>(3)</sup>	Output Timing Reference Level: 0.8V to 2.0V	95	105	$\mu\text{s}$
$t_{OE}$	Data Valid from $\overline{OE}$ <sup>(2)</sup>			150	ns
$t_{PRT}$	$V_{PP}$ Pulse Rise Time During Programming		50		ns

- Notes:
- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$
  - This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.
  - Program Pulse width tolerance is  $100 \mu\text{sec} \pm 5\%$ .

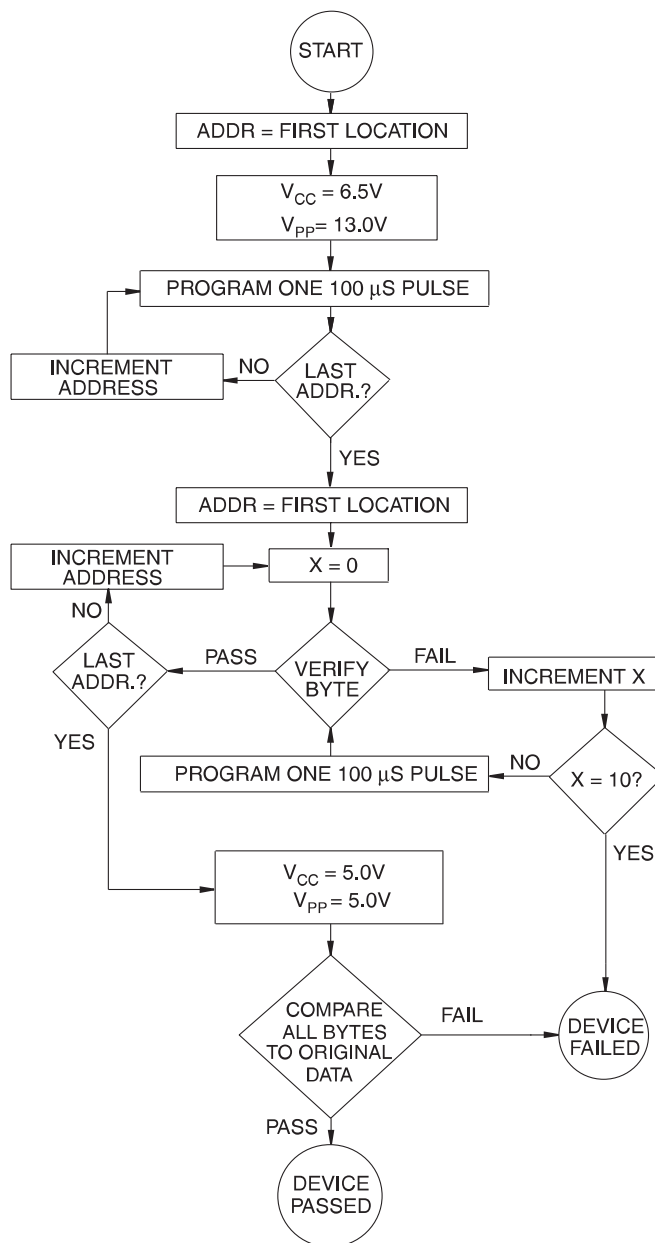
## 17. Atmel's AT27C040 Integrated Product Identification Code

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	0	1	1	0B



## 18. Rapid Programming Algorithm

A 100  $\mu\text{s}$   $\overline{\text{CE}}$  pulse width is used to program. The address is set to the first location.  $V_{\text{CC}}$  is raised to 6.5V and  $V_{\text{PP}}$  is raised to 13.0V. Each address is first programmed with one 100  $\mu\text{s}$   $\overline{\text{CE}}$  pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100  $\mu\text{s}$  pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked.  $V_{\text{PP}}$  is then lowered to 5.0V and  $V_{\text{CC}}$  to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.





## 19. Ordering Information

### 19.1 Standard Package

$t_{ACC}$ (ns)	$I_{CC}$ (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	30	0.1	AT27C040-70JI AT27C040-70PI AT27C040-70TI	32J 32P6 32T	Industrial (-40°C to 85°C)
90	30	0.1	AT27C040-90JI AT27C040-90PI AT27C040-90TI	32J 32P6 32T	Industrial (-40°C to 85°C)

Note: Refer to PCN# SC042702.

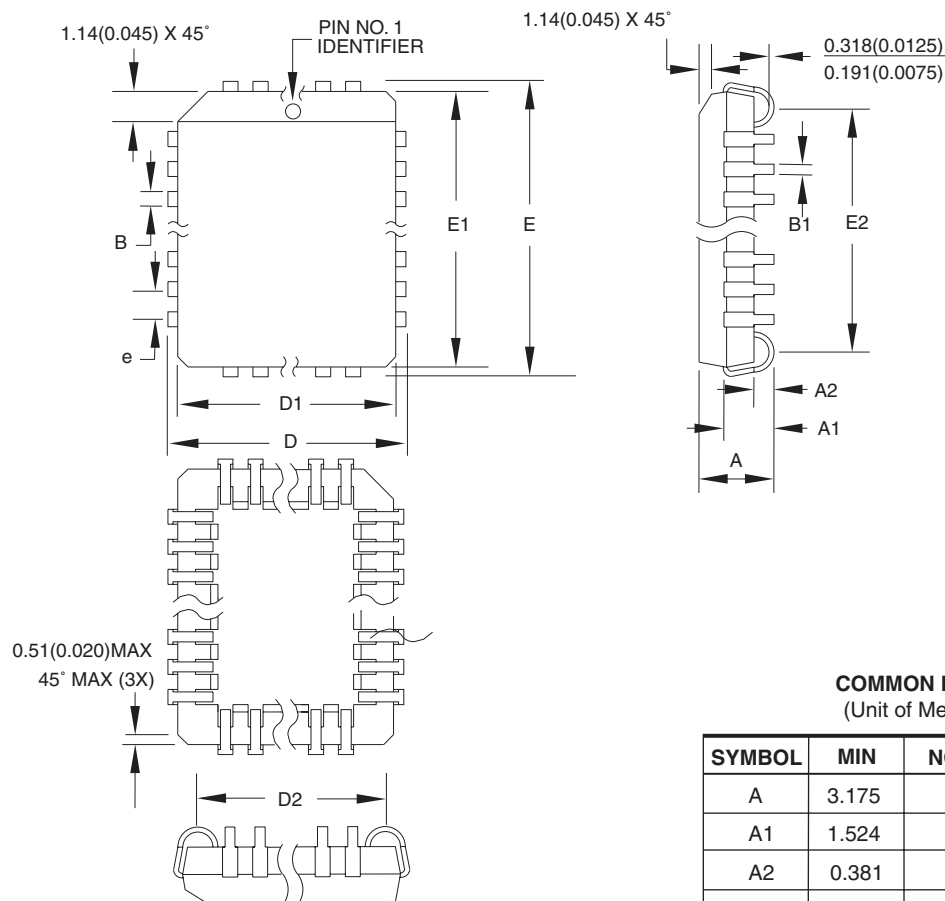
### 19.2 Green Package Option (Pb/Halide-free)

$t_{ACC}$ (ns)	$I_{CC}$ (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	30	0.1	AT27C040-70JU AT27C040-70PU AT27C040-70TU	32J 32P6 32T	Industrial (-40°C to 85°C)
90	30	0.1	AT27C040-90JU AT27C040-90PU AT27C040-90TU	32J 32P6 32T	Industrial (-40°C to 85°C)

Package Type	
<b>32J</b>	32-lead, Plastic J-leaded Chip Carrier (PLCC)
<b>32P6</b>	32-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
<b>32T</b>	32-lead, Plastic Thin Small Outline Package (TSOP)

## 20. Package Information

### 20.1 32J – PLCC



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)

**DRAWING NO.**

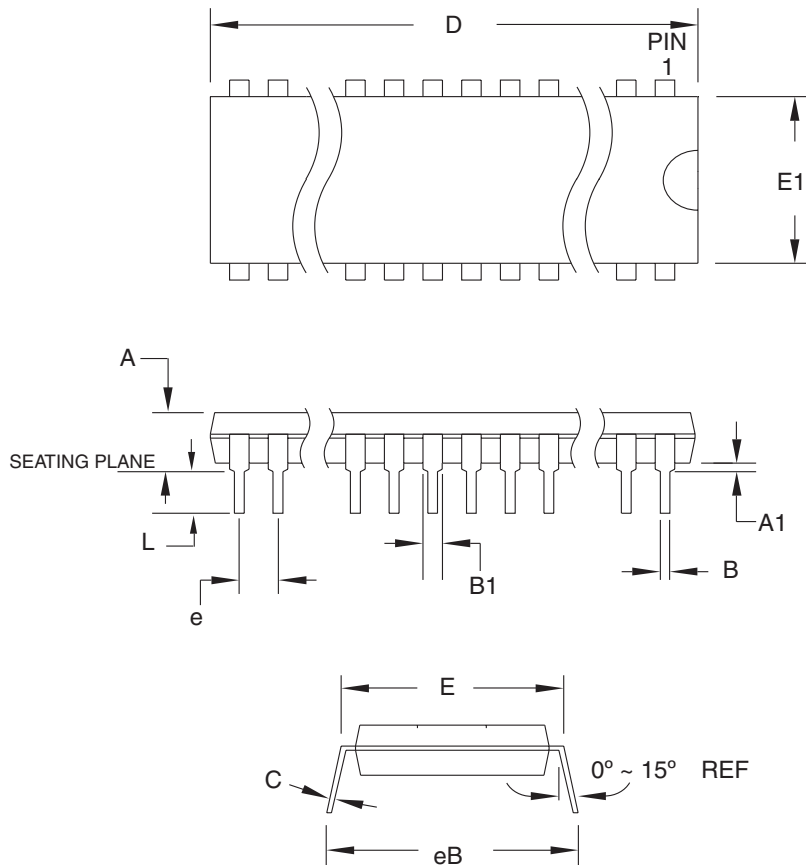
32J

**REV.**

B



## 20.2 32P6 – PDIP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	41.783	–	42.291	Note 1
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 1
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Note: 1. Dimensions D and E1 do not include mold Flash or Protrusion.  
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01



2325 Orchard Parkway  
San Jose, CA 95131

### TITLE

**32P6**, 32-lead (0.600"/15.24 mm Wide) Plastic Dual  
Inline Package (PDIP)

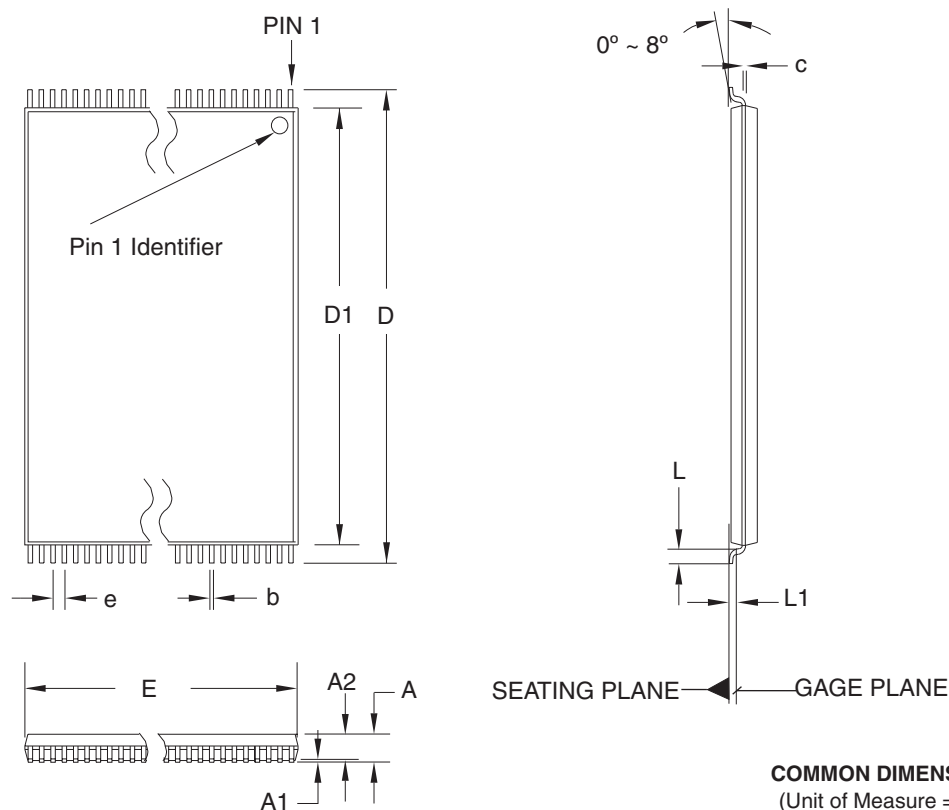
### DRAWING NO.

32P6

### REV.

B

## 20.3 32T – TSOP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	
A1	0.05	—	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	—	0.21	
e	0.50 BASIC			

- Notes:
1. This package conforms to JEDEC reference MO-142, Variation BD.
  2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
  3. Lead coplanarity is 0.10 mm maximum.

10/18/01



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**32T**, 32-lead (8 x 20 mm Package) Plastic Thin Small Outline  
Package, Type I (TSOP)

**DRAWING NO.**

32T

**REV.**

B



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Fax: (44) 1355-242-743

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