

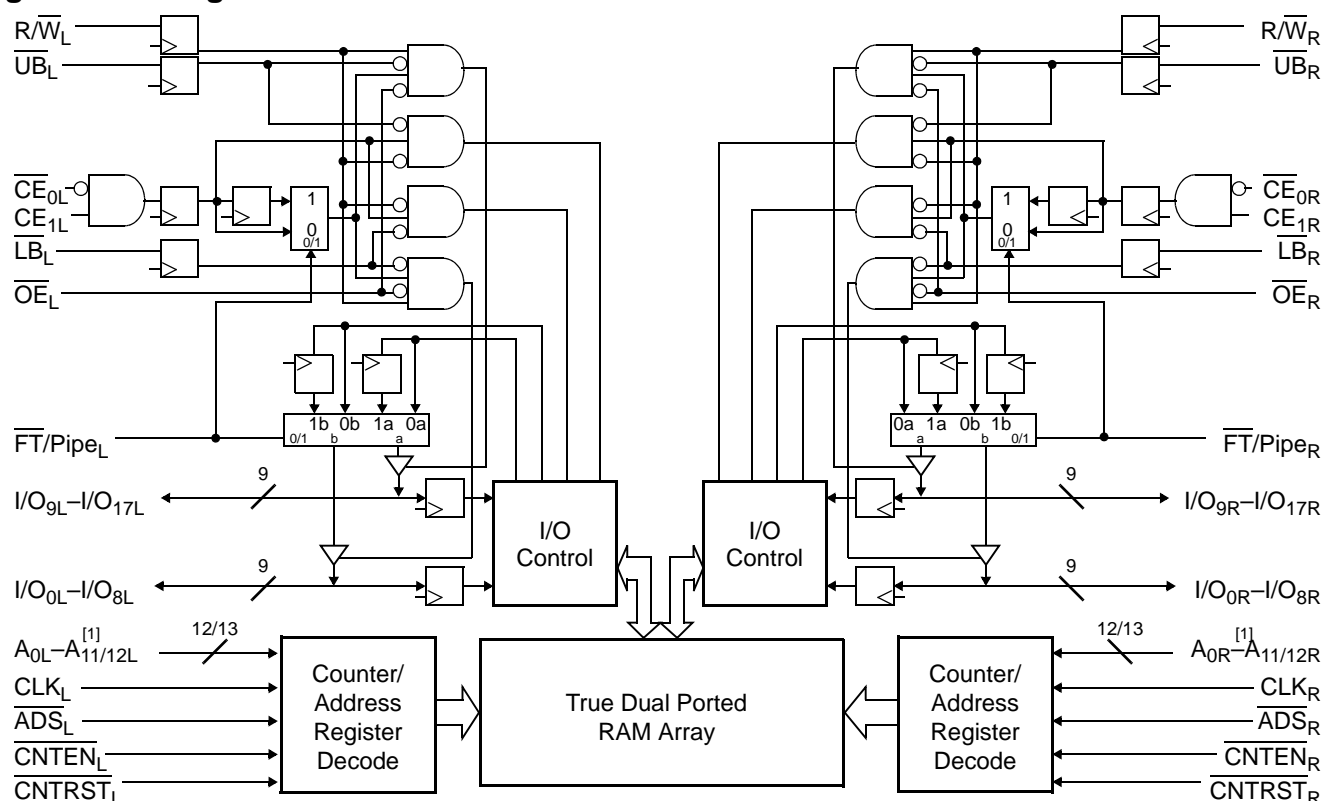
# 3.3 V 4 K/8 K × 18 Synchronous Dual Port Static RAM

## Features

- True dual ported memory cells which allow simultaneous access of the same memory location
- Two flow-through/pipelined devices
  - 4 K × 18 organization (CY7C09349AV)
  - 8 K × 18 organization (CY7C09359AV)
- Three modes
  - Flow-through
  - Pipelined
  - Burst
- Pipelined output mode on both ports allows fast 67-MHz operation
- 0.35-micron complementary metal oxide semiconductor (CMOS) for optimum speed/power
- High-speed clock to data access 9 and 12 ns (max)
- 3.3 V low operating power
  - Active = 135 mA (typical)
  - Standby = 10 μA (typical)
- Fully synchronous interface for easier operation
- Burst counters increment addresses internally
  - Shorten cycle times
  - Minimize bus noise
  - Supported in flow-through and pipelined modes
- Dual chip enables for easy depth expansion
- Upper and lower byte controls for bus matching
- Automatic power-down
- Available in 100-pin thin quad flat pack (TQFP)

For a complete list of related documentation, [click here](#).

## Logic Block Diagram



### Note

1. A<sub>0</sub>-A<sub>11</sub> for 4 K; A<sub>0</sub>-A<sub>12</sub> for 8 K devices.

## Functional Description

The CY7C09349AV and CY7C09359AV are high-speed 3.3 V synchronous CMOS 4 K and 8 K × 18 dual-port static RAMs. Two ports are provided, permitting independent, simultaneous access for reads and writes to any location in memory.<sup>[2]</sup> Registers on control, address, and data lines allow for minimal set-up and hold times. In pipelined output mode, data is registered for decreased cycle time. Clock to data valid  $t_{CD2} = 9$  ns (pipelined). Flow-through mode can also be used to bypass the pipelined output register to eliminate access latency. In flow-through mode data will be available  $t_{CD1} = 20$  ns after the address is clocked into the device. Pipelined output or flow-through mode is selected via the  $\overline{FT}/\text{Pipe}$  pin.

Each port contains a burst counter on the input address register. The internal write pulse width is independent of the LOW-to-HIGH transition of the clock signal. The internal write pulse is self-timed to allow the shortest possible cycle times.

A HIGH on  $\overline{CE}_0$  or LOW on  $CE_1$  for one clock cycle will power down the internal circuitry to reduce the static power consumption. The use of multiple chip enables allows easier banking of multiple chips for depth expansion configurations. In the pipelined mode, one cycle is required with  $\overline{CE}_0$  LOW and  $CE_1$  HIGH to reactivate the outputs.

Counter enable inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for fast interleaved memory applications. A port's burst counter is loaded with the port's address strobe (ADS). When the port's count enable (CNTEN) is asserted, the address counter will increment on each LOW-to-HIGH transition of that port's clock signal. This will read/write one word from/into each successive address location until CNTEN is deasserted. The counter can address the entire memory array and will loop back to the start. Counter reset (CNTRST) is used to reset the burst counter.

All parts are available in 100-pin thin quad plastic flatpack (TQFP) packages.

### Note

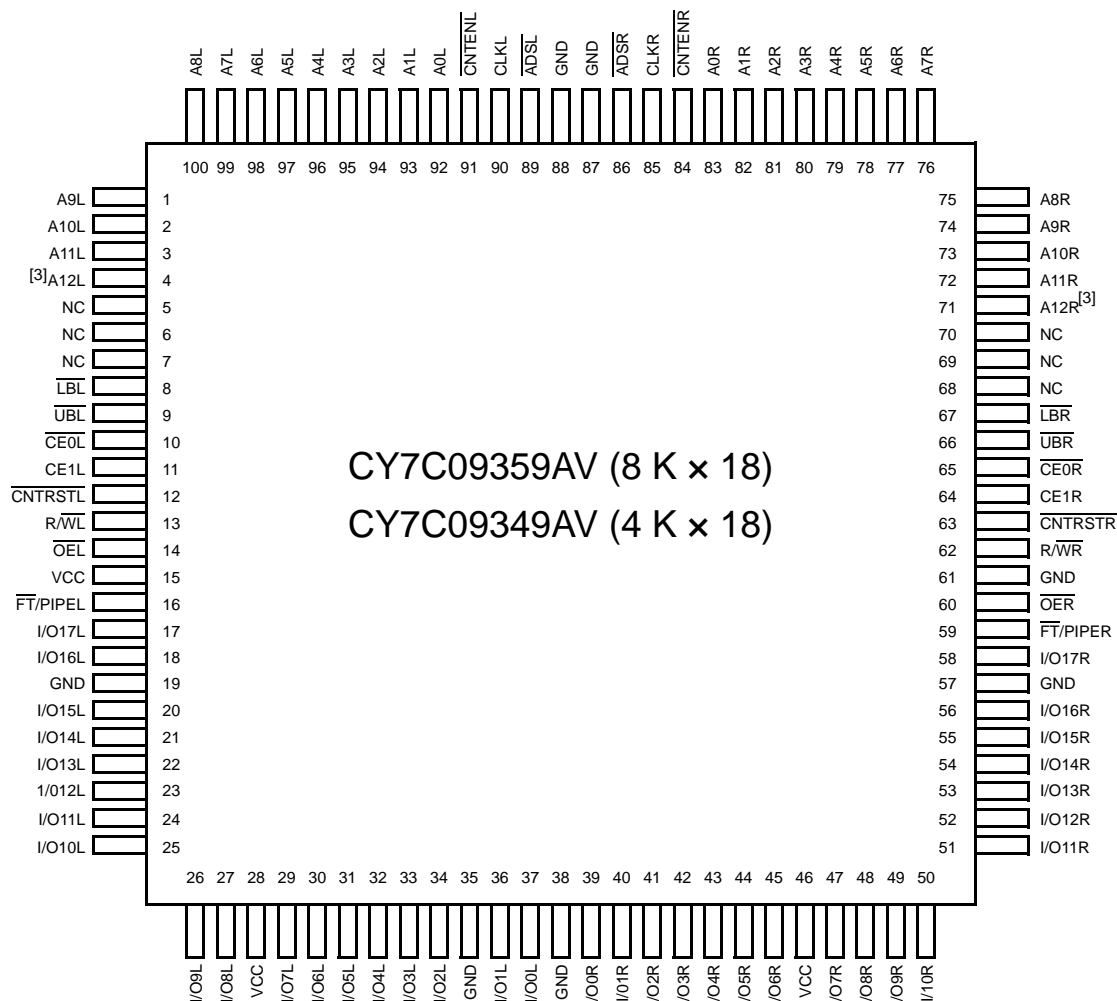
2. When simultaneously writing to the same location, final value cannot be guaranteed.

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## Pin Configuration

**Figure 1. 100-pin TQFP (Top View)**



## Selection Guide

	<b>CY7C09349AV</b> <b>CY7C09359AV</b> <b>-9</b>	<b>CY7C09349AV</b> <b>-12</b>
$f_{MAX2}$ (MHz) (pipelined)	67	50
Max access time (ns) (clock to data, pipelined)	9	12
Typical operating current $I_{CC}$ (mA)	135	115
Typical standby current for $I_{SB1}$ (mA) (both ports TTL level)	20	20
Typical standby current for $I_{SB3}$ ( $\mu$ A) (both ports CMOS level)	10	10

### Note

3. This pin is NC for CY7C09349AV.

## Pin Definitions

Left Port	Right Port	Description
A <sub>0L</sub> –A <sub>12L</sub>	A <sub>0R</sub> –A <sub>12R</sub>	Address inputs (A <sub>0</sub> –A <sub>11</sub> for 4 K, A <sub>0</sub> –A <sub>12</sub> for 8 K devices).
ADS <sub>L</sub>	ADS <sub>R</sub>	Address strobe input. Used as an address qualifier. This signal should be asserted LOW during normal read or write transactions. Asserting this signal LOW also loads the burst address counter with data present on the I/O pins.
CE <sub>0L</sub> , CE <sub>1L</sub>	CE <sub>0R</sub> , CE <sub>1R</sub>	Chip enable input. To select either the left or right port, both CE <sub>0</sub> and CE <sub>1</sub> must be asserted to their active states (CE <sub>0</sub> ≤ V <sub>IL</sub> and CE <sub>1</sub> ≥ V <sub>IH</sub> ).
CLK <sub>L</sub>	CLK <sub>R</sub>	Clock signal. This input can be free running or strobed. Maximum clock input rate is f <sub>MAX</sub> .
CNTEN <sub>L</sub>	CNTEN <sub>R</sub>	Counter enable input. Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK. CNTEN is disabled if ADS or CNTRST are asserted LOW.
CNTRST <sub>L</sub>	CNTRST <sub>R</sub>	Counter reset input. Asserting this signal LOW resets the burst address counter of its respective port to zero. CNTRST is not disabled by asserting ADS or CNTEN.
I/O <sub>0L</sub> –I/O <sub>17L</sub>	I/O <sub>0R</sub> –I/O <sub>17R</sub>	Data bus input/output (I/O <sub>0</sub> –I/O <sub>15</sub> for ×16 devices).
LB <sub>L</sub>	LB <sub>R</sub>	Lower byte select input. Asserting this signal LOW enables read and write operations to the lower byte (I/O <sub>0</sub> –I/O <sub>8</sub> for ×18, I/O <sub>0</sub> –I/O <sub>7</sub> for ×16) of the memory array. For read operations both the LB and OE signals must be asserted to drive output data on the lower byte of the data pins.
UB <sub>L</sub>	UB <sub>R</sub>	Upper byte select input. Same function as LB, but to the upper byte (I/O <sub>8/9L</sub> –I/O <sub>15/17L</sub> ).
OE <sub>L</sub>	OE <sub>R</sub>	Output enable input. This signal must be asserted LOW to enable the I/O data pins during read operations.
R/W <sub>L</sub>	R/W <sub>R</sub>	Read/write enable input. This signal is asserted LOW to write to the dual port memory array. For read operations, assert this pin HIGH.
FT/PIPE <sub>L</sub>	FT/PIPE <sub>R</sub>	Flow-through/pipelined select input. For flow-through mode operation, assert this pin LOW. For pipelined mode operation, assert this pin HIGH.
GND		Ground input.
NC		No connect.
V <sub>CC</sub>		Power input.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature..... –65 °C to +150 °C

Ambient temperature with power applied . –55 °C to +125 °C

Supply voltage to ground potential .....–0.5 V to +4.6 V

DC voltage applied to  
outputs in high Z state .....–0.5 V to V<sub>CC</sub> + 0.5 V

DC input voltage .....–0.5 V to V<sub>CC</sub> + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0 °C to +70 °C	3.3 V ± 300 mV
Industrial	–40 °C to +85 °C	3.3 V ± 300 mV

## Electrical Characteristics

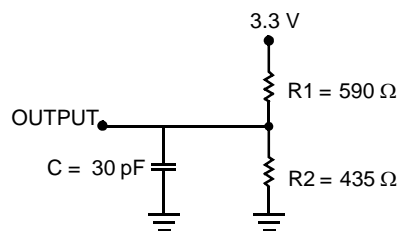
Over the Operating Range

Parameter	Description		CY7C09349AV CY7C09359AV						Unit	
			−9			−12				
			Min	Typ	Max	Min	Typ	Max		
V <sub>OH</sub>	Output HIGH voltage (V <sub>CC</sub> = Min, I <sub>OH</sub> = −4.0 mA)		2.4	−	−	2.4	−	−	V	
V <sub>OL</sub>	Output LOW voltage (V <sub>CC</sub> = Min, I <sub>OH</sub> = +4.0 mA)		−		0.4	−		0.4	V	
V <sub>IH</sub>	Input HIGH voltage		2.0		−	2.0		−	V	
V <sub>IL</sub>	Input LOW voltage		−		0.8	−		0.8	V	
I <sub>OZ</sub>	Output leakage current		−10		10	−10		10	μA	
I <sub>CC</sub>	Operating current (V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA) outputs disabled	Commercial	−	135	230	−	115	180	mA	
		Industrial		−			155	250	mA	
I <sub>SB1</sub>	Standby current (both ports TTL level) <sup>[4]</sup> CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>IH</sub> , f = f <sub>MAX</sub>			Commercial	20		75	20	70	mA
				Industrial	−		30	80	mA	
I <sub>SB2</sub>	Standby current (one port TTL level) <sup>[4]</sup> CE <sub>L</sub> or CE <sub>R</sub> ≥ V <sub>IH</sub> , f = f <sub>MAX</sub>			Commercial	95		155	85	140	mA
				Industrial	−		95	150	mA	
I <sub>SB3</sub>	Standby current (both ports CMOS level) <sup>[4]</sup> CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>CC</sub> − 0.2 V, f = 0			Commercial	10		500	10	500	μA
				Industrial	−		10	500	μA	
I <sub>SB4</sub>	Standby current (one port CMOS level) <sup>[4]</sup> CE <sub>L</sub> or CE <sub>R</sub> ≥ V <sub>IH</sub> , f = f <sub>MAX</sub>			Commercial	85		115	75	100	mA
				Industrial	−		85	110	mA	

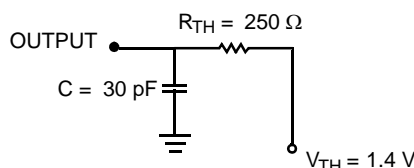
## Capacitance

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 3.3 V	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

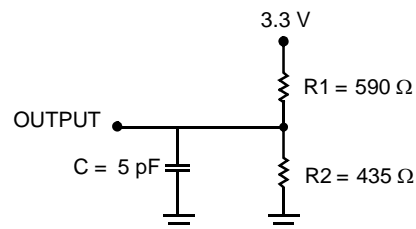
## AC Test Loads



(a) Normal Load (Load 1)



(b) Thévenin Equivalent (Load 1)



(c) Three-State Delay (Load 2)  
(Used for t<sub>CKLZ</sub>, t<sub>OLZ</sub>, & t<sub>OHZ</sub>  
including scope and jig)

### Note

4. CE<sub>L</sub> and CE<sub>R</sub> are internal signals. To select either the left or right port, both CE<sub>0</sub> AND CE<sub>1</sub> must be asserted to their active states (CE<sub>0</sub> ≤ V<sub>IL</sub> and CE<sub>1</sub> ≥ V<sub>IH</sub>).

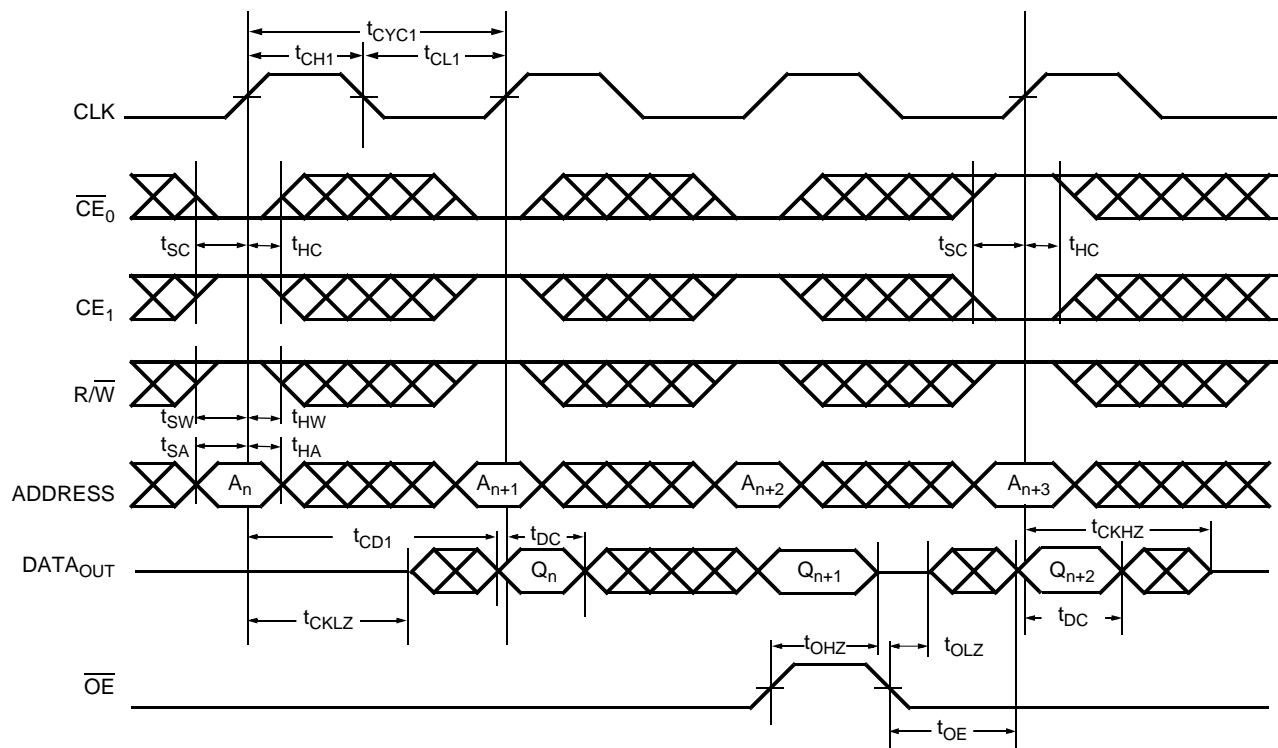
## Switching Characteristics

Over the Operating Range

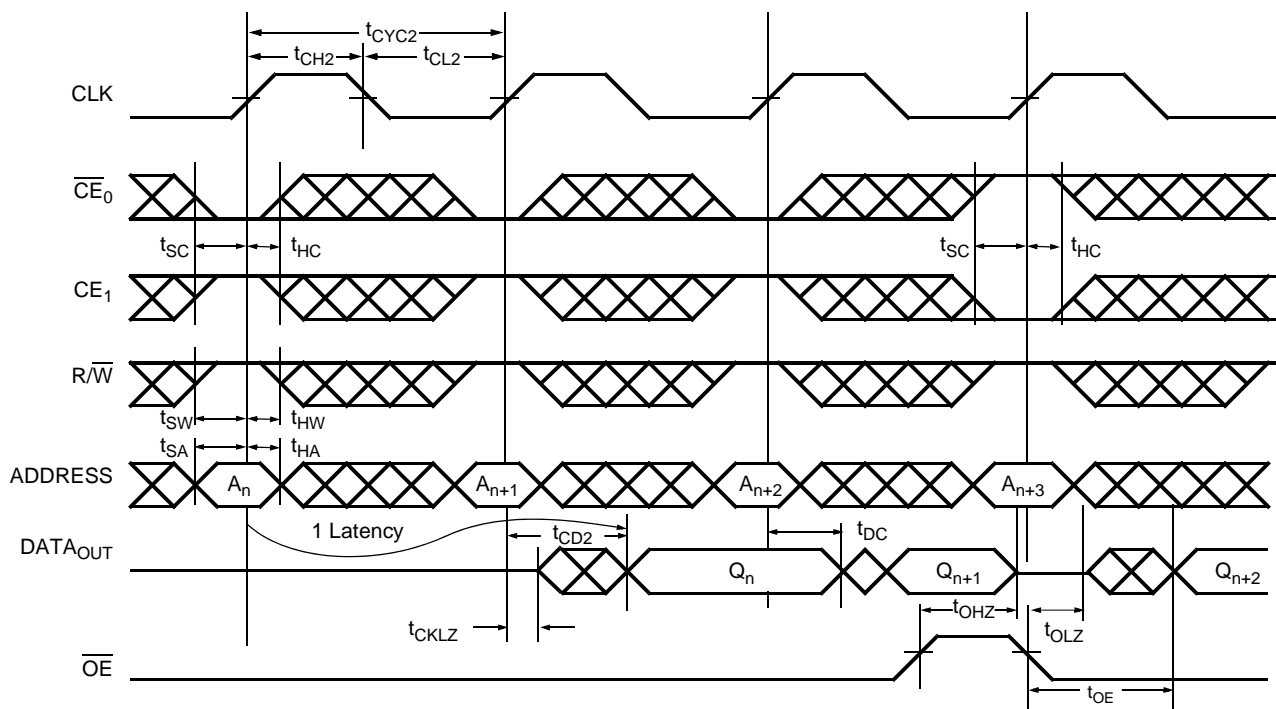
Parameter	Description	CY7C09349AV CY7C09359AV				Unit
		−9		−12		
		Min	Max	Min	Max	
f <sub>MAX1</sub>	f <sub>Max</sub> flow-through	–	40	–	33	MHz
f <sub>MAX2</sub>	f <sub>Max</sub> pipelined	–	67	–	50	MHz
t <sub>CYC1</sub>	Clock cycle time – flow-through	25	–	30	–	ns
t <sub>CYC2</sub>	Clock cycle time – pipelined	15	–	20	–	ns
t <sub>CH1</sub>	Clock HIGH time – flow-through	12	–	12	–	ns
t <sub>CL1</sub>	Clock LOW time – flow-through	12	–	12	–	ns
t <sub>CH2</sub>	Clock HIGH time – pipelined	6	–	8	–	ns
t <sub>CL2</sub>	Clock LOW time – pipelined	6	–	8	–	ns
t <sub>R</sub>	Clock rise time	–	3	–	3	ns
t <sub>F</sub>	Clock fall time	–	3	–	3	ns
t <sub>SA</sub>	Address set-up time	4	–	4	–	ns
t <sub>HA</sub>	Address hold time	1	–	1	–	ns
t <sub>SC</sub>	Chip enable set-up time	4	–	4	–	ns
t <sub>HC</sub>	Chip enable hold time	1	–	1	–	ns
t <sub>SW</sub>	R/ $\overline{W}$ set-up time	4	–	4	–	ns
t <sub>HW</sub>	R/ $\overline{W}$ hold time	1	–	1	–	ns
t <sub>SD</sub>	Input data set-up time	4	–	4	–	ns
t <sub>HD</sub>	Input data hold time	1	–	1	–	ns
t <sub>SAD</sub>	$\overline{ADS}$ set-up time	4	–	4	–	ns
t <sub>HAD</sub>	$\overline{ADS}$ hold time	1	–	1	–	ns
t <sub>SCN</sub>	$\overline{CNTEN}$ set-up time	4	–	4	–	ns
t <sub>HCN</sub>	$\overline{CNTEN}$ hold time	1	–	1	–	ns
t <sub>SRST</sub>	$\overline{CNTRST}$ set-up time	4	–	4	–	ns
t <sub>HRST</sub>	$\overline{CNTRST}$ hold time	1	–	1	–	ns
t <sub>OE</sub>	Output enable to data valid	–	10	–	12	ns
t <sub>OLZ</sub>	$\overline{OE}$ to low Z	2	–	2	–	ns
t <sub>OHZ</sub>	$\overline{OE}$ to high Z	1	7	1	7	ns
t <sub>CD1</sub>	Clock to data valid – flow-through	–	20	–	25	ns
t <sub>CD2</sub>	Clock to data valid – pipelined	–	9	–	12	ns
t <sub>DC</sub>	Data output hold after clock HIGH	2	–	2	–	ns
t <sub>CKHZ</sub>	Clock HIGH to output high Z	2	9	2	9	ns
t <sub>CKLZ</sub>	Clock HIGH to output low Z	2	–	2	–	ns
Port to port delays						
t <sub>CWDD</sub>	Write port clock HIGH to read data delay	–	40	–	40	ns
t <sub>CCS</sub>	Clock to clock set-up time	–	15	–	15	ns

## Switching Waveforms

**Figure 2. Read Cycle for Flow-through Output ( $\overline{\text{FT/PIPE}} = V_{\text{IL}}$ )**<sup>[5, 6, 7, 8]</sup>



**Figure 3. Read Cycle for Pipelined Operation ( $\overline{\text{FT/PIPE}} = V_{\text{IH}}$ )**<sup>[5, 6, 7, 8]</sup>



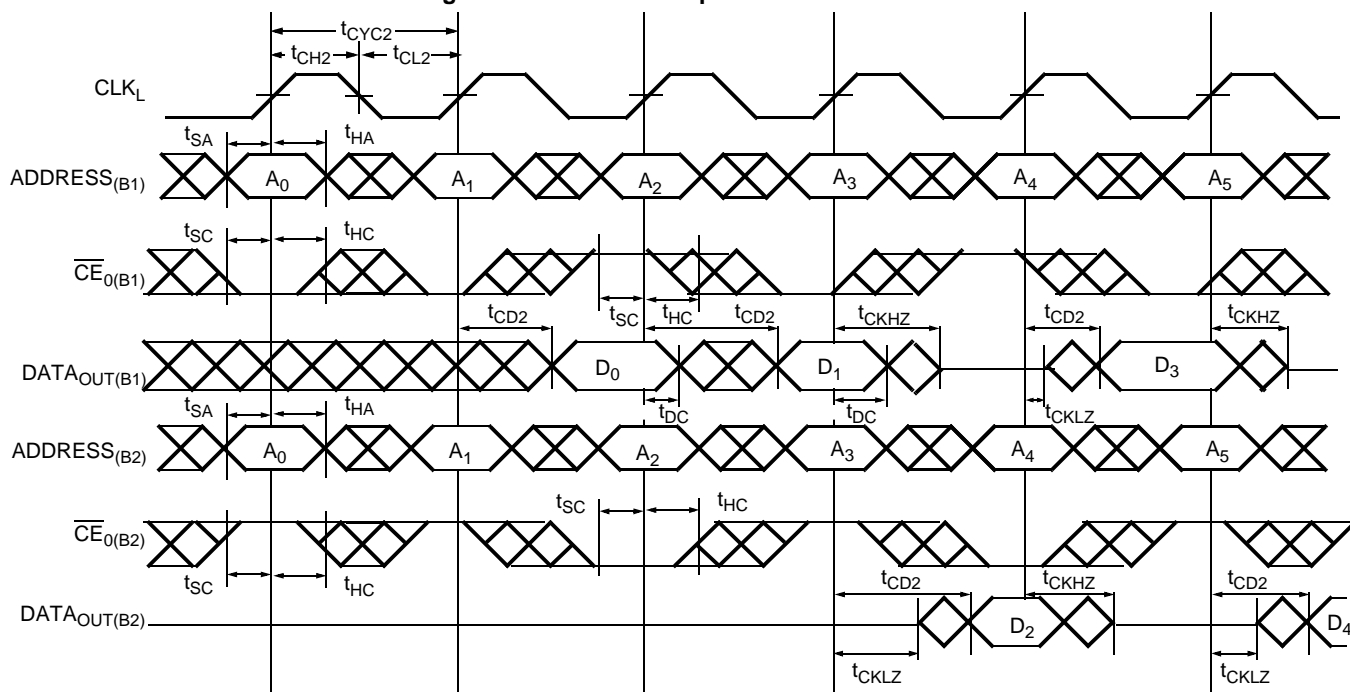
### Notes

5.  $\overline{\text{OE}}$  is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
6.  $\text{ADS} = V_{\text{IL}}$ ,  $\text{CNTEN}$  and  $\text{CNTRST} = V_{\text{IH}}$ .
7. The output is disabled (high-impedance state) by  $\overline{\text{CE}}_0 = V_{\text{IH}}$  or  $\text{CE}_1 = V_{\text{IL}}$  following the next rising edge of the clock.
8. Addresses do not have to be accessed sequentially since  $\text{ADS} = V_{\text{IL}}$  constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

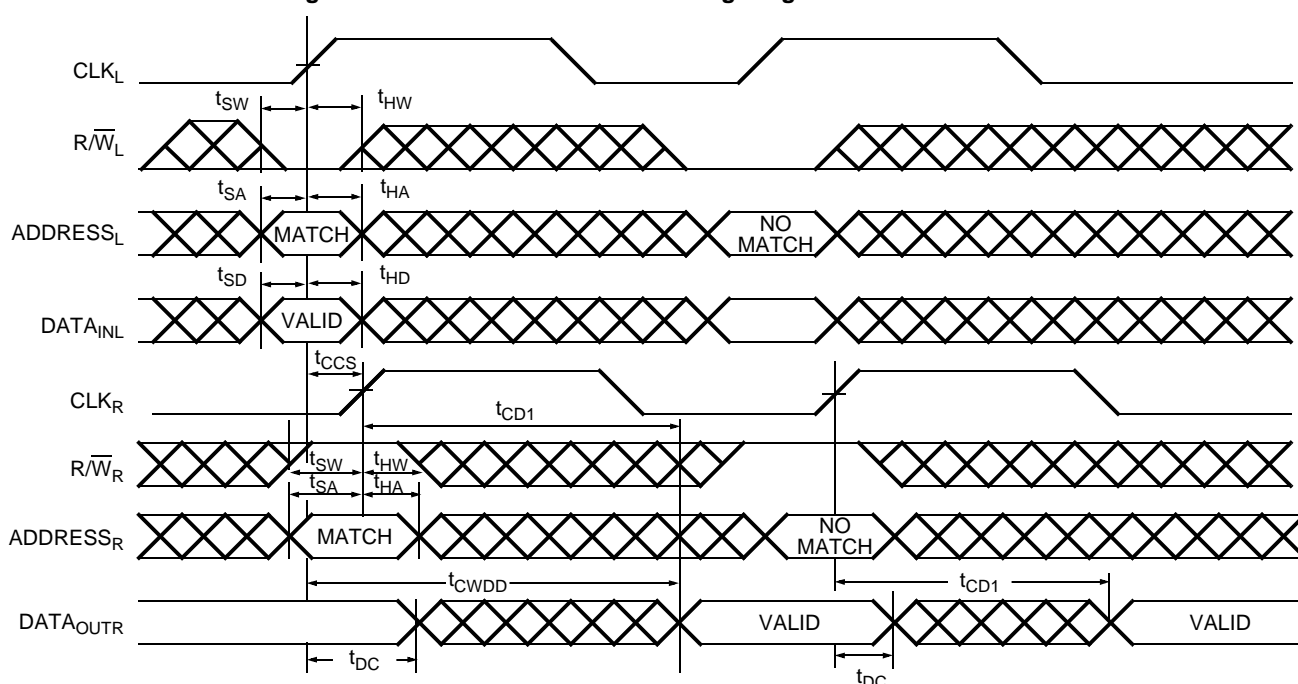


## Switching Waveforms (continued)

**Figure 4. Bank Select Pipelined Read**<sup>[9, 10]</sup>



**Figure 5. Left Port Write to Flow-through Right Port Read**<sup>[11, 12, 13, 14]</sup>



### Notes

9. In this depth expansion example, B1 represents Bank #1 and B2 is Bank #2; Each bank consists of one Cypress dual-port device from this data sheet.
10.  $\overline{UB}$ ,  $\overline{LB}$ ,  $\overline{OE}$  and  $\overline{ADS} = V_{IL}$ ;  $\overline{CE}_{1(B1)}$ ,  $\overline{CE}_{1(B2)}$ ,  $\overline{R/W}$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST} = V_{IH}$ .
11. The same waveforms apply for a right port write to flow-through left port read.
12.  $\overline{CE}_0$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and  $\overline{ADS} = V_{IL}$ ;  $\overline{CE}_1$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST} = V_{IH}$ .
13.  $\overline{OE} = V_{IL}$  for the right port, which is being read from.  $\overline{OE} = V_{IH}$  for the left port, which is being written to.
14. If  $t_{CCS} \leq$  maximum specified, then data from right port READ is not valid until the maximum specified for  $t_{CWDD}$ . If  $t_{CCS} >$  maximum specified, then data is not valid until  $t_{CCS} + t_{CD1}$ .  $t_{CWDD}$  does not apply in this case.

## Switching Waveforms (continued)

Figure 6. Pipelined Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>[15, 16, 17, 18]</sup>

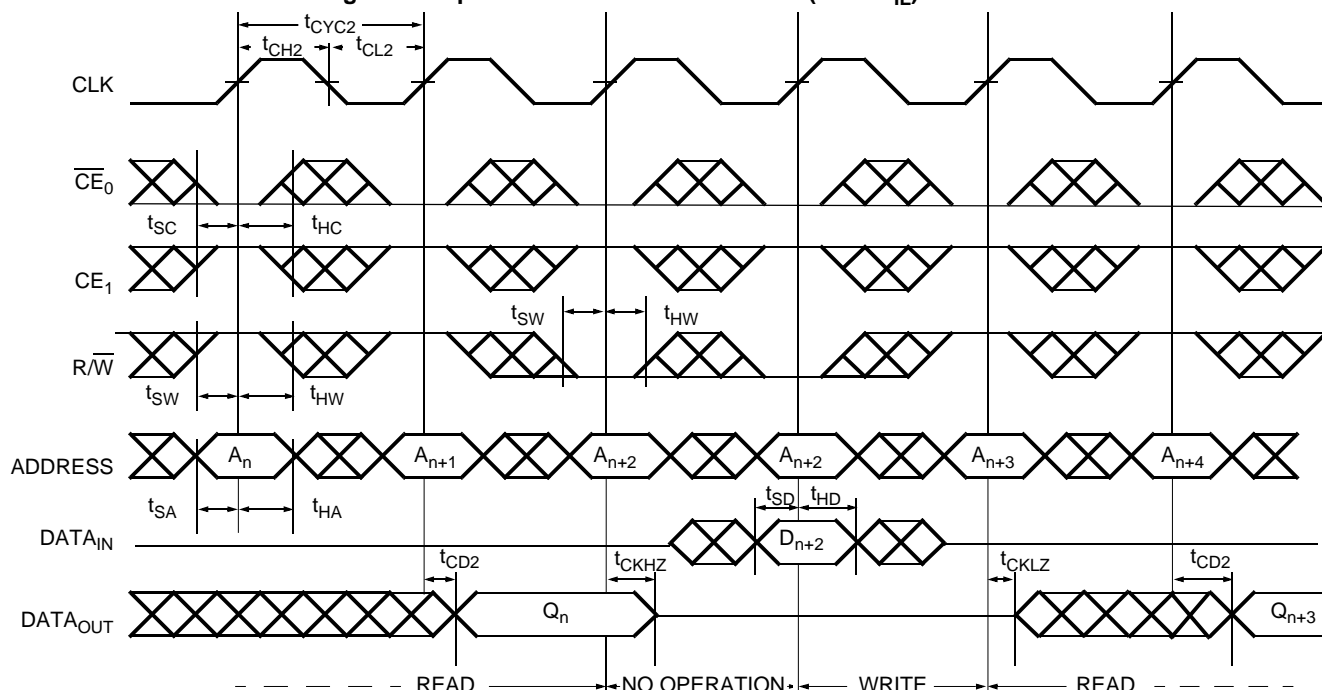
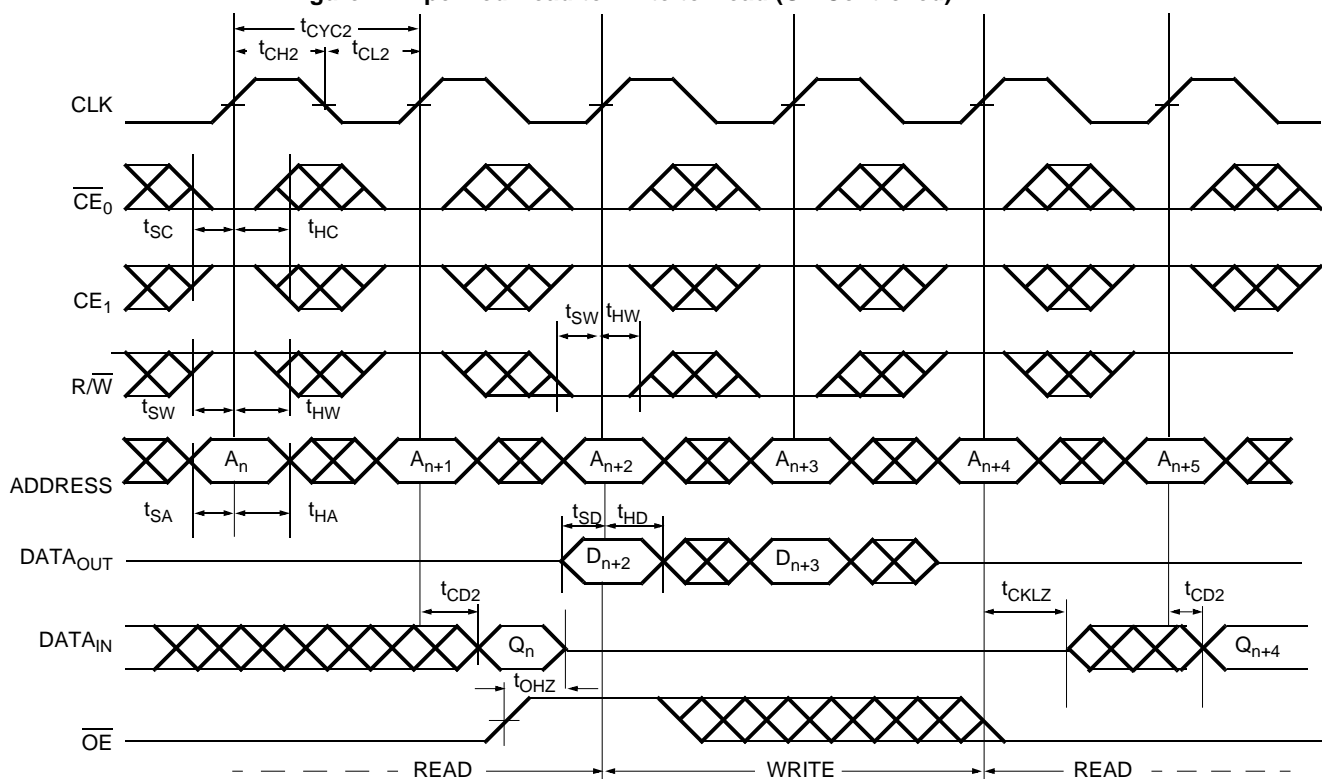


Figure 7. Pipelined Read-to-Write-to-Read (OE Controlled)<sup>[15, 16, 17, 18]</sup>



### Notes

15. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
16. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
17.  $\overline{CE}_0$  and  $\overline{ADS} = V_{IL}$ ;  $\overline{CE}_1$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST} = V_{IH}$ .
18. During "No operation", data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.

## Switching Waveforms (continued)

Figure 8. Flow-through Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>[19, 20, 22, 23]</sup>

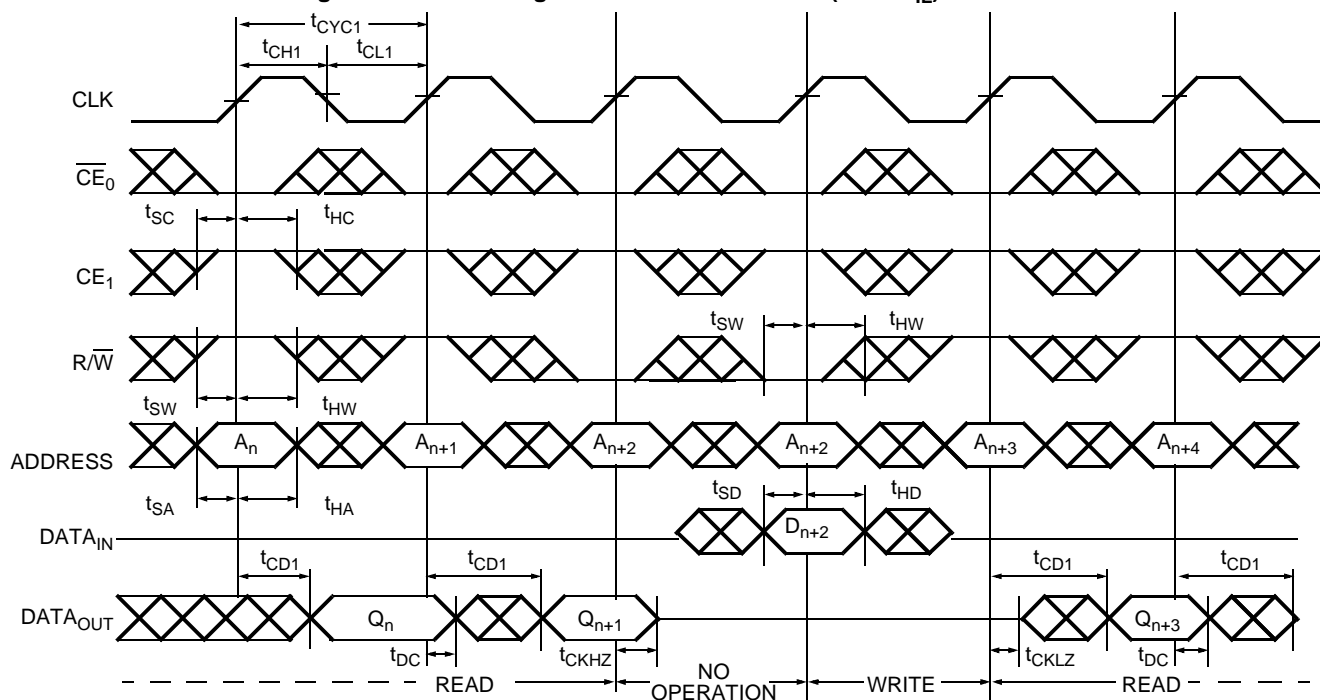
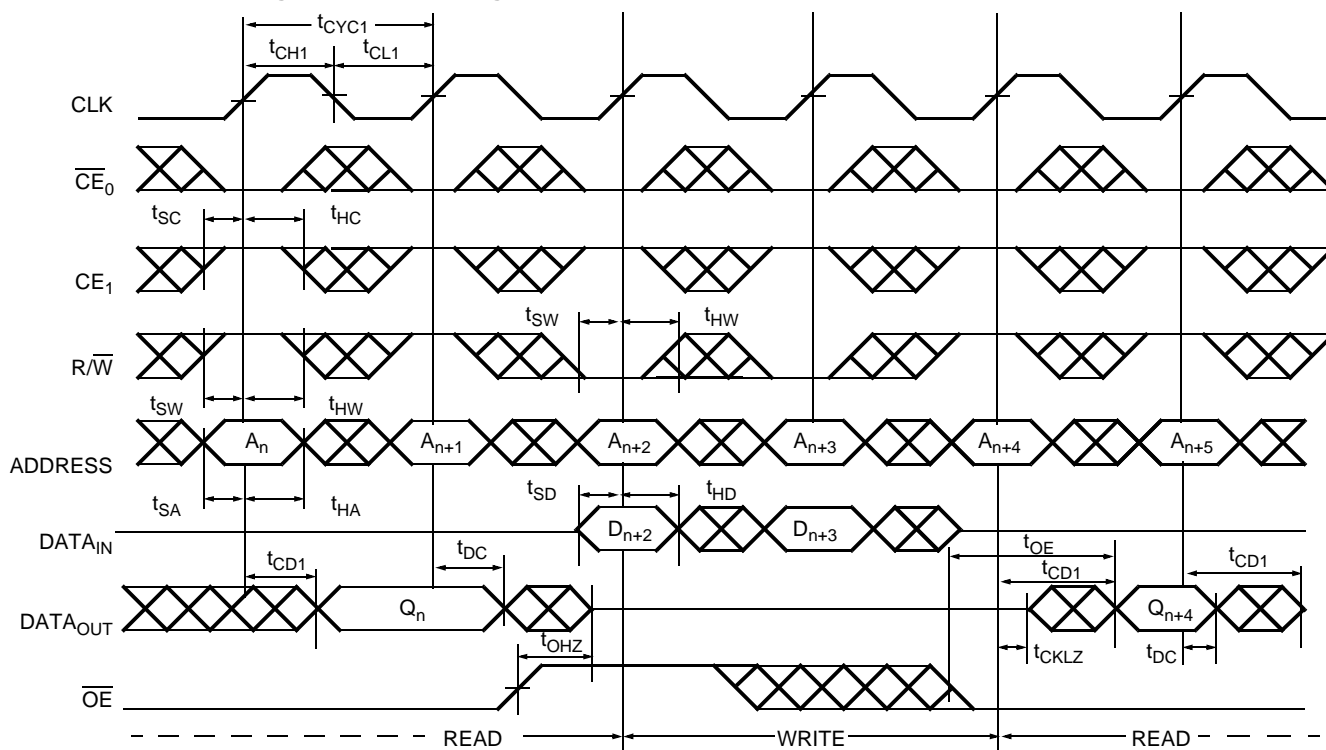


Figure 9. Flow-through Read-to-Write-to-Read (OE Controlled)<sup>[19, 20, 21, 22, 23]</sup>



### Notes

19.  $ADS = V_{IL}$ ,  $\overline{CNTEN}$  and  $\overline{CNTRST} = V_{IH}$ .
20. Addresses do not have to be accessed sequentially since  $ADS = V_{IL}$  constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
21. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
22.  $\overline{CE}_0$  and  $ADS = V_{IL}$ ;  $\overline{CE}_1$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST} = V_{IH}$ .
23. During "No operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.

## Switching Waveforms (continued)

Figure 10. Pipelined Read with Address Counter Advance<sup>[24]</sup>

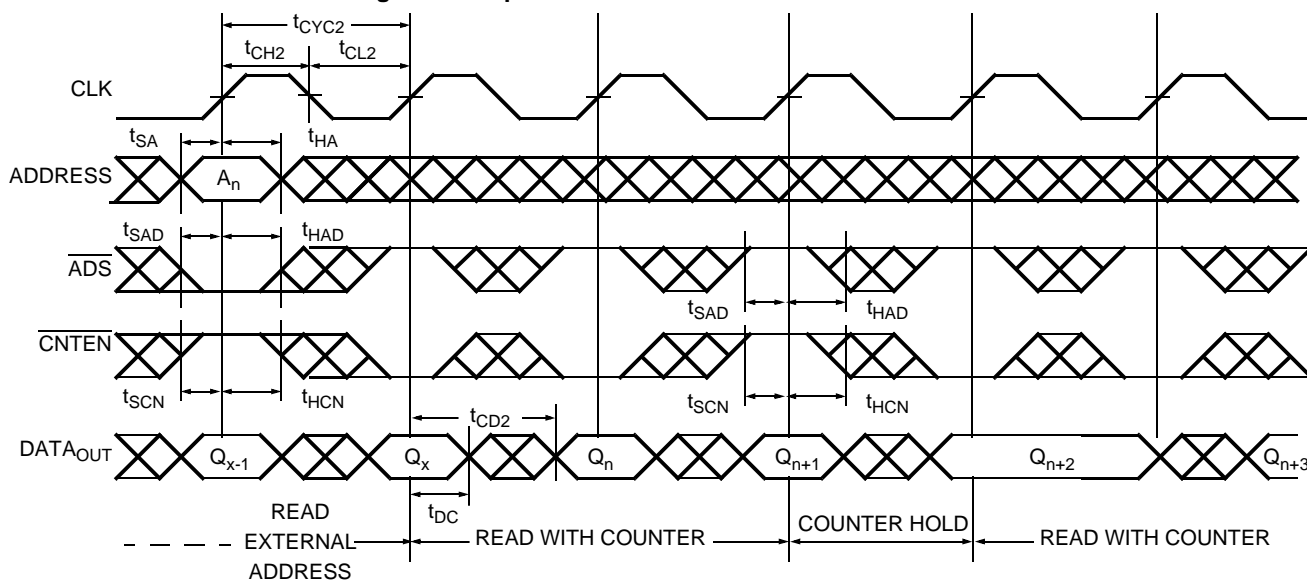
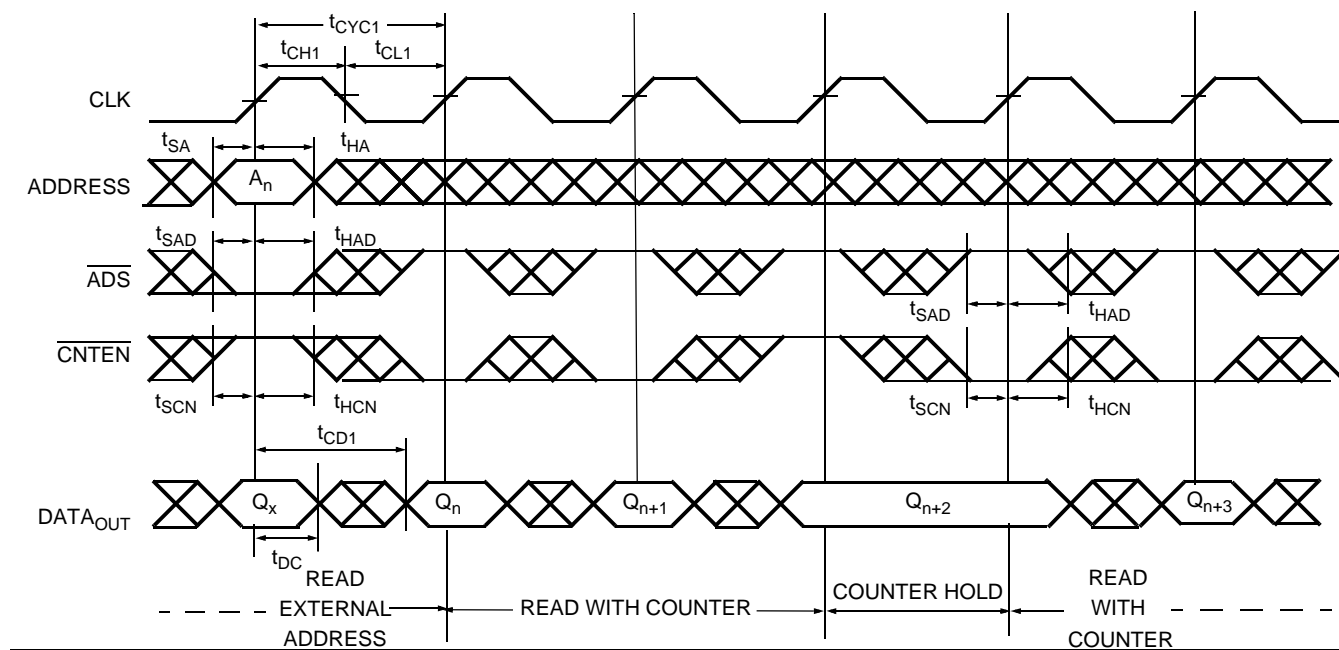


Figure 11. Flow-through Read with Address Counter Advance<sup>[24]</sup>

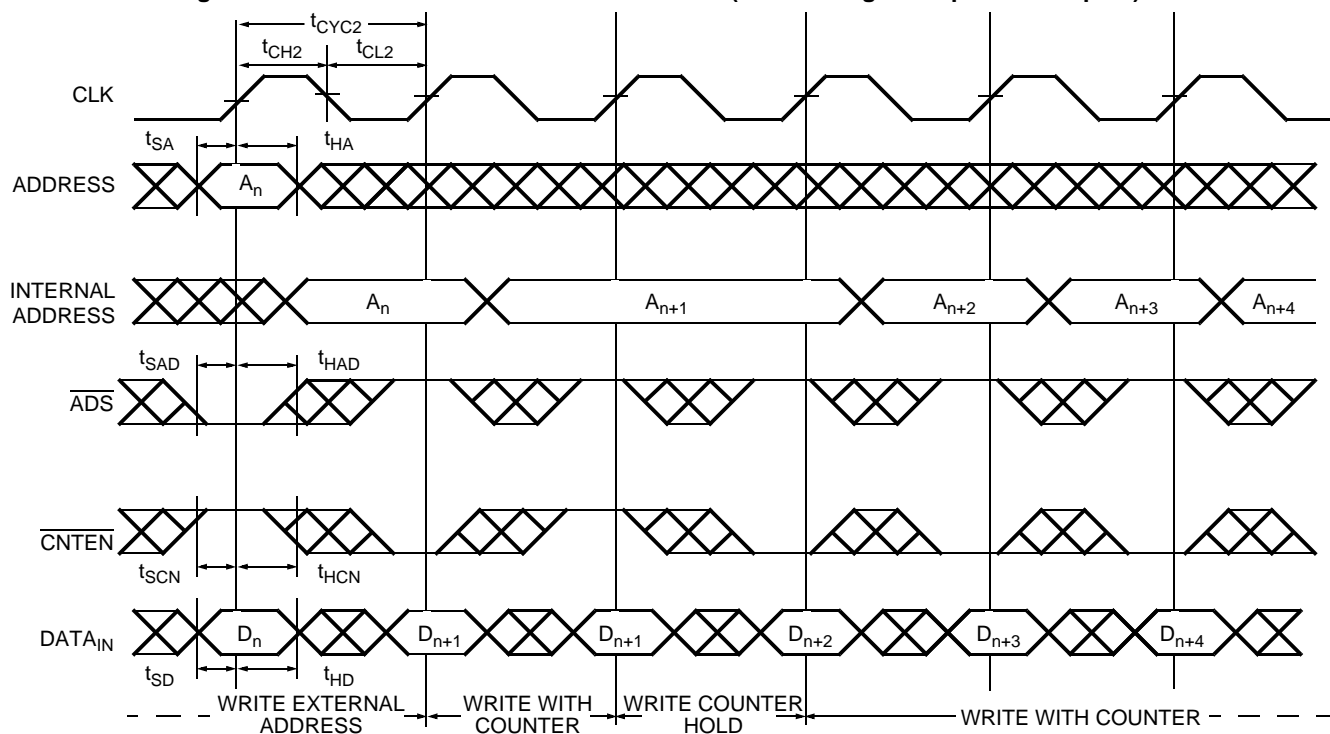


### Note

24.  $\overline{CE_0}$  and  $\overline{OE} = V_{IL}$ ;  $CE_1$ ,  $R/\overline{W}$  and  $\overline{CNTRST} = V_{IH}$ .

## Switching Waveforms (continued)

**Figure 12. Write with Address Counter Advance (Flow-through or Pipelined Outputs)<sup>[25, 26]</sup>**



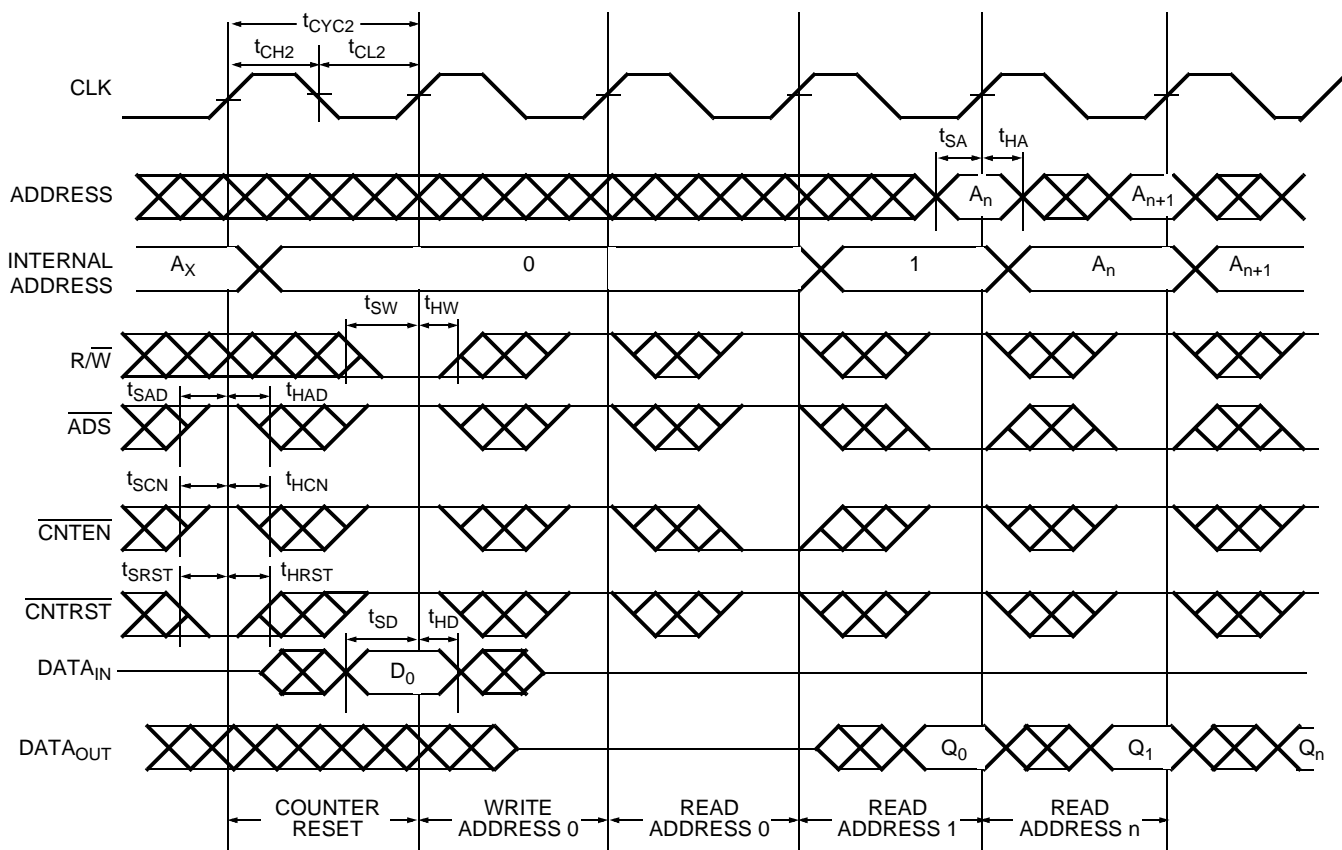
### Notes

25.  $\overline{CE_0}$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and  $R/\overline{W} = V_{IL}$ ;  $CE_1$  and  $\overline{CNTST} = V_{IH}$ .

26. The "Internal Address" is equal to the "External Address" when  $\overline{ADS} = V_{IL}$  and equals the counter output when  $\overline{ADS} = V_{IH}$ .

## Switching Waveforms (continued)





Figure 13. Counter Reset (Pipelined Outputs)<sup>[27, 28, 29, 30]</sup>







### Notes

27. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
28. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
29.  $\overline{CE}_0$ ,  $\overline{UB}$ , and  $\overline{LB} = V_{IL}$ ;  $CE_1 = V_{IH}$ .
30. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset.

## Read/Write and Enable Operation<sup>[31, 32, 33]</sup>

Inputs					Outputs	Operation
OE	CLK	CE <sub>0</sub>	CE <sub>1</sub>	R/W	I/O <sub>0</sub> –I/O <sub>17</sub>	
X		H	X	X	High Z	Deselected <sup>[34]</sup>
X		X	L	X	High Z	Deselected <sup>[34]</sup>
X		L	H	L	D <sub>IN</sub>	Write
L		L	H	H	D <sub>OUT</sub>	Read <sup>[34]</sup>
H	X	L	H	X	High Z	Outputs disabled

## Address Counter Control Operation<sup>[31, 35, 36, 37]</sup>

Address	Previous Address	CLK	ADS	CNTEN	CNTRST	I/O	Mode	Operation
X	X		X	X	L	D <sub>out(0)</sub>	Reset	Counter reset to address 0
A <sub>n</sub>	X		L	X	H	D <sub>out(n)</sub>	Load	Address load into counter
X	A <sub>n</sub>		H	H	H	D <sub>out(n)</sub>	Hold	External address blocked—counter disabled
X	A <sub>n</sub>		H	L	H	D <sub>out(n+1)</sub>	Increment	Counter enabled—internal address generation

### Notes

31. "X" = "Don't Care," "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>.

32. ADS, CNTEN, CNTRST = "Don't Care."

33. OE is an asynchronous input signal.

34. When CE changes state in the pipelined mode, deselection and read happen in the following clock cycle.

35. CE<sub>0</sub> and OE = V<sub>IL</sub>; CE<sub>1</sub> and R/W = V<sub>IH</sub>.

36. Data shown for flow-through mode; pipelined mode output will be delayed by one cycle.

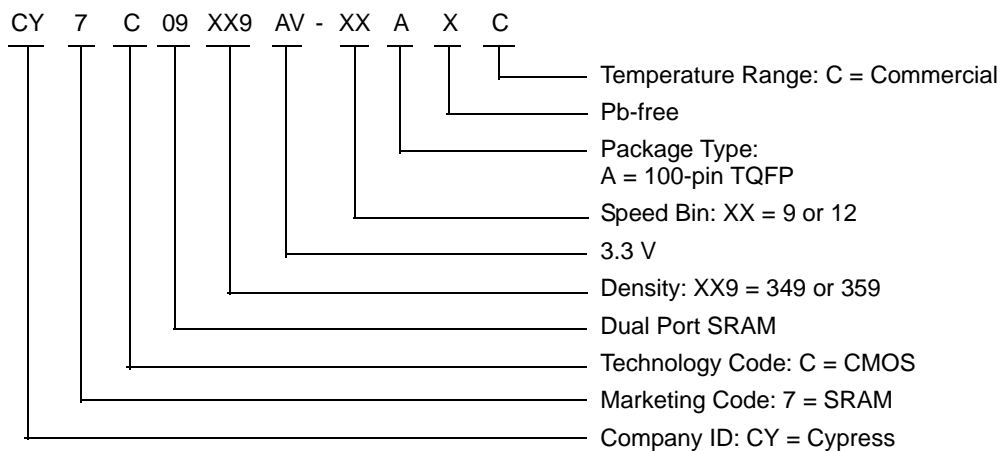
37. Counter operation is independent of CE<sub>0</sub> and CE<sub>1</sub>.

## Ordering Information

### 4 K × 18 3.3 V Synchronous Dual-Port SRAM

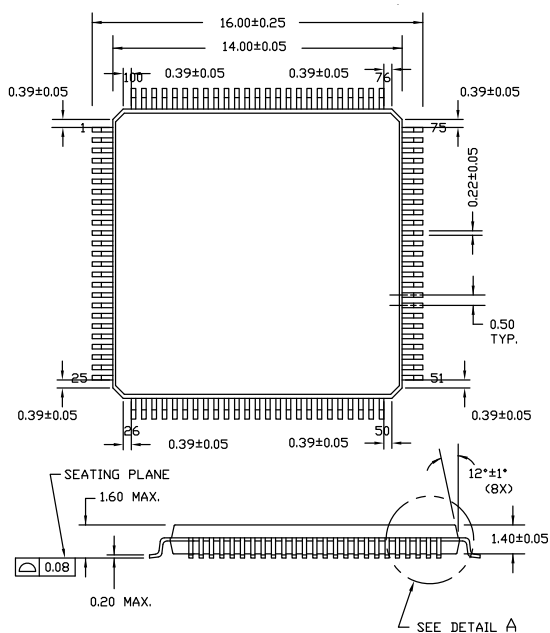
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
9	CY7C09349AV-9AXC	A100	100-pin Pb-free Thin Quad Flat Pack	Commercial
12	CY7C09349AV-12AXC	A100	100-pin Pb-free Thin Quad Flat Pack	Commercial

### Ordering Code Definitions



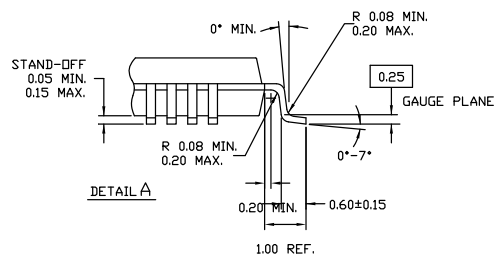


**Figure 14. 100-pin TQFP (14 x 14 x 1.4 mm) A100SA Package Outline, 51-85048**



**NOTE:**

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE  
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS



NOTE: PKG. CAN HAVE



OR



TOP LEFT CORNER CHAMFER

#### 4 CORNERS CHAMFER

51-85048 \*I

## Acronyms

Acronym	Description
CE	chip enable
CLK	clock
CMOS	complementary metal oxide semiconductor
I/O	Input/output
OE	output enable
SRAM	static random access memory
TQFP	thin quad flat pack

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microamperes
mA	milliamperes
mV	millivolts
mW	milliwatts
ns	nanoseconds
pF	picofarad
V	volts
W	watts

## Document History Page

Document Title: CY7C09349AV/CY7C09359AV, 3.3 V 4 K/8 K x 18 Synchronous Dual Port Static RAM Document Number: 001-63888				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	2998931	09/16/2010	RAME	New data sheet.
*A	3386551	09/28/2011	ADMU	Updated footnotes. Updated <a href="#">Package Diagram</a> .
*B	4547288	10/21/2014	ADMU	Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Package Diagram</a> : spec 51-85048 – Changed revision from *E to *I. Updated to new template.
*C	4580426	11/25/2014	ADMU	Added related documentation hyperlink in page 1.

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