

AN1082, AN1082S, AN6581

Dual J-FET Input Operational Amplifiers

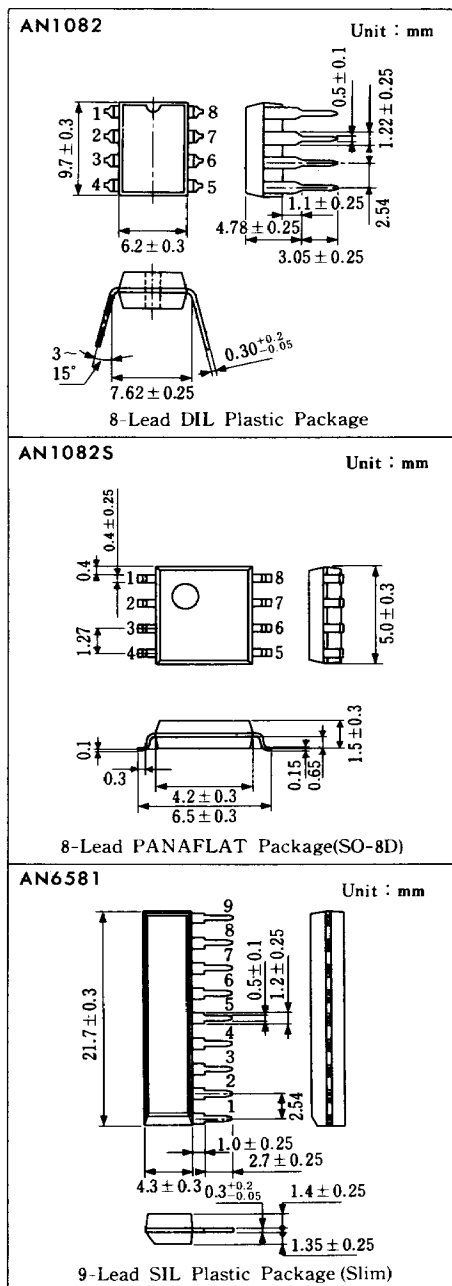
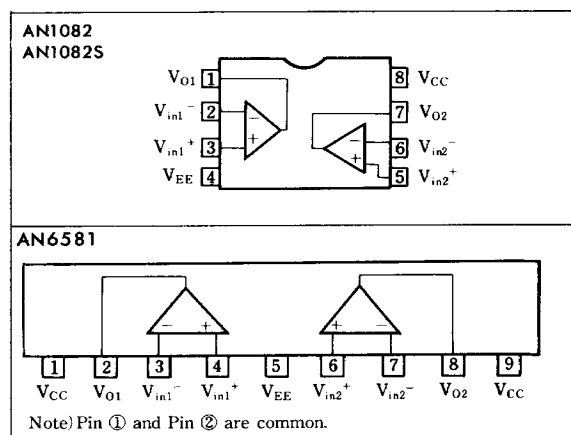
■ Outline

The AN1082, the AN1082S and the AN6581 are dual operational amplifiers with input stages consisting of Pch J-FET adopting the ion implantation process, realizing high speed response, high input impedance and low input bias current. Therefore, they can be applied widely to general control equipment and medical equipment such as integrators, sample & hold circuits and high input impedance buffers.

■ Features

- High slew rate : $SR=11V/\mu s$ typ.
- Low input bias current : $I_{bias}=30pA$ typ.
- Low offset current : $I_{io}=5pA$ typ.
- High impedance : $10^{12}\Omega$
- High gain : $G_v=106dB$ typ.
- Wide range of supply voltage : $\pm 5V \sim \pm 18V$
- Built-in phase compensation circuit

■ Block Diagrams



■ Pin

<AN1082, AN1082S>

Pin No.	Pin Name
1	Ch. 1 Output
2	Ch. 1 Invert Input
3	Ch. 1 Non Invert Input
4	V _{EE}
5	Ch. 2 Non Invert Input
6	Ch. 2 Invert Input
7	Ch. 2 Output
8	V _{CC}

<AN6581>

Pin No.	Pin Name
1	V _{CC}
2	Ch. 1 Output
3	Ch. 1 Invert Input
4	Ch. 1 Non Invert Input
5	V _{EE}
6	Ch. 2 Non Invert Input
7	Ch. 2 Invert Input
8	Ch. 2 Output
9	V _{CC}

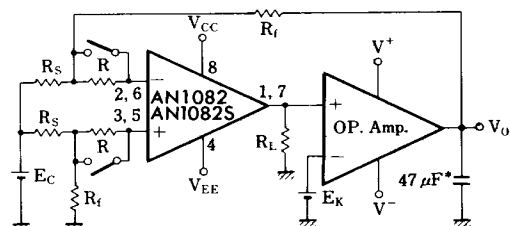
■ Absolute Maximum Ratings (Ta=25°C)

Item		Symbol	Rating	Unit
Voltage	Supply Voltage	V _{CC}	±18	V
	Differential Input Voltage	V _{ID}	±30	V
	Common-Mode Input Voltage	V _{ICM}	±15	V
Power Dissipation	AN1082, AN6581	P _D	500	mW
	AN1082S		360	
Operating Ambient Temperature		T _{opr}	-20 ~ +75	°C
Storage Temperature	AN1082, AN6581	T _{stg}	-55 ~ +150	°C
	AN1082S		-55 ~ +125	

■ Electrical Characteristics (V_{CC}=15V, V_{EE}= -15V, Ta=25°C)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Input Offset Voltage	V _{I(offset)}	1	R _S ≤ 50Ω		2	10	mV
Input Offset Current	I _{IO}	1			5	200	pA
Input Bias Current	I _{Bias}	1			30	400	pA
Voltage Gain	G _V	1		88	106		dB
Maximum Output Voltage	V _{O(max.)}	2	R _L ≥ 10kΩ	±12	±13.5		V
Maximum Output Voltage	V _{O(max.)}	2	R _L ≥ 2kΩ	±10	±12		V
Common-Mode Input Voltage Range	V _{CM}	3		±10			V
Common-Mode Rejection Ratio	CMR	1		70	76		dB
Supply Voltage Rejection Ratio	SVR	1		70	76		dB
Power Consumption	P _C	4	R _L = ∞		120	168	mW
Slew Rate	SR	5	R _L ≥ 2kΩ		11		V/μs
Unity-gain Band Width	f _(T)	6	A _v = 1		3		MHz
Equivalent Input Noise Voltage	V _{ni}	7	R _S = 100Ω, B = 10Hz ~ 30kHz		4		μV _{rms}

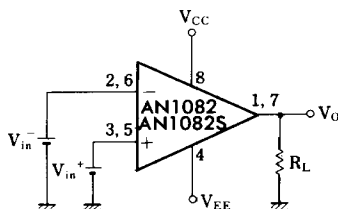
Test Circuit 1 ($V_{I(offset)}$, I_{IO} , I_{Bias} , G_V , CMR , SVR)



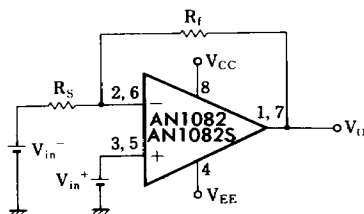
*Bipolar should be used (NP).

Note) For the connection method of the AN6581, see the block diagram.

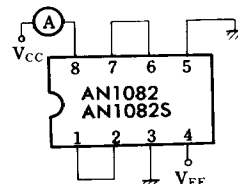
Test Circuit 2 ($V_{O(max)}$)



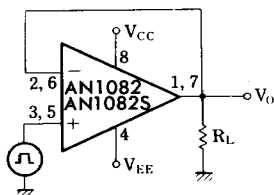
Test Circuit 3 (V_{CM})



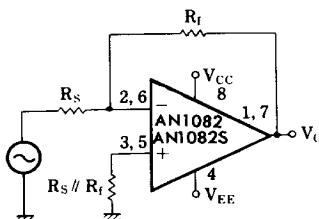
Test Circuit 4 (P_C)



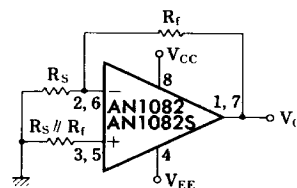
Test Circuit 5 (SR)



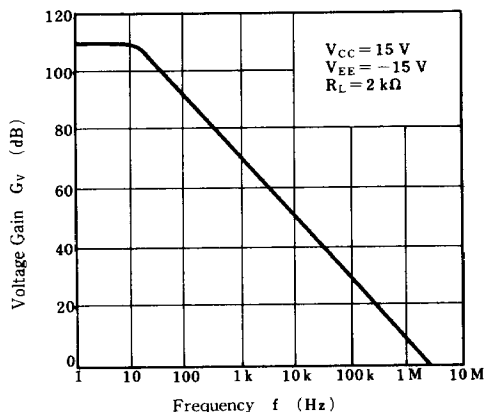
Test Circuit 6 ($f_{(T)}$)



Test Circuit 7 (V_{ni})



$G_V - f$



$V_{O(max)} - f$

