

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

DESCRIPTION

These are single-chip 16-bit microcomputers designed with high-performance CMOS silicon gate technology, including the internal flash memory and, being packaged in 64-pin plastic molded QFP or shrink plastic molded DIP. These microcomputers support the 7900 Series instruction set, which are enhanced and expanded instruction set and are upper-compatible with the 7700/7751 Series instruction set. The CPU of these microcomputers is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. Also, the bus interface unit of these microcomputers enhances the memory access efficiency to execute instructions fast. Therefore, these microcomputers are suitable for office, business, and industrial equipment controller that require high-speed processing of large data. Also, they are suitable for motor-control equipment since each of them includes the motor control circuit.

For the internal flash memory, single-power-supply programming and erasure, using a PROM programmer or the control by the central processing unit (CPU), is supported. Also, each of these microcomputers has the memory area dedicated for storing a certain software which controls programming and erasure (reprogramming control software). Therefore, on these microcomputers, the program can easily be changed even after they are mounted on the board.

DISTINCTIVE FEATURES

<Microcomputer mode>

- Number of basic machine instructions 203
- Memory
 - Flash memory (User ROM area) 60 Kbytes
 - RAM 3072 bytes
 - Flash memory (Boot ROM area) 8 Kbytes
- Instruction execution time
 - The fastest instruction at 20 MHz frequency 50 ns
- Single power supply 5 V ± 0.5 V
- Interrupts 8 external sources, 23 internal sources, 7 levels
- Multi-functional 16-bit timer 10 + 3
 (Three-phase motor drive waveform or Pulse motor drive waveform output is available.)
- Serial I/O (UART or Clock synchronous) 3
- 10-bit A-D converter 12-channel inputs
- 8-bit D-A converter 2-channel outputs
- 12-bit watchdog timer
- Programmable input/output (ports P1, P2, P4, P5, P6, P7, P8) 50

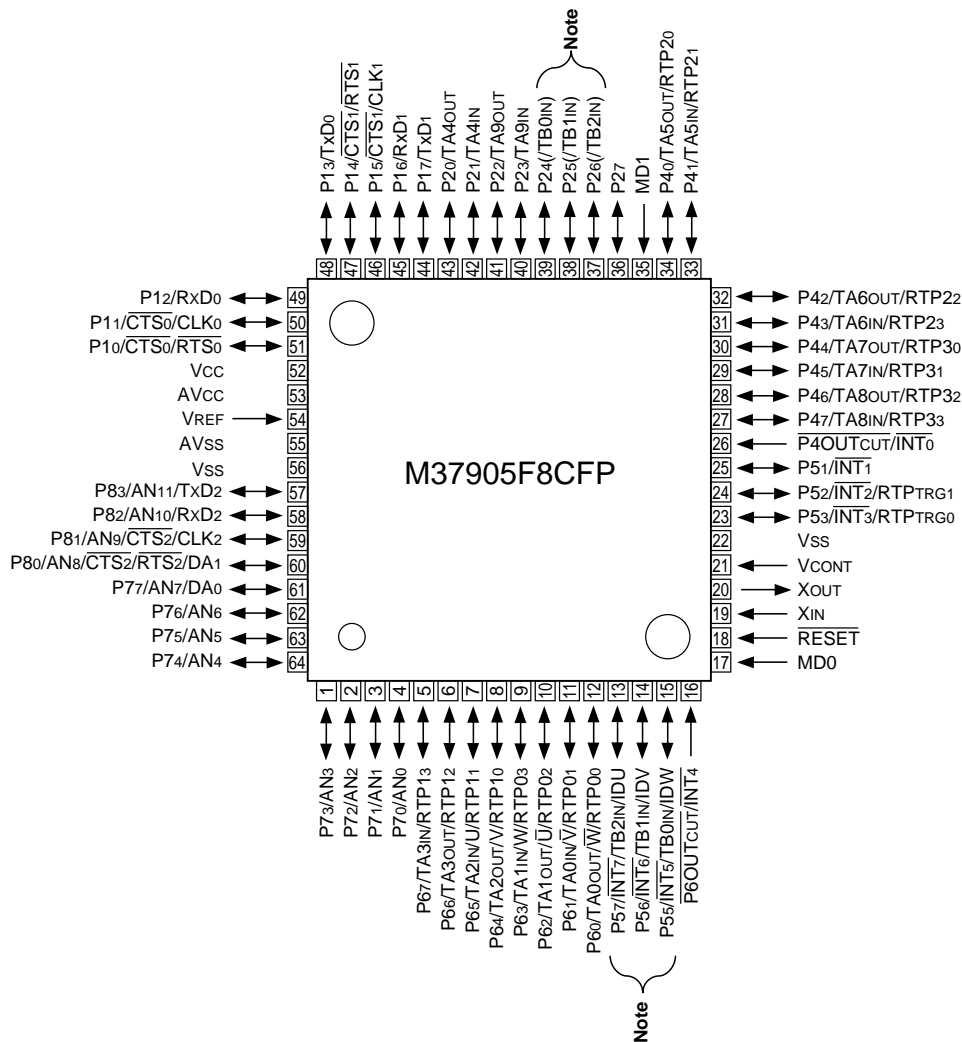
<Flash memory mode>

- Power supply voltage 5 V ± 0.5 V
- Programming/Erase voltage 5 V ± 0.5 V
- Programming method Programming in a unit of word
- Erase method Block erase or Total erase
 M37905F8CFP, M37905F8CSP
 4 blocks (8 Kbytes X 2, 16 Kbytes X 1, 28 Kbytes X 1)
- Programming/Erase control by software command
- Maximum number of reprograms 100

APPLICATION

- Control devices for office equipment such as copiers and facsimiles
- Control devices for industrial equipment such as communication and measuring instruments
- Control devices for equipment, requiring motor control, such as inverter air conditioners and general-purpose inverters

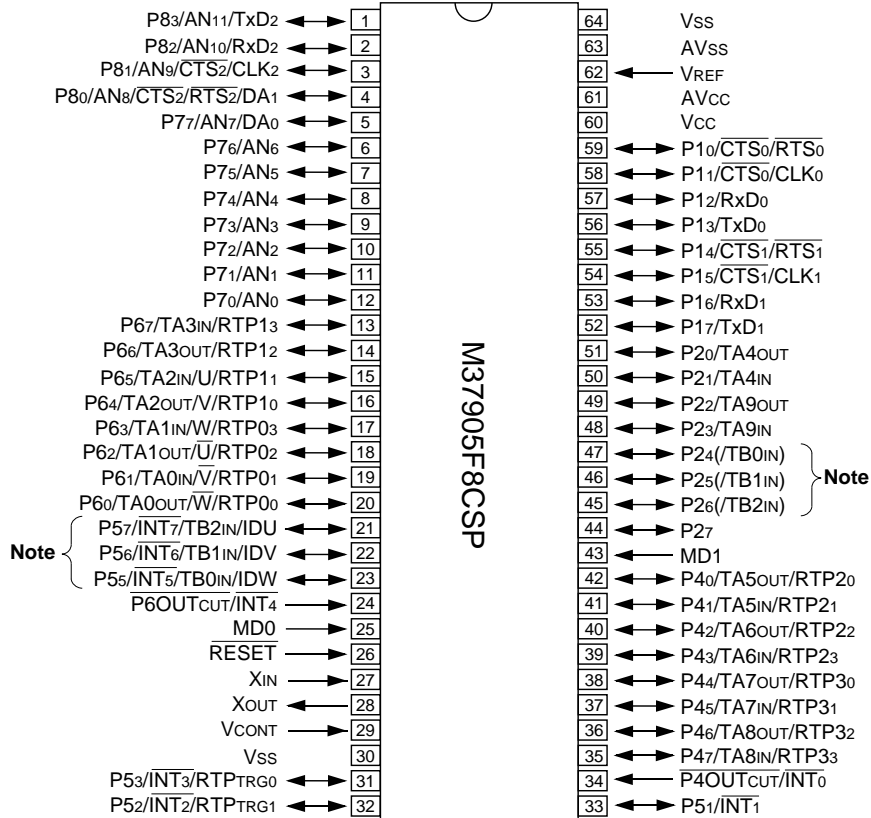
M37905F8CFP PIN CONFIGURATION (TOP VIEW)



Outline 64P6N-A

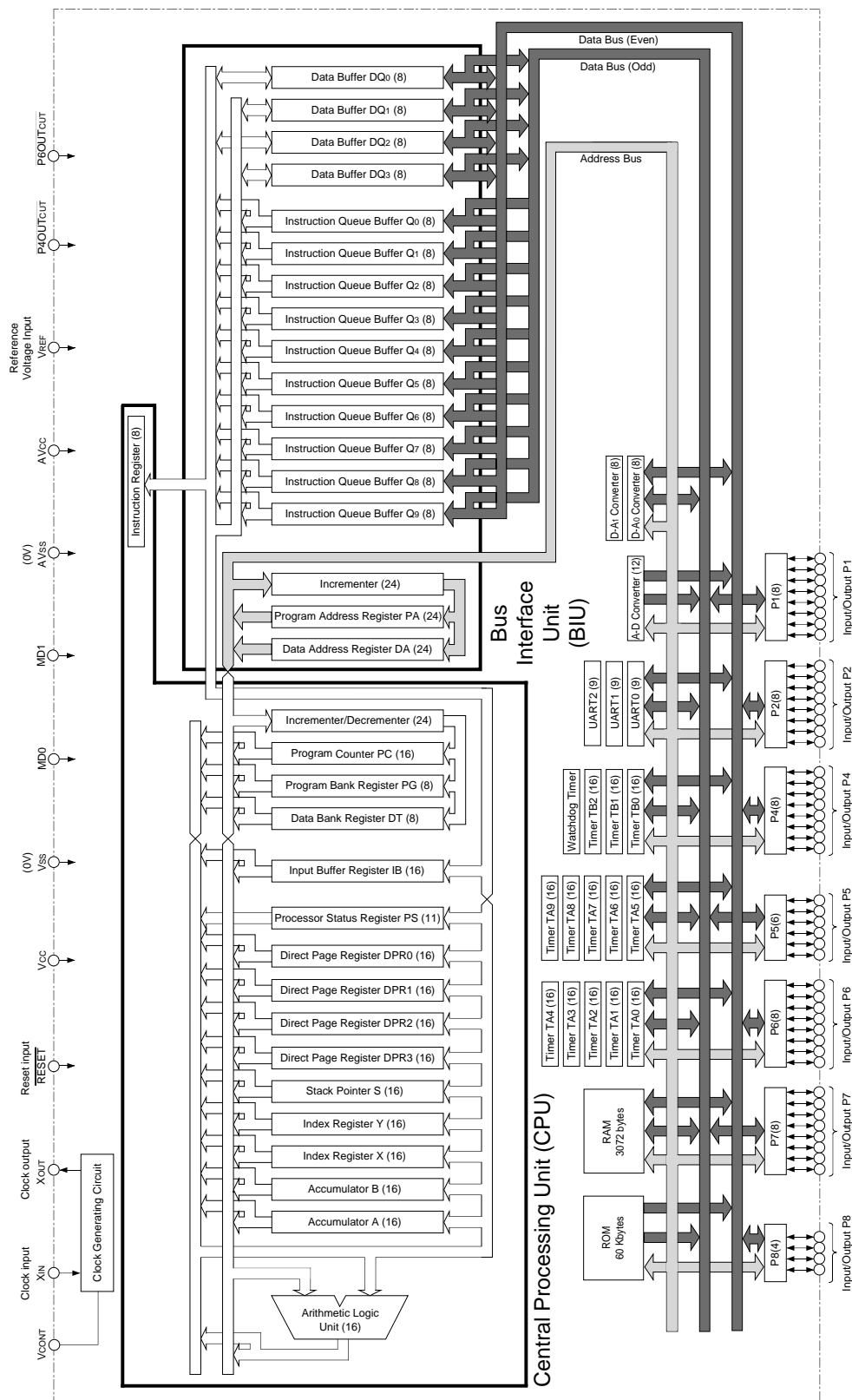
Note: Allocation of pins TB0IN to TB2IN can be switched by software.

M37905F8CSP PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

BLOCK DIAGRAM



FUNCTIONS (Microcomputer mode)

Parameter		Functions
Number of basic machine instructions		203
Instruction execution time		50 ns (the fastest instruction at $f(f_{sys}) = 20$ MHz)
External clock input frequency $f(XIN)$		20 MHz (Max.)
System clock frequency $f(f_{sys})$		20 MHz (Max.)
Memory size	Flash memory (User ROM area)	60 Kbytes
	RAM	3072 bytes
	Flash memory (Boot ROM area)	8 Kbytes
Programmable input/output ports	P1, P2, P4, P6, P7	8-bit X 5
	P5	6-bit X 1
	P8	4-bit X 1
Multi-functional timers	TA0–TA9	16-bit X 10
	TB0–TB2	16-bit X 3
Serial I/O	UART0, UART1, and UART2	(UART or Clock synchronous serial I/O) X 3
A-D converter		10-bit successive approximation method X 1 (12 channels)
D-A converter		8-bit X 2
Dead-time timer		8-bit X 3
Watchdog timer		12-bit X 1
Interrupts	Maskable interrupts	8 external sources, 20 internal sources. Each interrupt can be set to a priority level within the range of 0–7 by software.
	Non-maskable interrupts	3 internal sources.
Clock generating circuit		Incorporated (externally connected to a ceramic resonator or quartz crystal resonator).
PLL frequency multiplier		The following multiplication ratios are available: X2, X3, X4.
Power supply voltage		5 V \pm 0.5 V
Power dissipation		125 mW (at $f(f_{sys}) = 20$ MHz, Typ., ; the PLL frequency multiplier is inactive.)
Ports' input/output characteristics	Input/Output withstand voltage	5 V
	Output current	5 mA
Memory expansion		Not available (single-chip mode only).
Operating ambient temperature range		–20 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		(Note)

Note:	Packages	M37905F8CFP	64-pin plastic molded QFP (64P6N-A)
		M37905F8CSP	64-pin shrink plastic moldeds DIP (64P4B)

FUNCTIONS (Flash memory mode)

Parameter		Functions
Power supply voltage		5 V \pm 0.5 V
Programming/Erase voltage		5 V \pm 0.5 V
Flash memory mode		3 modes: parallel I/O, serial I/O, and CPU reprogramming modes
Block division for erasure	User ROM area	4 blocks (8 Kbytes \times 2, 16 Kbytes \times 1, 28 Kbytes \times 1); total of 60 Kbytes
	Boot ROM area	1 block (8 Kbytes \times 1) (Note)
Programming method		Programmed per word
	Flash memory parallel I/O mode	User ROM area + Boot ROM area
	Flash memory serial I/O mode	User ROM area
	Flash memory CPU reprogramming mode	User ROM area
Erase method		Total erase/Block erase
	Flash memory parallel I/O mode	User ROM area + Boot ROM area
	Flash memory serial I/O mode	User ROM area
	Flash memory CPU reprogramming mode	User ROM area
Programming/Erase control		Programming/Erase control by software commands
Number of commands		6 commands
Maximum number of reprograms		100

Note: On shipment, our reprogramming control firmware for the flash memory serial I/O mode has been stored into the boot ROM area.

PIN DESCRIPTION (MICROCOMPUTER MODE)

Pin	Name	Input/ Output	Functions
Vcc, Vss	Power supply input	—	Apply 5 V \pm 0.5 V to Vcc, and 0 V to Vss.
MD0	MD0	Input	Connect this pin to Vss.
MD1	MD1	Input	Connect this pin to Vss.
RESET	Reset input	Input	The microcomputer is reset when "L" level is applies to this pin.
XIN	Clock input	Output	These are input and output pins of the internal clock generating circuit. Connect a ceramic resonator or quartz-crystal oscillator between pins XIN and XOUT. When an external clock is used, the clock source should be connected to pin XIN, and pin XOUT should be left open.
XOUT	Clock output		
VCONT	Filter circuit connection	—	When using the PLL frequency multiplier, connect this pin to the filter circuit. When not using the PLL frequency multiplier, this pin should be left open.
AVcc, AVss	Analog power supply input	—	Power supply input pins for the A-D and D-A converters. Connect AVcc to Vcc, and AVss to Vss externally.
VREF	Reference voltage input	Input	This is the reference voltage input pin for the A-D and D-A converters.
P10–P17	I/O port P1	I/O	Port P1 is an 8-bit I/O port. This port has an I/O direction register, and each pin can be programmed for input or output. These pins enter the input mode at reset. These pins also function as I/O pins of UART0, 1.
P20–P27	I/O port P2	I/O	In addition to having the same functions as port P1, these pins function as I/O pins for timers A4 and A9. Also, they can be programmed to function as input pins for timers B0 to B2.
P40–P47	I/O port P4	I/O	In addition to having the same functions as port P1, these pins function as I/O pins for timers A5 to A8. Also, they function as output pins for motor drive waveform.
P51–P53, P55–P57	I/O port P5	I/O	In addition to having the same functions as port P1, these pins function as input pins for INT1 to INT3 and INT5 to INT7. Also, pins P55 to P57 function as input pins for timers B0 to B2 and as input pins for position data in the three-phase waveform mode; and pins P52 and P53 function as trigger-input pins in the pulse output port mode.
P60–P67	I/O port P6	I/O	In addition to having the same functions as port P1, these pins function as I/O pins for timers A0 to A3. Also, they function as motor drive waveform output pins.
P70–P77	I/O port P7	I/O	In addition to having the same functions as port P1, these pins function as input pins for the A-D converter. Also, P77 functions as an output pin for the D-A converter.
P80–P83	I/O port P8	I/O	In addition to having the same functions as port P1, these pins function as input pins for the A-D converter. Also, these pins function as I/O pins for UART2, and pin P80 functions as an output pin for the D-A converter.
P4OUTCUT	P4OUTCUT input	Input	This pin has the function to forcibly place port P4 pins in the input mode. Also, this pin functions as an input pin for INT0; and this pin is used to input a signal, which forcibly cuts off a motor drive waveform output.
P6OUTCUT	P6OUTCUT input	Input	This pin has the function to forcibly place port P6 pins in the input mode. Also, this pin functions as an input pin for INT4; and this pin is used to input a signal, which forcibly cuts off a motor drive waveform output.

PIN DESCRIPTION (FLASH MEMORY SERIAL I/O MODE)

Pin	Name	Input /Output	Functions
Vcc, Vss	Power supply input	—	Apply 5 V \pm 0.5 V to Vcc, and 0 V to Vss.
MD0	MD0	Input	Connect this pin to Vss.
MD1	MD1	Input	Connect this pin to Vss via a resistor of 10 k Ω to 100 k Ω .
RESET	Reset input	Input	The reset input pin.
XIN	Clock input	Input	Connect a ceramic oscillator between the XIN and XOUT pins, or input an external clock from the XIN pin with the XOUT pin left open.
XOUT	Clock output	Output	
AVcc, AVss	Analog supply input	—	Connect AVcc to Vcc, and AVss to Vss.
VREF	Reference voltage input	Input	Input an arbitrary level within the range of Vss–Vcc. (This is not used in the flash memory serial I/O mode.)
P10–P17	Input port P1	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P20–P23, P27	Input port P2	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P24	SCLK input	Input	This is an input pin for a serial clock.
P25	SDA I/O	I/O	This is an I/O pin for serial data. Connect this pin to Vcc via a resistor (about 1 k Ω).
P26	BUSY output	Output	This is an output pin for the BUSY signal.
P4OUTCUT	P4OUTCUT input	Input	Input “H”.
P6OUTCUT	P6OUTCUT input	Input	Input “H”.
P40–P47	Input port P4	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P55–P53, P55–P57	Input port P5	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P60–P67	Input port P6	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P70–P74	Input port P7	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P80–P83	Input port P8	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
VCONT	Filter circuit connection	—	Connect this pin to the filter circuit, or leave this pin open. (This is not used in the flash memory serial I/O mode.)

BASIC FUNCTION BLOCKS

Each of the M37905F8CFP and M37905F8CSP has the same function as that of the M37905M4C-XXXXFP except for the following. Therefore, for details except for the following, refer to the datasheet of the M37905M4C-XXXXFP.

- Internal ROM: type (flash memory) and size
- RAM size

MEMORY

Figure 1 shows the memory map.

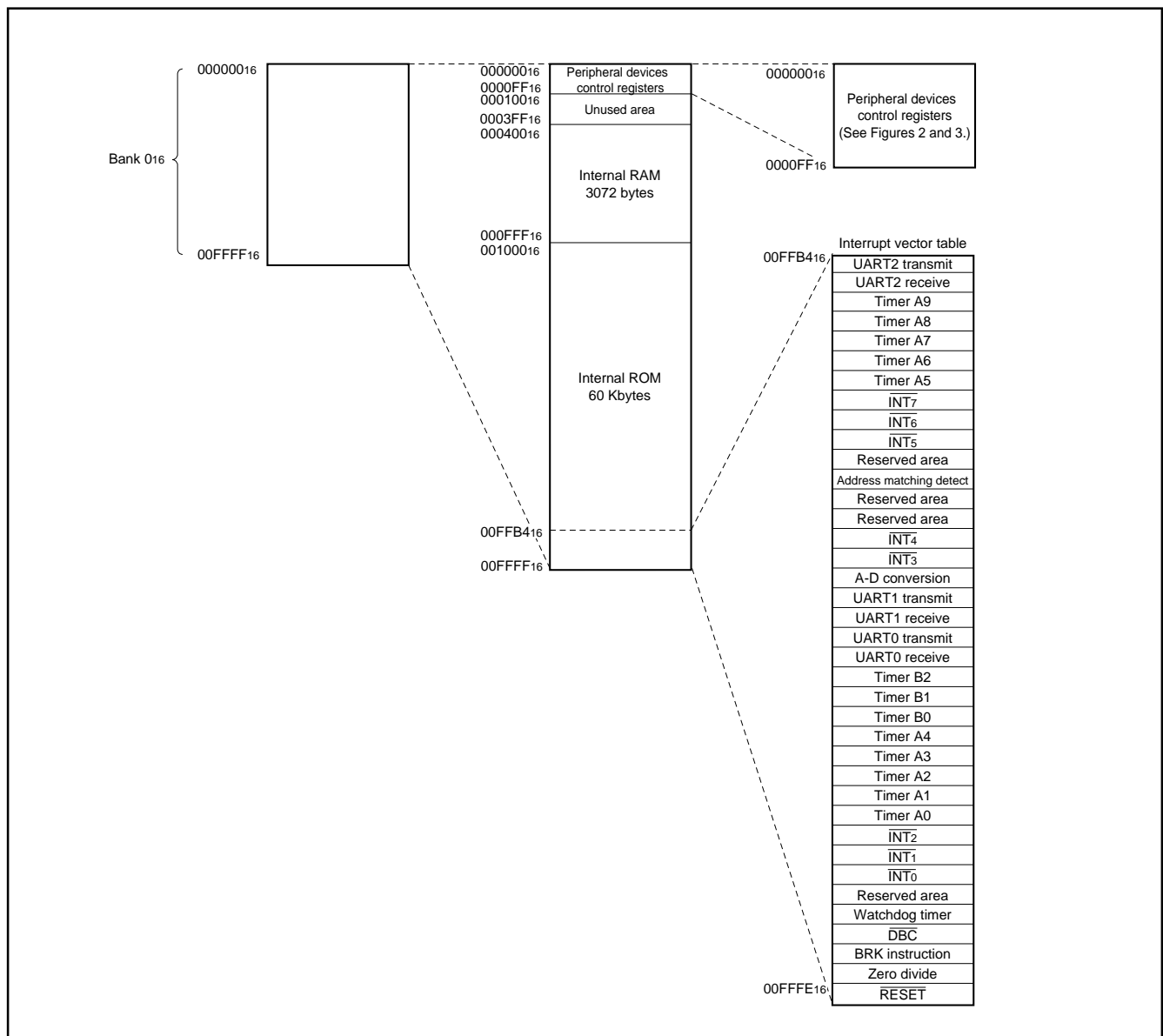


Fig. 1 Memory map of M37905F8CFP, M37905F8CSP (Single-chip mode)

Address (Hexadecimal notation)		Address (Hexadecimal notation)	
000000 ¹⁶	Reserved area (Note)	000040 ¹⁶	Count start register 0
000001 ¹⁶	Reserved area (Note)	000041 ¹⁶	Count start register 1
000002 ¹⁶	Reserved area (Note)	000042 ¹⁶	One-shot start register 0
000003 ¹⁶	Port P1 register	000043 ¹⁶	One-shot start register 1
000004 ¹⁶	Reserved area (Note)	000044 ¹⁶	Up-down register 0
000005 ¹⁶	Port P1 direction register	000045 ¹⁶	Timer A clock division select register
000006 ¹⁶	Port P2 register	000046 ¹⁶	Timer A0 register
000007 ¹⁶	Reserved area (Note)	000047 ¹⁶	
000008 ¹⁶	Port P2 direction register	000048 ¹⁶	Timer A1 register
000009 ¹⁶	Reserved area (Note)	000049 ¹⁶	
00000A ¹⁶	Port P4 register	00004A ¹⁶	Timer A2 register
00000B ¹⁶	Port P5 register	00004B ¹⁶	
00000C ¹⁶	Port P4 direction register	00004C ¹⁶	Timer A3 register
00000D ¹⁶	Port P5 direction register	00004D ¹⁶	
00000E ¹⁶	Port P6 register	00004E ¹⁶	Timer A4 register
00000F ¹⁶	Port P7 register	00004F ¹⁶	
000010 ¹⁶	Port P6 direction register	000050 ¹⁶	Timer B0 register
000011 ¹⁶	Port P7 direction register	000051 ¹⁶	
000012 ¹⁶	Port P8 register	000052 ¹⁶	Timer B1 register
000013 ¹⁶		000053 ¹⁶	
000014 ¹⁶	Port P8 direction register	000054 ¹⁶	Timer B2 register
000015 ¹⁶		000055 ¹⁶	
000016 ¹⁶	Reserved area (Note)	000056 ¹⁶	Timer A0 mode register
000017 ¹⁶	Reserved area (Note)	000057 ¹⁶	Timer A1 mode register
000018 ¹⁶	Reserved area (Note)	000058 ¹⁶	Timer A2 mode register
000019 ¹⁶	Reserved area (Note)	000059 ¹⁶	Timer A3 mode register
00001A ¹⁶		00005A ¹⁶	Timer A4 mode register
00001B ¹⁶		00005B ¹⁶	Timer B0 mode register
00001C ¹⁶		00005C ¹⁶	Timer B1 mode register
00001D ¹⁶		00005D ¹⁶	Timer B2 mode register
00001E ¹⁶	A-D control register 0	00005E ¹⁶	Processor mode register 0
00001F ¹⁶	A-D control register 1	00005F ¹⁶	Processor mode register 1
000020 ¹⁶	A-D register 0	000060 ¹⁶	Watchdog timer register
000021 ¹⁶		000061 ¹⁶	Watchdog timer frequency select register
000022 ¹⁶	A-D register 1	000062 ¹⁶	Particular function select register 0
000023 ¹⁶		000063 ¹⁶	Particular function select register 1
000024 ¹⁶	A-D register 2	000064 ¹⁶	Particular function select register 2
000025 ¹⁶		000065 ¹⁶	Reserved area (Note)
000026 ¹⁶	A-D register 3	000066 ¹⁶	Debug control register 0
000027 ¹⁶		000067 ¹⁶	Debug control register 1
000028 ¹⁶	A-D register 4	000068 ¹⁶	Address comparison register 0
000029 ¹⁶		000069 ¹⁶	
00002A ¹⁶	A-D register 5	00006A ¹⁶	Address comparison register 1
00002B ¹⁶		00006B ¹⁶	
00002C ¹⁶	A-D register 6	00006C ¹⁶	INT ₃ interrupt control register
00002D ¹⁶		00006D ¹⁶	
00002E ¹⁶	A-D register 7	00006E ¹⁶	INT ₄ interrupt control register
00002F ¹⁶		00006F ¹⁶	A-D conversion interrupt control register
000030 ¹⁶	UART0 transmit/receive mode register	000070 ¹⁶	UART0 transmit interrupt control register
000031 ¹⁶	UART0 baud rate register (BRG0)	000071 ¹⁶	UART0 receive interrupt control register
000032 ¹⁶	UART0 transmit buffer register	000072 ¹⁶	UART1 transmit interrupt control register
000033 ¹⁶		000073 ¹⁶	UART1 receive interrupt control register
000034 ¹⁶	UART0 transmit/receive control register 0	000074 ¹⁶	Timer A0 interrupt control register
000035 ¹⁶	UART0 transmit/receive control register 1	000075 ¹⁶	Timer A1 interrupt control register
000036 ¹⁶	UART0 receive buffer register	000076 ¹⁶	Timer A2 interrupt control register
000037 ¹⁶		000077 ¹⁶	Timer A3 interrupt control register
000038 ¹⁶	UART1 transmit/receive mode register	000078 ¹⁶	Timer A4 interrupt control register
000039 ¹⁶	UART1 baud rate register (BRG1)	000079 ¹⁶	Timer B0 interrupt control register
00003A ¹⁶	UART1 transmit buffer register	00007A ¹⁶	Timer B1 interrupt control register
00003B ¹⁶		00007B ¹⁶	Timer B2 interrupt control register
00003C ¹⁶	UART1 transmit/receive control register 0	00007C ¹⁶	INT ₀ interrupt control register
00003D ¹⁶	UART1 transmit/receive control register 1	00007D ¹⁶	INT ₁ interrupt control register
00003E ¹⁶	UART1 receive buffer register	00007E ¹⁶	INT ₂ interrupt control register
00003F ¹⁶		00007F ¹⁶	

Note: Do not write to this address.

Fig. 2 Location of SFRs (1)

Address (Hexadecimal notation)		Address (Hexadecimal notation)	
000080 ¹⁶	Reserved area (Note)	0000C0 ¹⁶	
000081 ¹⁶	Reserved area (Note)	0000C1 ¹⁶	
000082 ¹⁶	Reserved area (Note)	0000C2 ¹⁶	
000083 ¹⁶	Reserved area (Note)	0000C3 ¹⁶	
000084 ¹⁶	Reserved area (Note)	0000C4 ¹⁶	Up-down register 1
000085 ¹⁶	Reserved area (Note)	0000C5 ¹⁶	
000086 ¹⁶	Reserved area (Note)	0000C6 ¹⁶	Timer A5 register
000087 ¹⁶	Reserved area (Note)	0000C7 ¹⁶	
000088 ¹⁶		0000C8 ¹⁶	Timer A6 register
000089 ¹⁶		0000C9 ¹⁶	
00008A ¹⁶	Reserved area (Note)	0000CA ¹⁶	Timer A7 register
00008B ¹⁶		0000CB ¹⁶	
00008C ¹⁶	Reserved area (Note)	0000CC ¹⁶	Timer A8 register
00008D ¹⁶		0000CD ¹⁶	
00008E ¹⁶	Reserved area (Note)	0000CE ¹⁶	Timer A9 register
00008F ¹⁶		0000CF ¹⁶	
000090 ¹⁶	Reserved area (Note)	0000D0 ¹⁶	Timer A0 ₁ register
000091 ¹⁶		0000D1 ¹⁶	
000092 ¹⁶	Reserved area (Note)	0000D2 ¹⁶	Timer A1 ₁ register
000093 ¹⁶		0000D3 ¹⁶	
000094 ¹⁶		0000D4 ¹⁶	Timer A2 ₁ register
000095 ¹⁶	External interrupt input read-out register	0000D5 ¹⁶	
000096 ¹⁶	D-A control register	0000D6 ¹⁶	Timer A5 mode register
000097 ¹⁶		0000D7 ¹⁶	Timer A6 mode register
000098 ¹⁶	D-A register 0	0000D8 ¹⁶	Timer A7 mode register
000099 ¹⁶	D-A register 1	0000D9 ¹⁶	Timer A8 mode register
00009A ¹⁶		0000DA ¹⁶	Timer A9 mode register
00009B ¹⁶		0000DB ¹⁶	A-D control register 2
00009C ¹⁶	Reserved area (Note)	0000DC ¹⁶	Comparator function select register 0
00009D ¹⁶	Reserved area (Note)	0000DD ¹⁶	Comparator function select register 1
00009E ¹⁶	Flash memory control register	0000DE ¹⁶	Comparator result register 0
00009F ¹⁶		0000DF ¹⁶	Comparator result register 1
0000A0 ¹⁶	Pulse output control register	0000E0 ¹⁶	
0000A1 ¹⁶		0000E1 ¹⁶	A-D register 8
0000A2 ¹⁶	Pulse output data register 0	0000E2 ¹⁶	
0000A3 ¹⁶		0000E3 ¹⁶	A-D register 9
0000A4 ¹⁶	Pulse output data register 1	0000E4 ¹⁶	
0000A5 ¹⁶		0000E5 ¹⁶	A-D register 10
0000A6 ¹⁶	Waveform output mode register	0000E6 ¹⁶	
0000A7 ¹⁶	Dead-time timer	0000E7 ¹⁶	A-D register 11
0000A8 ¹⁶	Three-phase output data register 0	0000E8 ¹⁶	Reserved area (Note)
0000A9 ¹⁶	Three-phase output data register 1	0000E9 ¹⁶	Reserved area (Note)
0000AA ¹⁶	Position-data-retain function control register	0000EA ¹⁶	Reserved area (Note)
0000AB ¹⁶		0000EB ¹⁶	Reserved area (Note)
0000AC ¹⁶	Serial I/O pin control register	0000EC ¹⁶	Reserved area (Note)
0000AD ¹⁶		0000ED ¹⁶	Reserved area (Note)
0000AE ¹⁶	Port P2 pin function control register	0000EE ¹⁶	Reserved area (Note)
0000AF ¹⁶		0000EF ¹⁶	Reserved area (Note)
0000B0 ¹⁶	UART2 transmit/receive mode register	0000F0 ¹⁶	
0000B1 ¹⁶	UART2 band rate register (BRG2)	0000F1 ¹⁶	UART2 transmit interrupt control register
0000B2 ¹⁶	UART2 transmit buffer register	0000F2 ¹⁶	UART2 receive interrupt control register
0000B3 ¹⁶		0000F3 ¹⁶	
0000B4 ¹⁶	UART2 transmit/receive control register 0	0000F4 ¹⁶	
0000B5 ¹⁶	UART2 transmit/receive control register 1	0000F5 ¹⁶	Timer A5 interrupt control register
0000B6 ¹⁶	UART2 receive buffer register	0000F6 ¹⁶	Timer A6 interrupt control register
0000B7 ¹⁶		0000F7 ¹⁶	Timer A7 interrupt control register
0000B8 ¹⁶	Reserved area (Note)	0000F8 ¹⁶	Timer A8 interrupt control register
0000B9 ¹⁶		0000F9 ¹⁶	Timer A9 interrupt control register
0000BA ¹⁶	Reserved area (Note)	0000FA ¹⁶	
0000BB ¹⁶	Reserved area (Note)	0000FB ¹⁶	
0000BC ¹⁶	Clock control register 0	0000FC ¹⁶	
0000BD ¹⁶	Reserved area (Note)	0000FD ¹⁶	INT ₅ interrupt control register
0000BE ¹⁶	Reserved area (Note)	0000FE ¹⁶	INT ₆ interrupt control register
0000BF ¹⁶	Reserved area (Note)	0000FF ¹⁶	INT ₇ interrupt control register

Note: Do not write to this address.

Fig. 3 Location of SFRs (2)

FLASH MEMORY MODE

These microcomputers contain the flash memory; and single-power-supply reprogramming is available to this. These microcomputers have the following three modes, enabling reading/programming/erase for the flash memory:

- Flash memory parallel I/O mode and Flash memory serial I/O mode, where the flash memory is handled by using an external programmer.
- CPU reprogramming mode, where the flash memory is handled by the central processing unit (CPU).

As shown in Figure 4, the flash memory is divided into several blocks, and erasure per block is possible.

This internal flash memory has the boot ROM area storing the reprogramming control software for reprogramming in the CPU reprogramming mode and flash memory serial I/O mode, as well as the user ROM area storing a certain control software for the normal operation in the microcomputer mode.

Although our reprogramming control firmware for the flash memory serial I/O mode has been stored into this boot ROM area on shipment, the user-original reprogramming control software which is more appropriate for the user's system is reprogrammable into this area, instead. Note that the reprogramming for the boot ROM area is enabled only in the flash memory parallel I/O mode.

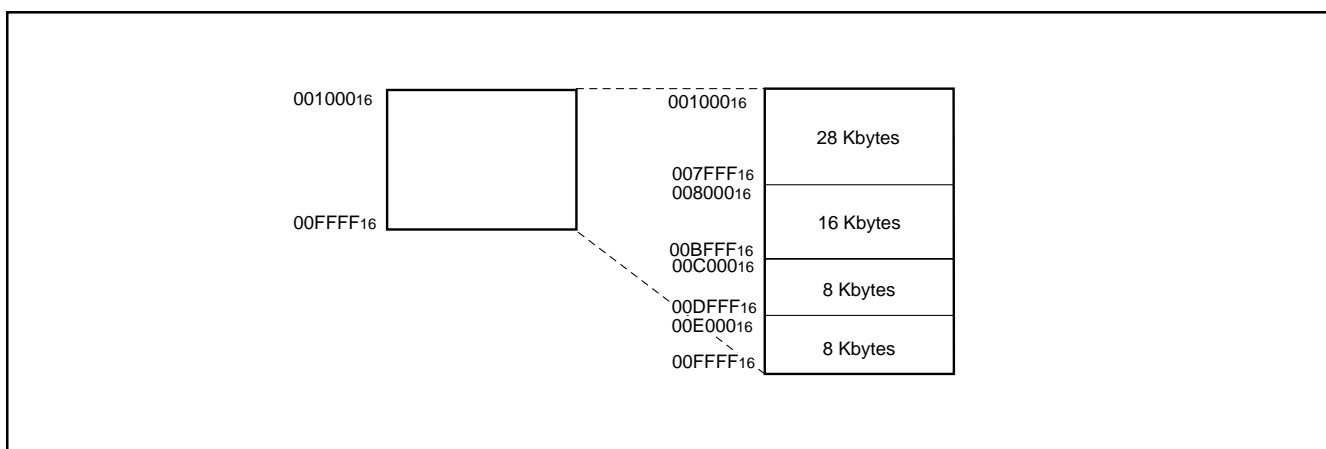


Fig. 4 M37905F8CFP, M37905F8CSP: block configuration of internal flash memory

Flash Memory Parallel I/O Mode

The flash memory parallel I/O mode is used to manipulate the internal flash memory with a parallel programmer. This parallel programmer uses the software commands listed in Table 1 to do the flash memory manipulations, such as read/programming/erase operations.

Table 1. Software commands (flash memory parallel I/O mode)

Software Command
Read Array
Read Status Register
Clear Status Register
Programming
Block Erase
Erase All Block

Addresses FF90₁₆ to FF9F₁₆ are the reserved area for the parallel programmer. Therefore, when the user uses the flash memory parallel I/O mode, do not program to this area.

User ROM Area and Boot ROM Area

The user ROM area and boot ROM area can be reprogrammed in the flash memory parallel I/O mode.

The programming and block erase operations can be performed only to these areas.

The boot ROM area, 8 Kbytes in size, is assigned to addresses 0000₁₆–1FFF₁₆, so that programming and block erase operations can be performed only to this area. (Access to any address out of this area is prohibited).

The erasable block in the boot ROM area is only one block, consisting of 8 Kbytes. The reprogramming control firmware to be used in the flash memory serial I/O mode has been stored to this boot ROM area on our shipment. Therefore, do not reprogram the boot ROM area if the user uses the flash memory serial I/O mode.

Do not program to addresses FF90₁₆ to FF9F₁₆ because this area is the reserved area for the programmer.

Note that, when the boot ROM area is read out from the CPU in the CPU reprogramming mode, described later, its addresses will be shifted to E000₁₆–FFFF₁₆.

Flash Memory Serial I/O Mode

In the flash memory serial I/O mode, addresses, data, and software commands, which are required to read/program/erase the internal flash memory, are serially input and output with a fewer pins and the dedicated serial programmer.

In this mode, being different from the flash memory parallel I/O mode, the CPU controls reprogramming of the flash memory (using the CPU reprogramming mode), serial input of the reprogramming data, etc.

The reprogramming control firmware for the flash memory serial I/O mode has been stored in the boot ROM area on shipment of the product from us. Note that, then, the flash memory serial I/O mode will become unavailable if the boot ROM area has been reprogrammed in the flash memory parallel I/O mode.

Note that, also, this reprogramming control firmware for the flash memory serial I/O mode is subject to change.

Figures 5 and 6 show the pin connections in the flash memory serial I/O mode.

The three pins, SCLK, SDA, and BUSY, are used to input and output serial data.

The SCLK pin is the input pin of external transfer clocks. The SDA pin is the I/O pin of transmit and receive data, and its output acts as the N-channel open-drain output. To the SDA pin, connect an external pullup resistor (about 1 k Ω). The BUSY pin is the output pin of the BUSY flag (CMOS output) and goes "H" during BUSY periods owing to a certain operation, such as transmit, receive, erase, programming, etc.

Transmit and receive data are serially transferred 8 bits at a time.

In the flash memory serial I/O mode, only the user ROM area can be reprogrammed; the boot ROM area is not accessible.

Addresses FF90₁₆ to FF9F₁₆ are the reserved area for the serial programmer. Therefore, when the user uses the flash memory serial I/O mode, do not program to this area.

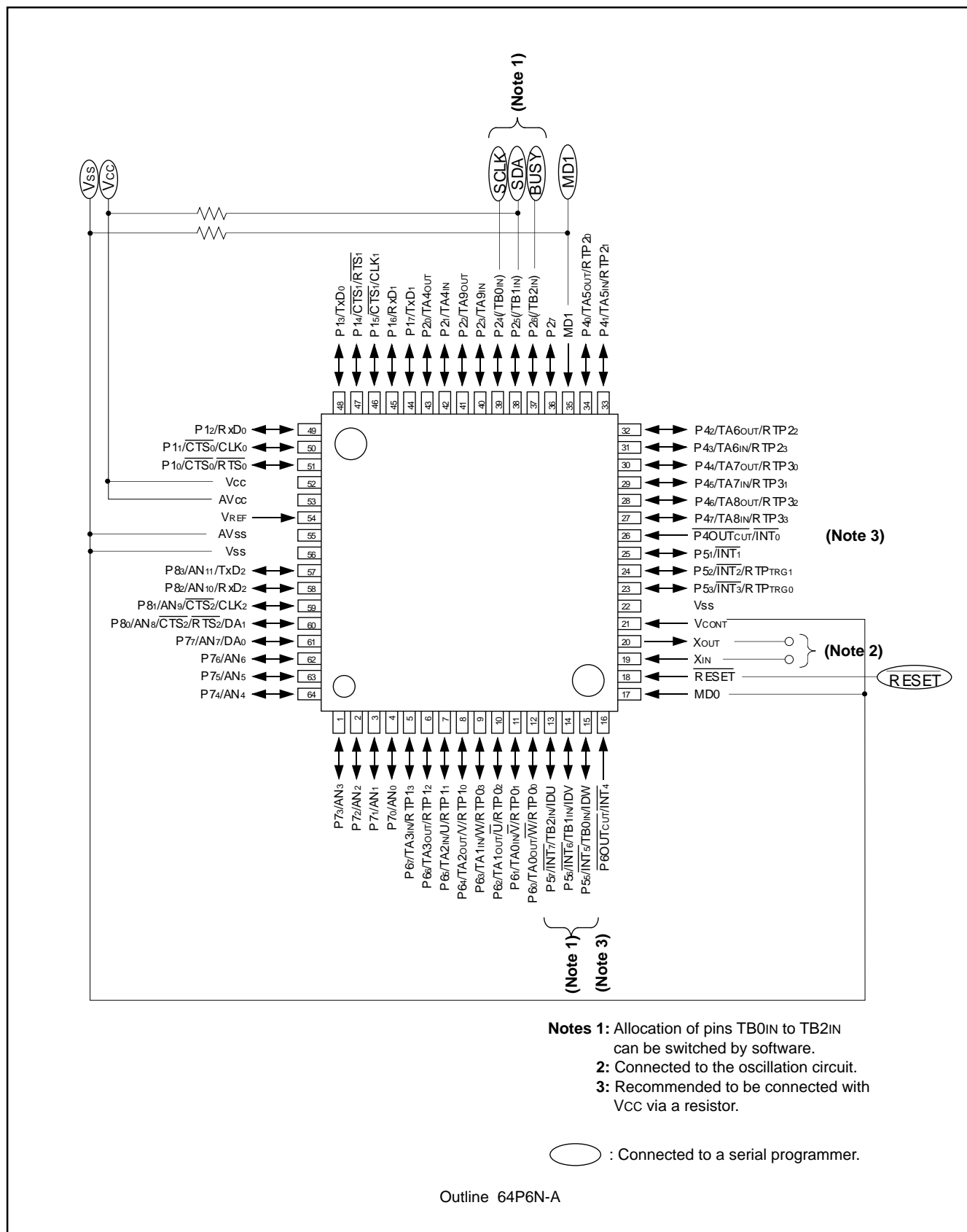


Fig. 5 Pin connection of M37905F8CFP in flash memory serial I/O mode (outline: 64P6N-A)

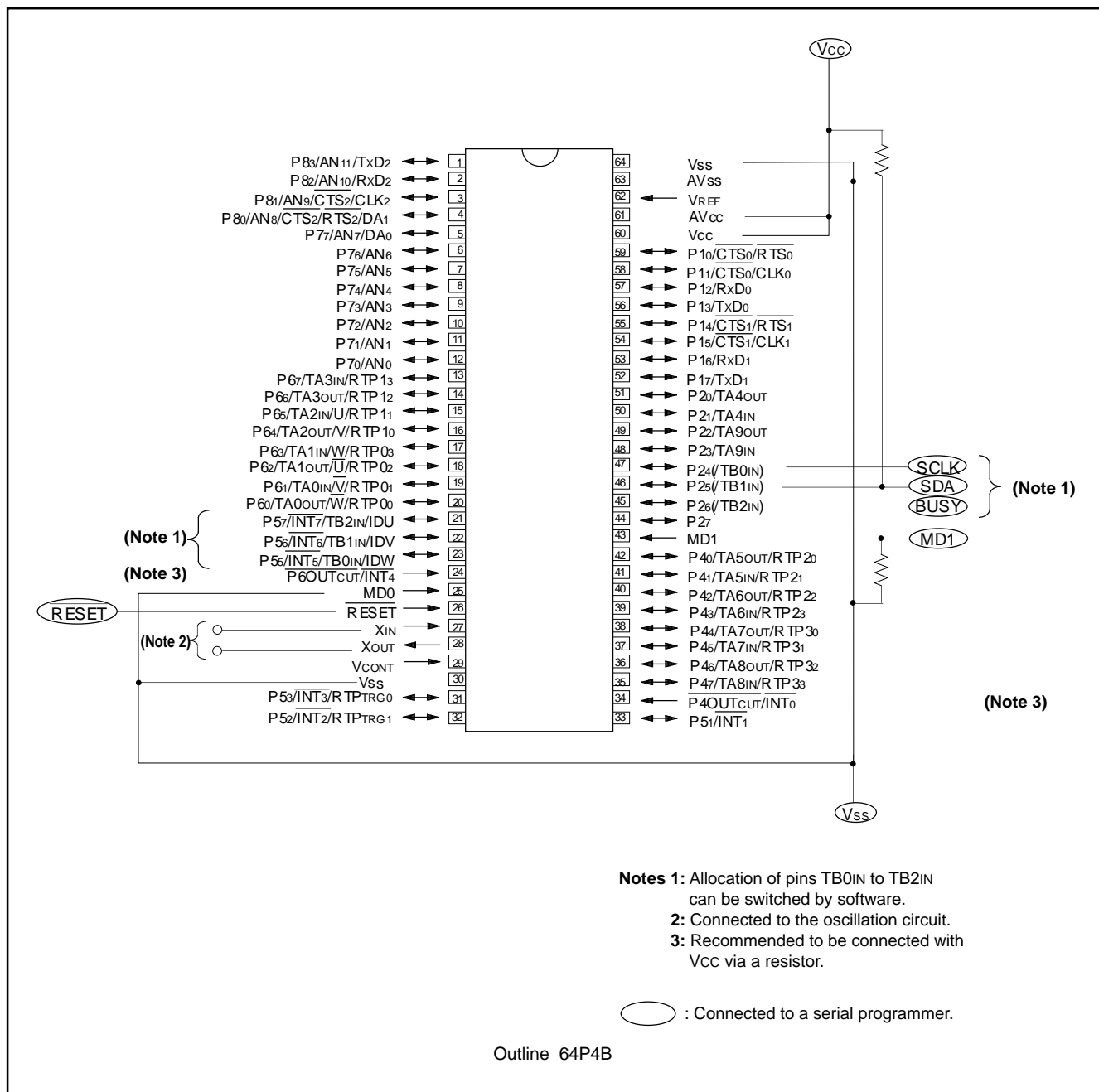


Fig. 6 Pin connection of M37905F8CSP in flash memory serial I/O mode (outline: 64P4B)

CPU Reprogramming Mode

The CPU reprogramming mode is used to perform the operations for the internal flash memory (reading, programming, erasing) under control of the CPU.

In this mode, only the user ROM area can be reprogrammed; the boot ROM area cannot be reprogrammed.

The user-original reprogramming control software for the CPU reprogramming mode can be stored in either the user ROM area or the boot ROM area.

Because the CPU cannot read out the flash memory in the CPU reprogramming mode, the above software must be transferred to the internal RAM in advance to be executed.

Boot Mode

The user-original reprogramming control software for the CPU reprogramming mode must be stored into the user ROM area or the boot ROM area in the flash memory parallel I/O mode in advance. (If this program has been stored into the boot ROM area, the flash memory serial I/O mode will become unavailable).

Note that addresses of the boot ROM area depend on the accessing ways to the boot ROM area. When accessing in the flash memory parallel I/O mode, these addresses will be shifted to 0000₁₆ to 1FFF₁₆. On the other hand, when accessing with the CPU, these addresses will be shifted to E000₁₆ to FFFF₁₆.

Reset removal with both of the MD0 and MD1 pins held "L" invokes the normal microcomputer mode, and the CPU operates using the control software stored in the user ROM area. In this case, the boot ROM area is not accessible.

Removing reset with the MD0 pin held "L" and the MD1 pin "H", the CPU starts its operation using the reprogramming control software stored in the boot ROM area. This mode is called the boot mode. The reprogramming control software in the boot ROM area can also reprogram the user ROM area.

After reset removal, be sure not to change the status at pins MD0 and MD1.

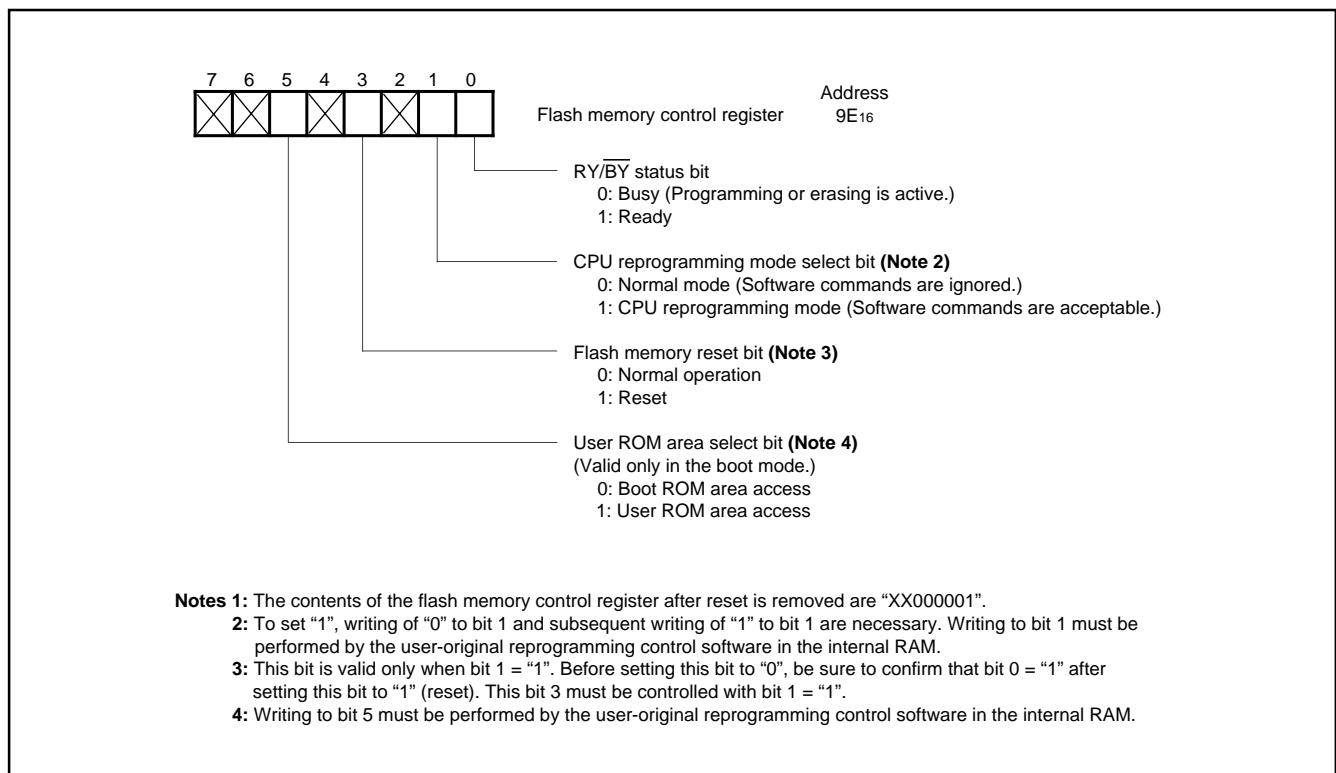


Fig. 7 Bit configuration of flash memory control register

Function overview (CPU reprogramming mode)

The CPU reprogramming mode is available in the single-chip mode, memory expansion mode, and boot mode to reprogram the user ROM area only.

In the CPU reprogramming mode, the CPU erases, programs, and reads the internal flash memory by writing software commands. Note that the user-original reprogramming control software must be transferred to the internal RAM in advance to be executed.

The CPU reprogramming mode becomes active when "1" is written into the flash memory control register's bit 1 (the CPU reprogramming mode select bit) shown in Figure 7, and software commands become acceptable.

In the CPU reprogramming mode, software commands and data are all written to and read from even addresses (Note that address A0 in byte addresses = "0"). 16 bits at a time. Therefore, a software command consisting of 8 bits must be written to an even address; therefore, any command written to an odd address will be invalid. Since the write data at the 2nd cycle of a programming command consists of 16 bits, this data must be written to even and odd addresses.

The sequencer in the flash memory controls the erase and programming operations. What the status of the sequencer operation is and whether the programming or erase operation has been completed normally or terminated by an error can be examined by reading the flash memory control register.

Figure 7 shows the bit configuration of the flash memory control register.

Bit 0 (the RY/BY status bit) is a read-only bit for indicating the sequencer operation. This bit goes to "0" (BUSY) while the automatic programming/erase operation is active and goes to "1" (READY) during the other operations.

Bit 1 serves as the CPU reprogramming mode select bit. Writing of "1" to this bit selects the CPU reprogramming mode, and software commands will be acceptable. Because the CPU cannot directly access the internal flash memory in the CPU reprogramming mode, writing to this bit 1 must be performed by the user-original reprogramming control software which has been transferred to the internal RAM in advance. To set bit 1 to "1", it is necessary to write "0" and "1" to this bit 1 successively. On the other hand, to clear this bit to "0", it is sufficient only to write "0".

Bit 3 (the flash memory reset bit) resets the control circuit of the internal flash memory and is used when the CPU reprogramming mode is terminated or when an abnormal access to the flash memory happens. Writing of "1" to bit 3 with the CPU reprogramming mode select bit = "1" performs the reset operation. To remove the reset, write "0" to bit 3 after confirming bit 0 (the RY/BY status bit) becomes "1".

Bit 5 serves as the user ROM area select bit and is valid only in the boot mode. Setting this bit to "1" in the boot mode switches an accessible area from the boot ROM area to the user ROM area. To use the CPU reprogramming mode in the boot mode, set this bit to "1". Note that when the microcomputer is booted up in the user ROM area, only the user ROM area is accessible and bit 5 is invalid; on the other hand, when the microcomputer is in the boot mode, bit 5 is valid independent of the CPU reprogramming mode. To rewrite bit 5, execute the user-original reprogramming control software transferred to the internal RAM in advance.

Figure 8 shows the CPU reprogramming mode set/termination flow-

chart, and be sure to follow this flowchart. As shown in Note 1 of Figure 8, before selecting the CPU reprogramming mode, set "0" to the processor mode register 1's bit 7 (the internal ROM bus cycle select bit) and set flag I to "1" to avoid an interrupt request input.

When a watchdog timer interrupt request is generated in the CPU reprogramming mode, when an input to the $\overline{\text{RESET}}$ pin is "L", or when the software reset is performed, the flash memory control circuit and flash memory control register will be reset.

When the flash memory is reset during the erase or programming operation, this operation is cancelled and the target block's data will be invalid. Just before writing a software command related to the erase/programming operation, be sure to write to the watchdog timer. In the CPU reprogramming mode, be sure not to use the **STP** and **WIT** instructions.

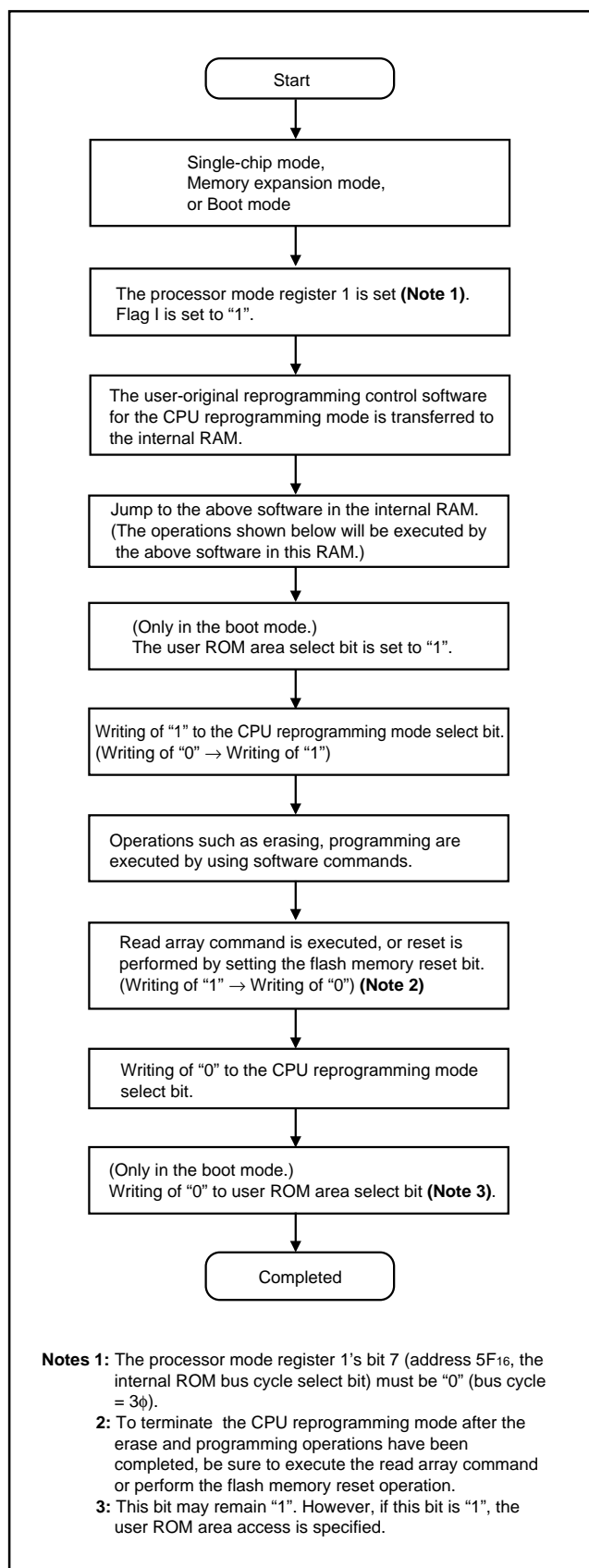


Fig. 8 CPU reprogramming mode set/termination flowchart

Software Commands

Table 2 lists the software commands.

By writing a software command after the CPU reprogramming mode select bit has been set to "1", erasing, programming, etc. can be specified. Note that, at software commands' input, the high-order byte (D₈–D₁₅) is ignored. (Except for the write data at the 2nd cycle of a programming command.)

Software commands are explained as below.

Read Array Command (FF₁₆)

By writing command code "FF₁₆" at the 1st bus cycle, the microcomputer enters the read array mode. If an address to be read is input in the next or the following bus cycles, the contents at the specified address are output to the data bus (D₀ to D₁₅) in a unit of 16 bits.

The read array mode is maintained until writing of another software command.

Read Status Register Command (70₁₆)

Writing command code "70₁₆" at the 1st bus cycle outputs the contents of the status register to the data bus (D₀–D₇) by a read at the 2nd bus cycle.

The status register is explained later.

Clear Status Register Command (50₁₆)

This command clears two status bits (SR.4, 5) each of which is set to "1" to indicate that the operation has been terminated by an error. To clear these bits, write command code "50₁₆" at the 1st bus cycle.

Programming Command (40₁₆)

This command facilitates programming of 1 word (2 bytes) at a time. To initiate programming, write command code "40₁₆" at the 1st bus cycle; when write data is written in a unit of 16 bits at the 2nd bus cycle, the address is specified at the same time. Upon completion of data writing, automatic programming (data programming and verification) operation is started.

The completion of the automatic programming operation is confirmed by a read of the flash memory control register. The RY/BY status bit of the flash memory control register goes "0" during the automatic programming operation; and also, it goes "1" after the end of it.

Before execution of the next command, be sure to confirm that the RY/BY status bit is set to "1" (READY). During the automatic programming operation, writing of commands and access to the flash memory must not be performed.

When programming continuously, the programming command can be executed with the read status register mode kept if there is no programming error. Simultaneously with start of the automatic programming, the read status register mode is automatically active. In this case, the read status register mode is retained until the next read array command (FF₁₆) is written or until the reset is performed by using the flash memory reset bit.

Reading out the status register after the automatic programming operation is completed reports the result of it. For details, refer to the section on the status register.

Figure 9 shows an example of the programming flowchart.

Additional programming to any word that has already been programmed is prohibited.

Table 2. Software commands (CPU reprogramming mode)

Command	1st cycle			2nd cycle		
	Mode	Address	Data (D ₀ to D ₇)	Mode	Address	Data
Read Array	Write	X (Note 2)	FF ₁₆	—	—	—
Read Status Register	Write	X	70 ₁₆	Read	X	SRD (Note 3)
Clear Status Register	Write	X	50 ₁₆	—	—	—
Programming	Write	X	40 ₁₆	Write	WA (Note 4)	WD (Note 4)
Block Erase	Write	X	20 ₁₆	Write	BA (Note 5)	D0 ₁₆
Erase All Block	Write	X	20 ₁₆	Write	X	20 ₁₆

Notes 1: At software commands' input, the high-order byte of data (D₈–D₁₅) is ignored.

2: X = An arbitrary address in the user ROM area. (Note that A₀ = "0".)

3: SRD = Status Register Data

4: WA = Write Address, WD = Write Data (16 bits).

5: Block address: the maximum address of each block must be input. Note that address A₀ = "0".

Block Erase Command (20₁₆/D0₁₆)

Writing command code "20₁₆" at the 1st bus cycle and writing confirmation command code "D0₁₆" and the maximum address of the block (Note that address A₀ = "0".) at the subsequent 2nd bus cycle initiate the automatic erase (erasing and erase verification) operation for the specified block.

The completion of the automatic erase operation is confirmed by a read of the flash memory control register. The RY/ $\overline{\text{BY}}$ status bit of the flash memory control register goes "0" simultaneously with start of the automatic erase operation; and also, it goes "1" simultaneously with completion of it.

Before execution of the next command, be sure to confirm that the RY/ $\overline{\text{BY}}$ status bit is set to "1" (READY). During the automatic erase operation, writing of commands and access to the flash memory must not be performed.

Simultaneously with start of the automatic erase, the read status register mode is automatically active. In this case, the read status register mode is retained until the next read array command (FF₁₆) is written or until the reset is performed by using the flash memory reset bit.

Reading out the status register after the automatic erase operation is completed reports the result of it. For details, refer to the section on the status register.

Figure 10 shows an example of the block erase flowchart.

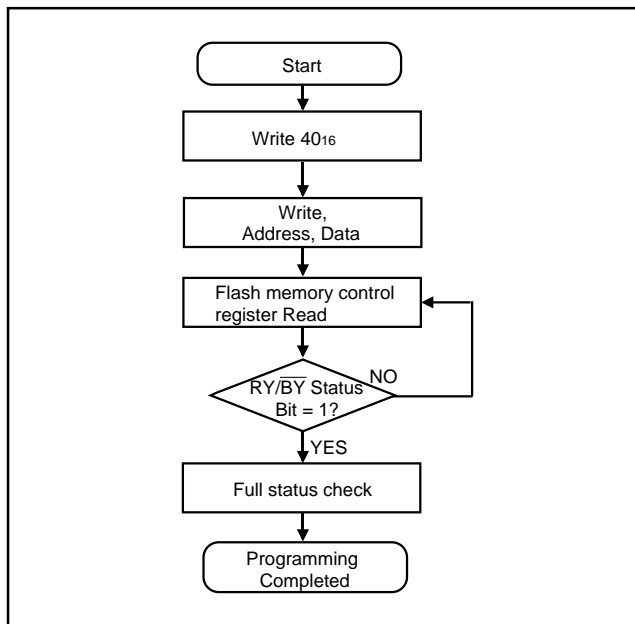


Fig. 9 Programming flowchart

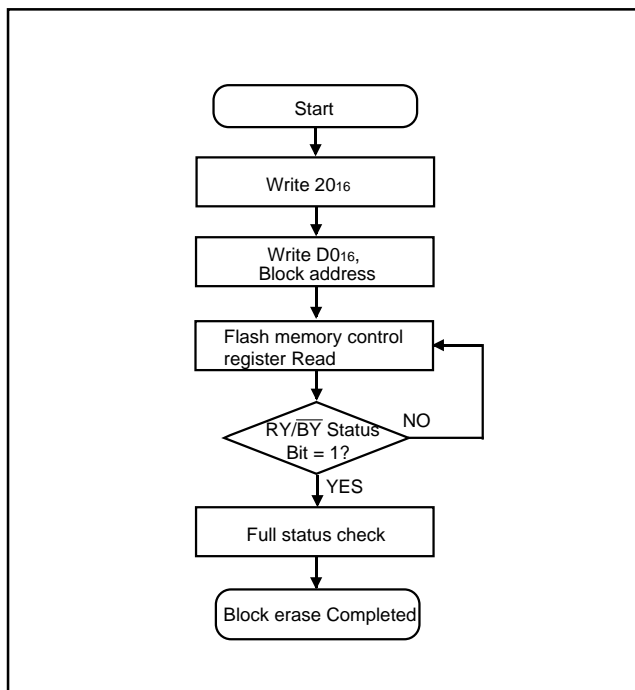


Fig. 10 Block erase flowchart

Erase All Block Command (2016/2016)

Writing command code "2016" at the 1st bus cycle and writing command code "2016" at the subsequent 2nd bus cycle initiate the continuous block erase (chip erase) operations for all the blocks.

The completion of the chip erase operation, as well as of the block erase operation, is confirmed by a read of the flash memory control register. The result of the automatic erase operation is also reported by a read of the status register.

During the automatic erase operation (when the RY/BY status bit = "0"), writing of commands and access to the flash memory must not be performed.

Status Register

The status register is used to indicate whether the programming/erase operation has been completed normally or terminated by an error. By writing the read status register command (7016), the contents of the status register can be read out; by writing the clear status register command (5016), the contents of the status register can be cleared.

Table 3 lists the definition of each bit of the status register.

The status register outputs "8016" after reset is removed.

The status of each bit is described below.

Erase Status Bit (SR.5)

This bit reports the status of the automatic erase operation. This bit is set to "1" if an erase error occurs and returns to "0" if the clear status register command (5016) is written.

Programming Status Bit (SR.4)

This bit reports the status of the automatic programming operation. This bit is set to "1" if a programming error occurs and returns to "0" if the clear status register command (5016) is written.

Under the condition that any of SR.5, SR.4 = "1", none of the programming, block erase, and erase all block commands can be accepted. Before execution of these commands, execute the clear status register command (5016), in advance, to clear these status bits.

Both of SR.4, SR.5 are set to "1" under the following conditions (Command Sequence Error):

- (1) when data other than "D016" and "FF16" is written to the data in the 2nd bus cycle of the block erase command (2016/D016)
- (2) when data other than "2016" and "FF16" is written to the data in the 2nd bus cycle of the erase all block command (2016/2016)

Note that, writing of "FF16" forces the microcomputer into the read array mode. Simultaneously with this, the command written in the 1st bus cycle will be canceled.

Full Status Check

The full status check reports the results of the erase or programming operation.

Figure 11 shows the full status check flowchart and actions to be taken if an error has occurred.

Table 3. Bit definition of status register

Symbol	Status	Definition	
		"1"	"0"
SR.7 (D7)	Reserved	—	—
SR.6 (D6)	Reserved	—	—
SR.5 (D5)	Erase Status	Terminated by error.	Terminated normally.
SR.4 (D4)	Programming Status	Terminated by error.	Terminated normally.
SR.3 (D3)	Reserved	—	—
SR.2 (D2)	Reserved	—	—
SR.1 (D1)	Reserved	—	—
SR.0 (D0)	Reserved	—	—

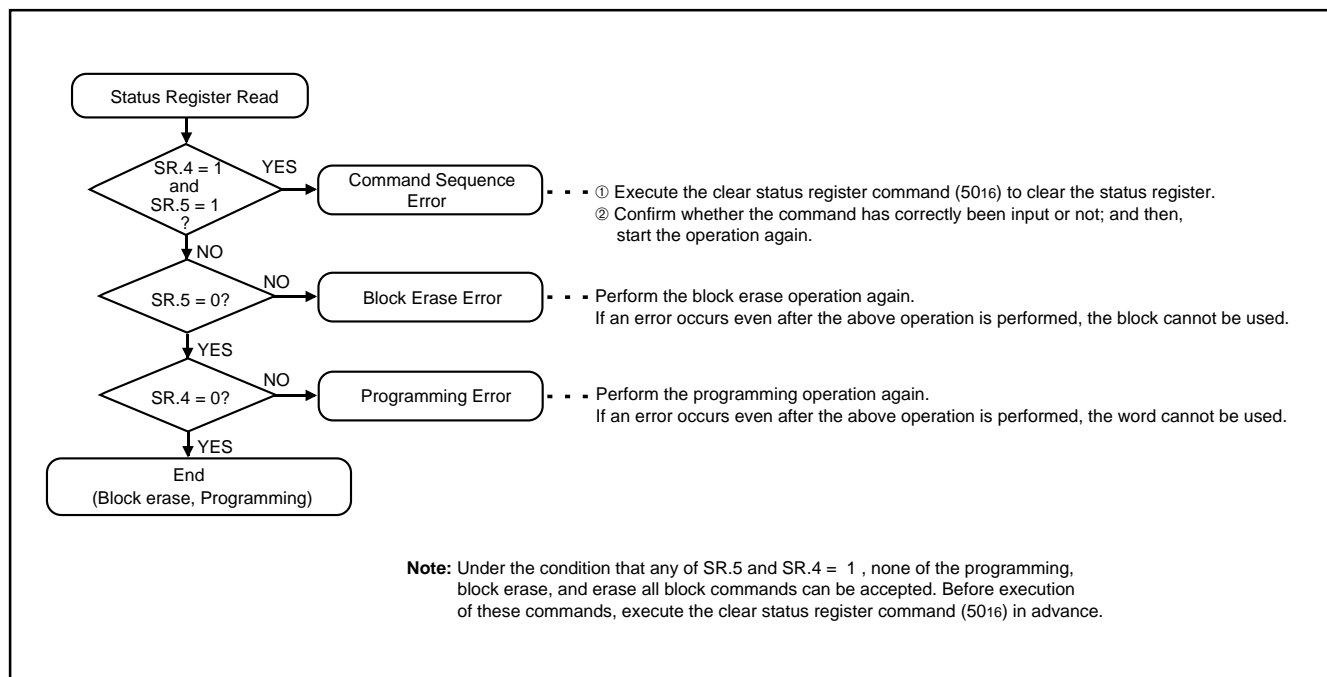


Fig. 11 Full status check flowchart and actions to be taken if an error has occurred

DC Electrical Characteristics (VCC = 5 V ± 0.5 V, Ta = 0 to 60 °C, f(fsyz) = 20 MHz (Note))

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Icc1	VCC power source current (at read)		30	48	mA
Icc2	VCC power source current (at write)			48	mA
Icc3	VCC power source current (at programming)			54	mA
Icc4	VCC power source current (at erasing)			54	mA

Limits of VIH, VIL, VOH, VOL, IiH, and IiL for each pin are the same as those in the microcomputer mode.

Note: f(fsyz) indicates the system clock (fsyz) frequency.

AC Electrical Characteristics (VCC = 5 V ± 0.5 V, Ta = 0 to 60 °C, f(fsyz) = 20 MHz (Note))

Parameter	Limits			Unit
	Min.	Typ.	Max.	
256-byte programming time		4	40	ms
Block erase time		0.6	8	s
Erase all block time		0.6 X n	8 X n	s

n = Number of blocks to be erased

The limits of parameters other than the above are same as those in the microcomputer mode.

Note: f(fsyz) indicates the system clock (fsyz) frequency.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V _{CC}	Power source voltage	−0.3 to 6.5	V
AV _{CC}	Analog power source voltage	−0.3 to 6.5	V
V _I	Input voltage P10–P17, P20–P27, P40–P47, P51–P53, P55–P57, P60–P67, P70–P77, P80–P83, P4OUTCUT, P6OUTCUT, VCONT, VREF, XIN, RESET, MD0, MD1	−0.3 to V _{CC} +0.3	V
V _O	Output voltage P10–P17, P20–P27, P40–P47, P51–P53, P55–P57, P60–P67, P70–P77, P80–P83, XOUT	−0.3 to V _{CC} +0.3	V
P _d	Power dissipation	300	mW
T _{opr}	Operating ambient temperature	−20 to 85	°C
T _{stg}	Storage temperature	−40 to 150	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 5 V, T_a = −20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{CC}	Power source voltage	4.5	5.0	5.5	V
AV _{CC}	Analog power source voltage		V _{CC}		V
V _{SS}	Power source voltage		0		V
AV _{SS}	Analog power source voltage		0		V
V _{IH}	High-level Input voltage P10–P17, P20–P27, P40–P47, P51–P53, P55–P57, P60–P67, P70–P77, P80–P83, P4OUTCUT, P6OUTCUT, XIN, RESET, MD0, MD1	0.8 V _{CC}		V _{CC}	V
V _{IL}	Low-level Input voltage P10–P17, P20–P27, P40–P47, P51–P53, P55–P57, P60–P67, P70–P77, P80–P83, P4OUTCUT, P6OUTCUT, XIN, RESET, MD0, MD1	0		0.2 V _{CC}	V
I _{OH} (peak)	High-level peak output current P10–P17, P20–P27, P55–P57, P60–P67, P70–P77			−10	mA
I _{OH} (avg)	High-level average output current P10–P17, P20–P27, P55–P57, P60–P67, P70–P77			−5	mA
I _{OL} (peak)	Low-level peak output current P10–P17, P20–P27, P51–P53, P55–P57, P70–P77			10	mA
I _{OL} (peak)	Low-level peak output current P40–P47, P60–P67			20	mA
I _{OL} (avg)	Low-level average output current P10–P17, P20–P27, P51–P53, P55–P57, P70–P77			5	mA
I _{OL} (avg)	Low-level average output current P40–P47, P60–P67			15	mA
f(XIN)	External clock input frequency (Note 1)			20	MHz
f(fsys)	System clock frequency			20	MHz

Notes 1: When using the PLL frequency multiplier, be sure that f(fsys) = 20 MHz or less.

2: Average output current is the average value of an interval of 100 ms.

3: The sum of I_{OL}(peak) must be 110 mA or less, the sum of I_{OH}(peak) must be 80 mA or less.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$, $f(f_{sys}) = 20\text{ MHz}$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	High-level output voltage P10–P17, P20–P27, P40–P47, P51–P53, P55–P57, P60–P67, P70–P77, P80–P83	$I_{OH} = -10\text{ mA}$	3			V
V_{OL}	Low-level output voltage P10–P17, P20–P27, P40–P47, P51–P53, P55–P57, P60–P67, P70–P77, P80–P83	$I_{OL} = 10\text{ mA}$			2	V
$V_{T+} - V_{T-}$	Hysteresis TA0IN–TA9IN, TA0OUT–TA9OUT, TB0IN–TB2IN, INT0–INT7, CTS0, CTS1, CTS2, CLK0, CLK1, CLK2, RxD0, RxD1, RxD2, RTPTRG0, RTPTRG1, P4OUTCUT, P6OUTCUT		0.4		1	V
$V_{T+} - V_{T-}$	Hysteresis $\overline{\text{RESET}}$		0.5		1.5	V
$V_{T+} - V_{T-}$	Hysteresis X_{IN}		0.1		0.3	V
I_{IH}	High-level input current P10–P17, P20–P27, P40–P47, P51–P53, P55–P57, P60–P67, P70–P77, P80–P83, P4OUTCUT, P6OUTCUT, X_{IN} , $\overline{\text{RESET}}$, MD0, MD1	$V_I = 5.0\text{ V}$			5	μA
I_{IL}	Low-level input current P10–P17, P20–P27, P40–P47, P51–P53, P55–P57, P60–P67, P70–P77, P80–P83, P4OUTCUT, P6OUTCUT, X_{IN} , $\overline{\text{RESET}}$, MD0, MD1	$V_I = 0\text{ V}$			–5	μA
VRAM	RAM hold voltage	When clock is stopped.	2			V
ICC	Power source current	Output-only pins are open, and the other pins are connected to V_{SS} or V_{CC} . An external square-waveform clock is input. (Pin X_{OUT} is open.) The PLL frequency multiplier is inactive.	$f(f_{sys}) = 20\text{ MHz}$. CPU is active.	25	50	mA
			$T_a = 25\text{ }^{\circ}\text{C}$ when clock is inactive.		1	μA
			$T_a = 85\text{ }^{\circ}\text{C}$ when clock is inactive.		20	

A-D CONVERTER CHARACTERISTICS

($V_{CC} = AV_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
	Resolution	$V_{REF} = V_{CC}$	A-D converter		10	Bits
			Comparator		$\frac{1}{256} V_{REF}$	V
	Absolute accuracy	$V_{REF} = V_{CC}$	10-bit resolution mode		± 3	LSB
			8-bit resolution mode		± 2	LSB
			Comparator		± 40	mV
RLADDER	Ladder resistance	$V_{REF} = V_{CC}$	5			k Ω
tCONV	Conversion time	$f(f_{sys}) \leq 20\text{ MHz}$	10-bit resolution mode		5.9	μs
			8-bit resolution mode		2.45 (Note)	
			Comparator		0.7 (Note)	
VREF	Reference voltage		2.7		V_{CC}	V
VIA	Analog input voltage		0		V_{REF}	V

Note: This is applied when A-D conversion frequency (ϕ_{AD}) = f_1 (ϕ).

D-A CONVERTER CHARACTERISTICS

($V_{CC} = 5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $V_{REF} = 5\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
	Resolution				8	Bits
	Absolute accuracy				± 1.0	%
t _{su}	Set time				3	μs
R _O	Output resistance		2	3.5	4.5	k Ω
I _{VREF}	Reference power source input current	(Note)			3.2	mA

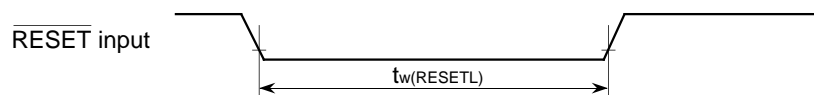
Note: The test conditions are as follows:

- One D-A converter is used.
- The D-A register value of the unused D-A converter is "0016."
- The reference power source input current for the ladder resistance of the A-D converter is excluded.

RESET INPUT

Reset input timing requirements ($V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESETL)	RESET input low-level pulse width	10			μs



PERIPHERAL DEVICE INPUT/OUTPUT TIMING

(VCC = 5 V±0.5 V, VSS = 0 V, Ta = -20 to 85 °C, f(fsyst) = 20 MHz unless otherwise noted)

* For limits depending on f(fsyst), their calculation formulas are shown below. Also, the values at f(fsyst) = 20 MHz are shown in ().

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TA)	TAiN input cycle time	80		ns
tw(TAH)	TAiN input high-level pulse width	40		ns
tw(TAL)	TAiN input low-level pulse width	40		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
tc(TA)	TAiN input cycle time	f(fsyst) ≤ 20 MHz	$\frac{16 \times 10^9}{f(fsyst)}$ (800)		ns
tw(TAH)	TAiN input high-level pulse width	f(fsyst) ≤ 20 MHz	$\frac{8 \times 10^9}{f(fsyst)}$ (400)		ns
tw(TAL)	TAiN input low-level pulse width	f(fsyst) ≤ 20 MHz	$\frac{8 \times 10^9}{f(fsyst)}$ (400)		ns

Note : The TAiN input cycle time requires 4 or more cycles of a count source. The TAiN input high-level pulse width and the TAiN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f2 at f(fsyst) ≤ 20 MHz.

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
tc(TA)	TAiN input cycle time	f(fsyst) ≤ 20 MHz	$\frac{8 \times 10^9}{f(fsyst)}$ (400)		ns
tw(TAH)	TAiN input high-level pulse width		80		ns
tw(TAL)	TAiN input low-level pulse width		80		ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tw(TAH)	TAiN input high-level pulse width	80		ns
tw(TAL)	TAiN input low-level pulse width	80		ns

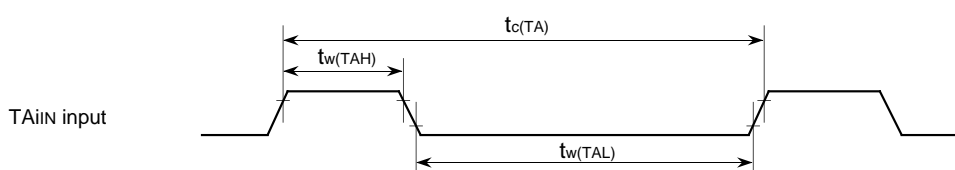
Timer A input (Up-down input and Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high-level pulse width	1000		ns
tw(UPL)	TAiOUT input low-level pulse width	1000		ns
tsu(UP-TiN)	TAiOUT input setup time	400		ns
th(TiN-UP)	TAiOUT input hold time	400		ns

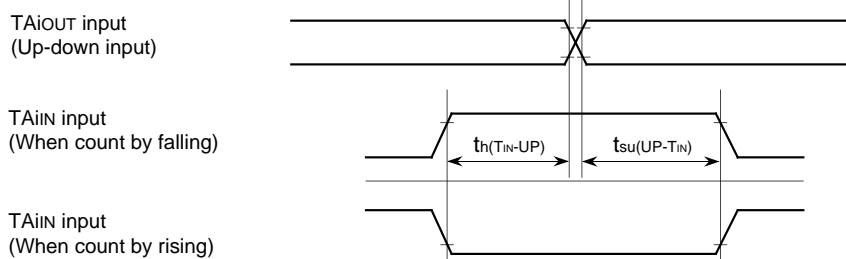
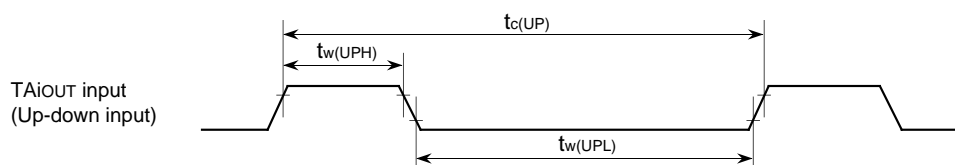
Timer A input (Two-phase pulse input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c(TA)$	TAjIN input cycle time	800		ns
$t_{su}(TA_{jIN}-TA_{jOUT})$	TAjIN input setup time	200		ns
$t_{su}(TA_{jOUT}-TA_{jIN})$	TAjOUT input setup time	200		ns

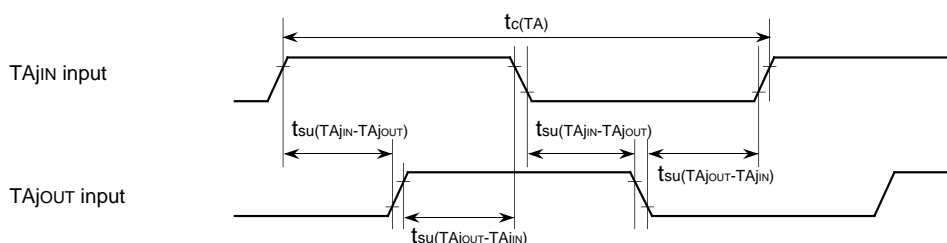
- Gating input in timer mode
- Count input in event counter mode
- External trigger input in one-shot pulse mode
- External trigger input in pulse width modulation mode



- Up-down and Count input in event counter mode



- Two-phase pulse input in event counter mode



Test conditions

- $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$
- Input timing voltage : $V_{IL} = 1.0\text{ V}$, $V_{IH} = 4.0\text{ V}$

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiN input cycle time (one edge count)	80		ns
$t_{w(TBH)}$	TBiN input high-level pulse width (one edge count)	40		ns
$t_{w(TBL)}$	TBiN input low-level pulse width (one edge count)	40		ns
$t_{c(TB)}$	TBiN input cycle time (both edge count)	160		ns
$t_{w(TBH)}$	TBiN input high-level pulse width (both edge count)	80		ns
$t_{w(TBL)}$	TBiN input low-level pulse width (both edge count)	80		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
$t_{c(TB)}$	TBiN input cycle time	$f(f_{sys}) \leq 20 \text{ MHz}$	$\frac{16 \times 10^9}{f(f_{sys})}$ (800)		ns
$t_{w(TBH)}$	TBiN input high-level pulse width	$f(f_{sys}) \leq 20 \text{ MHz}$	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns
$t_{w(TBL)}$	TBiN input low-level pulse width	$f(f_{sys}) \leq 20 \text{ MHz}$	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns

Note: The TBiN input cycle time requires 4 or more cycles of a count source. The TBiN input high-level pulse width and the TBiN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f₂ at $f(f_{sys}) \leq 20 \text{ MHz}$.

Timer B input (Pulse width measurement mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
$t_{c(TB)}$	TBiN input cycle time	$f(f_{sys}) \leq 20 \text{ MHz}$	$\frac{16 \times 10^9}{f(f_{sys})}$ (800)		ns
$t_{w(TBH)}$	TBiN input high-level pulse width	$f(f_{sys}) \leq 20 \text{ MHz}$	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns
$t_{w(TBL)}$	TBiN input low-level pulse width	$f(f_{sys}) \leq 20 \text{ MHz}$	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns

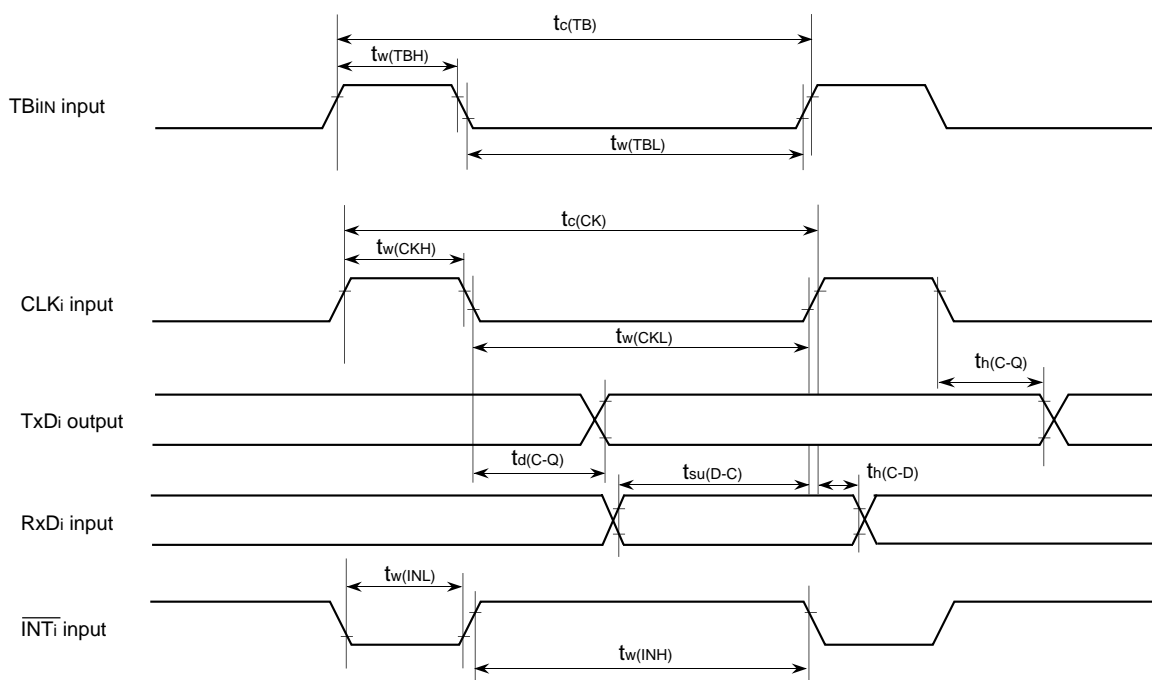
Note: The TBiN input cycle time requires 4 or more cycles of a count source. The TBiN input high-level pulse width and the TBiN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f₂ at $f(f_{sys}) \leq 20 \text{ MHz}$.

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK _i input cycle time	200		ns
$t_{w(CKH)}$	CLK _i input high-level pulse width	100		ns
$t_{w(CKL)}$	CLK _i input low-level pulse width	100		ns
$t_{d(C-Q)}$	TxD _i output delay time		80	ns
$t_{h(C-Q)}$	TxD _i hold time	0		ns
$t_{su(D-C)}$	RxD _i input setup time	20		ns
$t_{h(C-D)}$	RxD _i input hold time	90		ns

External interrupt ($\overline{\text{INTi}}$) input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_w(\text{INH})$	$\overline{\text{INTi}}$ input high-level pulse width	250		ns
$t_w(\text{INL})$	$\overline{\text{INTi}}$ input low-level pulse width	250		ns



Test conditions

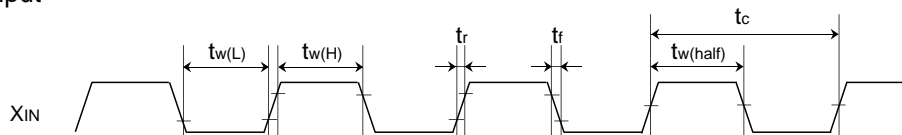
- $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$, $T_a = -20 \text{ to } 85 \text{ }^\circ\text{C}$
- Input timing voltage : $V_{IL} = 1.0 \text{ V}$, $V_{IH} = 4.0 \text{ V}$
- Output timing voltage : $V_{OL} = 0.8 \text{ V}$, $V_{OH} = 2.0 \text{ V}$, $C_L = 50 \text{ pF}$

External clock input

Timing Requirements ($V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(\text{half})}$	External clock input pulse width with half input-voltage	$0.45\ t_c$	$0.55\ t_c$	ns
$t_{w(\text{H})}$	External clock input high-level pulse width	$0.5\ t_c - 8$		ns
$t_{w(\text{L})}$	External clock input low-level pulse width	$0.5\ t_c - 8$		ns
t_r	External clock input rise time		8	ns
t_f	External clock input fall time		8	ns

External clock input



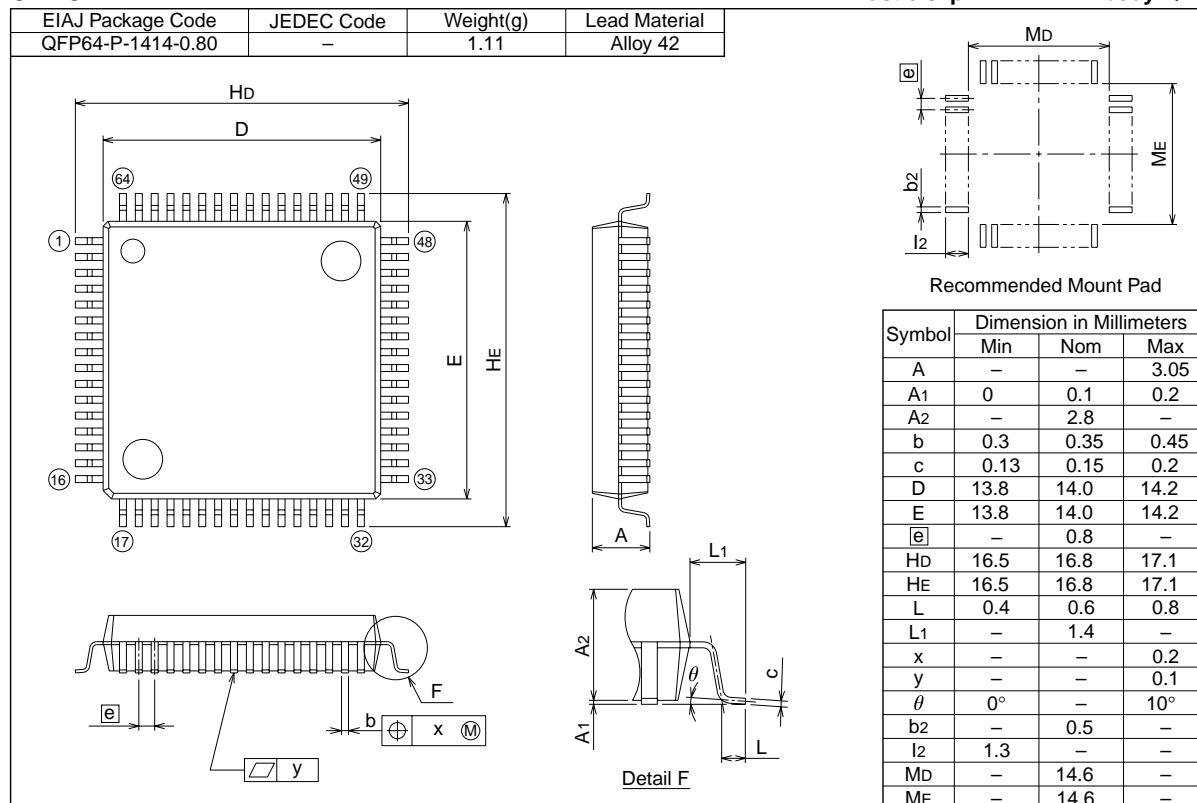
Test conditions

- $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $T_a = -20\text{ to }85\text{ }^{\circ}\text{C}$
- Input timing voltage : $V_{IL} = 1.0\text{ V}$, $V_{IH} = 4.0\text{ V}$ ($t_{w(\text{H})}$, $t_{w(\text{L})}$, t_r , t_f)
- Output timing voltage : 2.5 V (t_c , $t_{w(\text{half})}$)

PACKAGE OUTLINE

64P6N-A

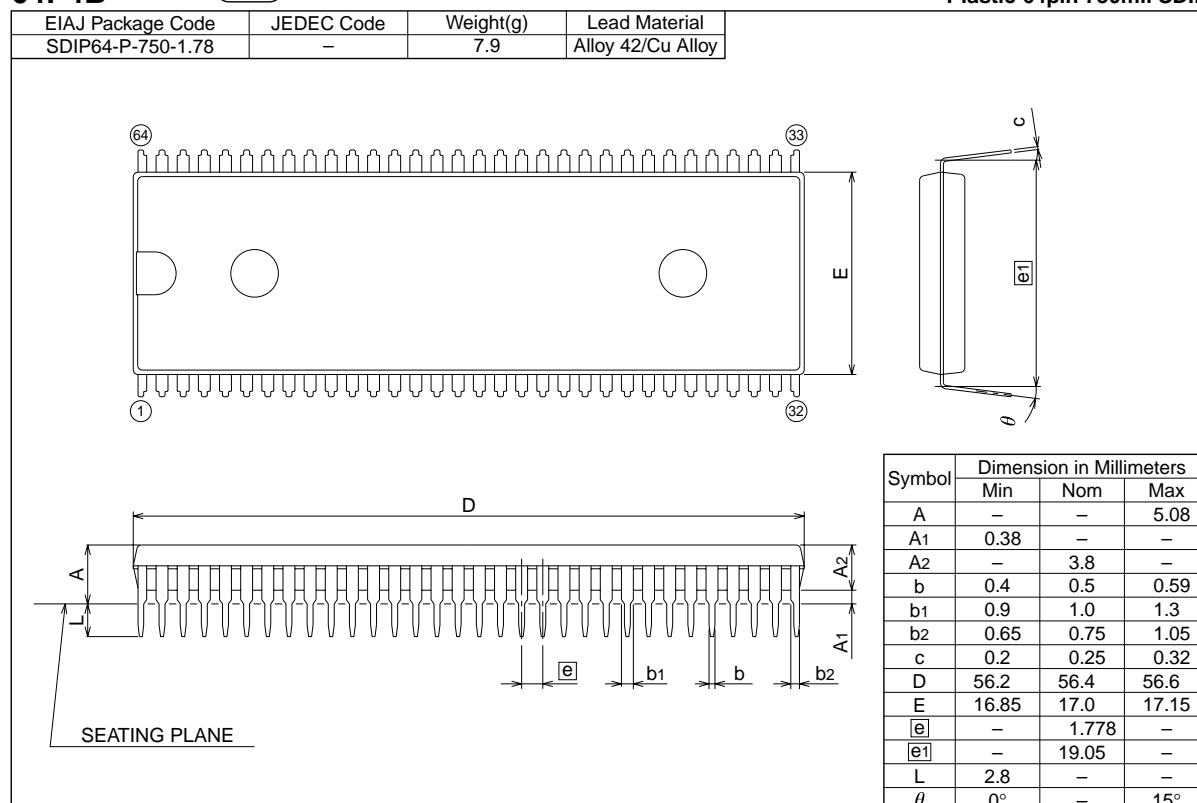
Plastic 64pin 14X14mm body QFP



64P4B

(MMP)

Plastic 64pin 750mil SDIP



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS

M37905F8CFP, M37905F8CSP

16-BIT CMOS MICROCOMPUTER

Renesas Technology Corp.

Nippon Bldg., 6-2, Otemachi 2-chome, Chiyoda-ku, Tokyo, 100-0004 Japan

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REVISION HISTORY	M37905F8CFP, M37905F8CSP DATASHEET
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Rev.	Date	Description	
		Page	Summary
1.0	5/28/01	—	First Edition