National Semiconductor

MICROCIRCUIT DATA SHEET

MJLM193-X REV 1A1

Original Creation Date: 05/04/95
Last Update Date: 05/24/01
Last Major Revision Date: 05/18/01

LOW POWER LOW OFFSET VOLTAGE DUAL COMPARATORS

General Description

The LM193 consists of two independent precision voltage comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

Industry Part Number

LM193

NS Part Numbers

JL193BGA
JL193BPA

Prime Die

LM193

Controlling Document

38510/11202, AMEND. 2 REV A

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Wide supply voltage range 5.0Vdc to 36Vdc
  ±2.5Vdc to ±18Vdc
- Very low supply current drain (0.4mA Typ)
  independent of supply voltage
- Low input biasing current 25nA Typ
- Low input offset current ±3nA Typ
  and maximum offset voltage +5mV Max (25 C)
- Input common-mode voltage range includes ground
- Differential input voltage range
  equal to the power supply voltage
- Low output saturation voltage 250mV at 4mA Typ
- Output voltage compatible with TTL,
  DTL, ECL, MOS and CMOS logic systems

(Absolute Maximum Ratings)

Supply Voltage, V+	36Vdc or ±18Vdc
Differential Input Voltage (Note 3)	36V
Output Voltage	36V
Input Voltage	-0.3V to +36V
Input Current (Vin < -0.3Vdc) (Note 2)	50mA
Power Dissipation	
METAL CAN	330mW at TA = 125 C
CERDIP	400mW at TA = 125 C
Maximum Junction Temperature	175 C
Output Short-Circuit to GND (Note 1)	Continuous
Operating Temperature Range	-55 C ≤ Ta ≤ +125 C
Thermal Resistance	
ThetaJA	
CERDIP	
(Still Air)	146 C/W
(500 LF/Min Air Flow)	85 C/W
METAL CAN	
(Still Air)	174 C/W
(500 LF/Min Air Flow)	99 C/W
ThetaJC	
CERDIP	33 C/W
METAL CAN	44 C/W
Storage Temperature Range	-65 C ≤ Ta ≤ +150 C
Soldering Information	
Soldering, (10 seconds)	260 C
ESD Tolerance (Note 4)	500V

Note 1: Short circuits from the output to V+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20mA independent of the magnitude of V+.

Note 2: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3Vdc.

Note 3: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3Vdc (or 0.3Vdc below the magnitude of the negative power supply, if used).

Note 4: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	+Vcc = 30V, -Vcc = 0V, Vo = 15V			-5	5	mV	1
					-7	7	mV	2, 3
		+Vcc = 2V, -Vcc = -28V, Vo = -13V			-5	5	mV	1
					-7	7	mV	2, 3
		+Vcc = 5V, -Vcc = 0V, Vo = 1.4V			-5	5	mV	1
					-7	7	mV	2, 3
		+Vcc = 2V, -Vcc = -3V, Vo = -1.6V			-5	5	mV	1
					-7	7	mV	2, 3
Iio	Input offset Current	+Vcc = 30V, -Vcc = 0V, Vo = 15V, Rs = 20K Ohms	1		-25	25	nA	1, 2
			1		-75	75	nA	3
		+Vcc = 2V, -Vcc = -28V, Vo = -13V, Rs = 20K Ohms	1		-25	25	nA	1, 2
			1		-75	75	nA	3
		+Vcc = 5V, -Vcc = 0V, Vo = 1.4V, Rs = 20K Ohms	1		-25	25	nA	1, 2
			1		-75	75	nA	3
		+Vcc = 2V, -Vcc = -3V, Vo = -1.6V, Rs = 20K Ohms	1		-25	25	nA	1, 2
			1		-75	75	nA	3
+Iib	Input Bias Current	+Vcc = 30V, -Vcc = 0V, Vo = 15V, Rs = 20K Ohms	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3
		+Vcc = 2V, -Vcc = -28V, Vo = -13V, Rs = 20K Ohms	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3
		+Vcc = 5V, -Vcc = 0V, Vo = 1.4V, Rs = 20K Ohms	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3
		+Vcc = 2V, -Vcc = -3V, Vo = -1.6V, Rs = 20K Ohms	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3

Electrical Characteristics

DC PARAMETERS(Continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
-Iib	Input Bias Current	+Vcc = 30V, -Vcc = 0V, Vo = 15V, Rs = 20K Ohms	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3
		+Vcc = 2V, -Vcc = -28V, Vo = -13V Rs = 20K Ohms	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3
		+Vcc = 5V, -Vcc = 0V, Vo = 1.4V, Rs = 20K Ohms	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3
		+Vcc = 2V, -Vcc = -3V, Vo = -1.6V, Rs = 20K Ohms	1		-100	+0.1	nA	1, 2
			1		-200	+0.1	nA	3
CMR	Input Voltage Common Mode Rejection	2V≤ +Vcc ≤30V, -28V≤ -Vcc ≤0V, -13V≤ Vo ≤15V			76		dB	1, 2, 3
		2V≤ +Vcc ≤5V, -3V≤ -Vcc ≤0V, -1.6V≤ Vo ≤1.4V			70		dB	1, 2, 3
ICEX	Output Leakage Current	+Vcc = 30V, -Vcc = 0V, Vo = +30V				1	uA	1, 2, 3
+Iil	Input Leakage Current	+Vcc=36V, -Vcc=0V, V+i=34V, V-i=0V			-500	500	nA	1, 2, 3
-Iil	Input Leakage Current	+Vcc=36V, -Vcc=0V, V+i=0V, V-i=34V			-500	500	nA	1, 2, 3
Vol	Logical "0" Output Voltage	+Vcc = 4.5V, -Vcc = 0V, Io = 4mA				.4	V	1
						.7	V	2, 3
		+Vcc = 4.5V, -Vcc = 0V, Io = 8mA				1.5	V	1
						2	V	2, 3
Icc	Power Supply Current	+Vcc = 5V, -Vcc = 0V, Vid = 15mV				2	mA	1, 2
						3	mA	3
		+Vcc = 30V, -Vcc = 0V, Vid = 15mV				3	mA	1, 2
						4	mA	3
DELTA Vio/ DELTA T	Temperature Coefficient of Input Offset Voltage	25 C ≤ TA ≤ +125 C	2		-25	25	uV/C	2
		-55 C ≤ TA ≤ 25 C	2		-25	25	uV/C	3
DELTA Iio/ DELTA T	Temperature Coefficient of Input Offset Current	25 C ≤ TA ≤ +125 C	2		-300	300	pA/C	2
		-55 C ≤ TA ≤ 25 C	2		-400	400	pA/C	3
AVS	Open Loop Voltage Gain	+Vcc = 15V, -Vcc = 0V, RL = 15K Ohms, 1V ≤ Vo ≤ 11V	3		50		V/mV	4
			3		25		V/mV	5, 6

Electrical Characteristics

DC PARAMETERS(Continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
VLAT	Voltage Latch (Logical "1" Input)	+Vcc=5V, -Vcc=0V, Vin=10V, Io=4mA				.4	V	9

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: +Vcc = 5V, -Vcc = 0V

tRLH	Response Time	Vin = 100mV, RL = 5.1K Ohms, Vod = 5mV	4			5	uS	7, 8B
			4			7	uS	8A
		Vin=100mV, RL=5.1K Ohms, Vod=50mV	4			.8	uS	7, 8B
			4			1.2	uS	8A
tRHL	Response Time	Vin = 100mV, RL = 5.1K Ohms, Vod = 5mV	4			2.5	uS	7, 8B
			4			3	uS	8A
		Vin=100mV, RL=5.1K Ohms, Vod=50mV	4			.8	uS	7, 8B
			4			1	uS	8A
CS	Channel Separation	+Vcc = 20V, -Vcc = -10V, A to B	4		80		dB	7
		+Vcc = 20V, -Vcc = -10V, B to A	4		80		dB	7

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: "Delta calculations performed at Group B-5".

Vio	Input Offset Voltage	+Vcc = 30V, -Vcc = 0V, Vo = 15V			-1	1	mV	1
+Iib	Input Bias Current	+Vcc = 30V, -Vcc = 0V, Vo = 15V, Rs = 20K Ohms			-15	15	nA	1
-Iib	Input Bias Current	+Vcc = 30V, -Vcc = 0V, Vo = 15V, Rs = 20K Ohms			-15	15	nA	1

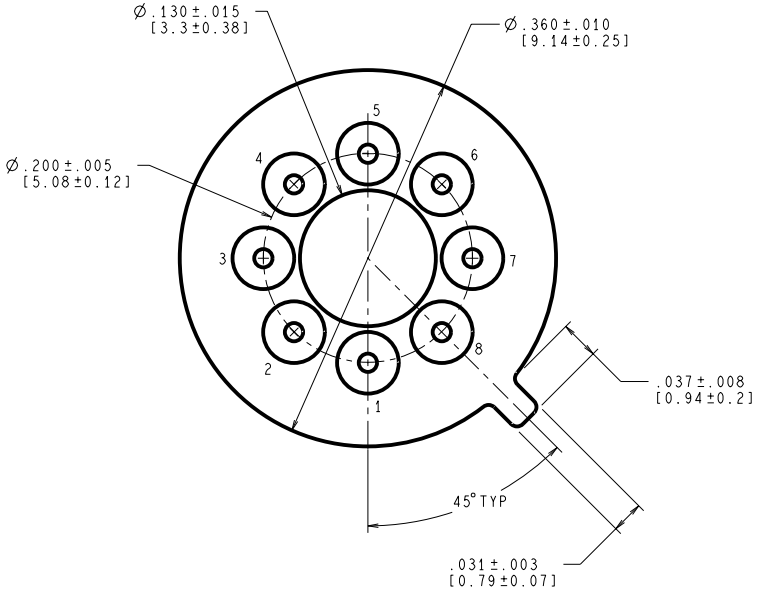
Note 1: S/S Rs = 20K Ohm, tested with Rs = 100K Ohm for better resolution.
Note 2: Calculated parameter for Delta Vio/Delta T and Delta Iio/Delta T
Note 3: K in datalog is equivalent to V/mV in units column.
Note 4: Bench tested

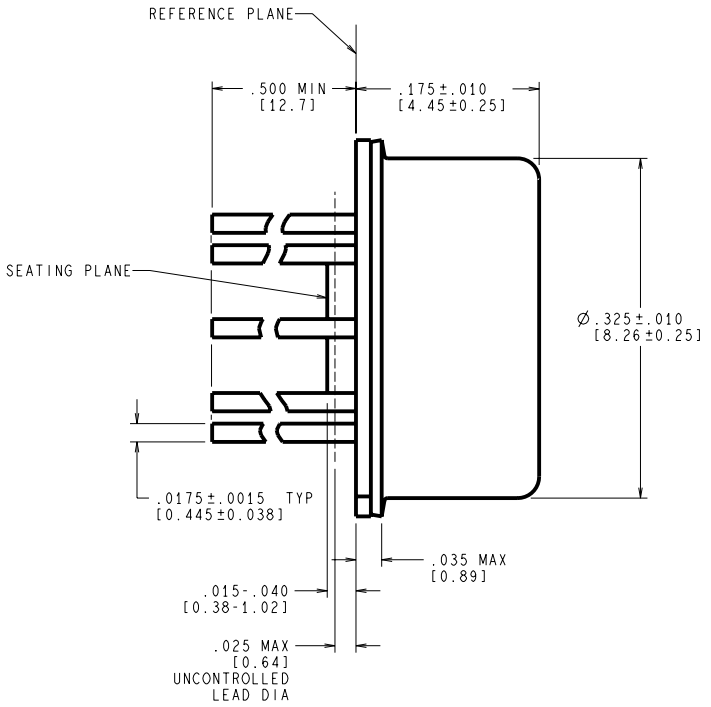
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05327HRB3	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (B/I CKT)
05425HRB3	CERDIP (J), 8 LEAD (B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000171A	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (PINOUT)
P000172B	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	

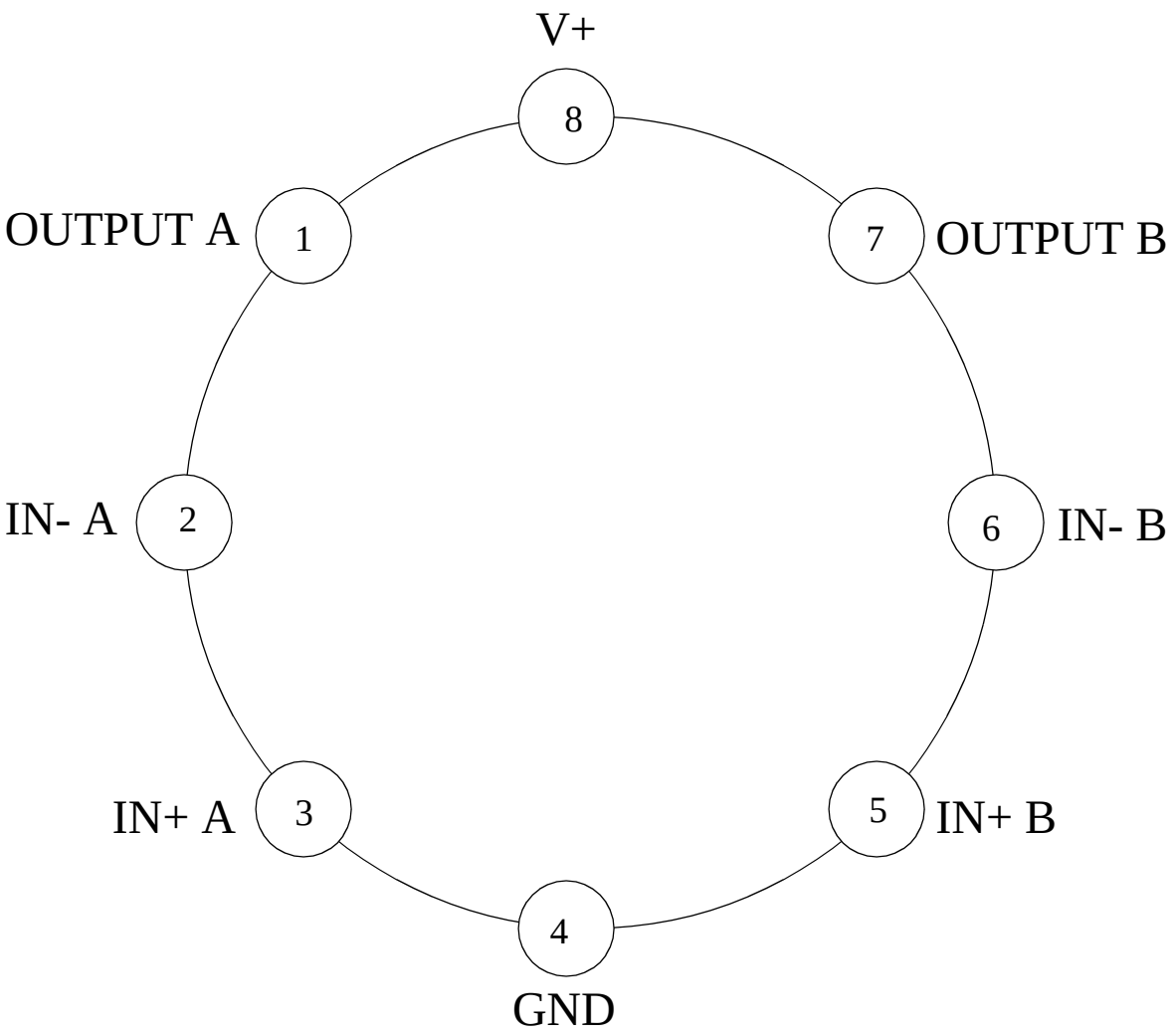
PROJECTION — INCH [MM]

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

METAL CAN, TO-99, 8 LEAD, .200 DIA P.C.

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING — SHEET 1 of 1



LM193AH, LM193H

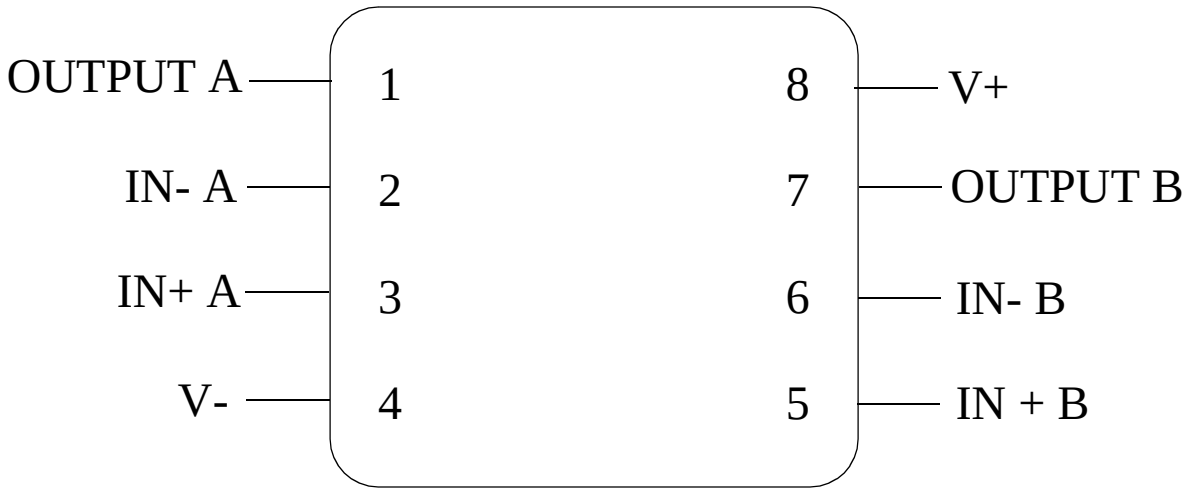
8 - PIN METAL CAN

CONNECTION DIAGRAM

TOP VIEW

P000171A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM193J, LM193AJ

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000172B

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A1	M0003804	05/24/01	Rose Malone	UPDATE MDS: MJLM193-X, Rev. 0B0 to MJLM193-X, Rev. 1A1. Corrected Icc Max limit from 3.5mA to 3mA in Electrical Section. Added graphics to Graphics Section.