

# SN54ALS1034, SN54AS1034A, SN74ALS1034, SN74AS1034A HEX DRIVERS

SDAS053B – APRIL 1982 – REVISED JANUARY 1995

- 'AS1034A Offer High Capacitive-Drive Capability
- Noninverting Drivers
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

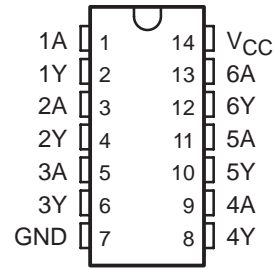
These devices contain six independent noninverting drivers. They perform the Boolean function  $Y = A$ .

The SN54ALS1034 and SN54AS1034A are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS1034 and SN74AS1034A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

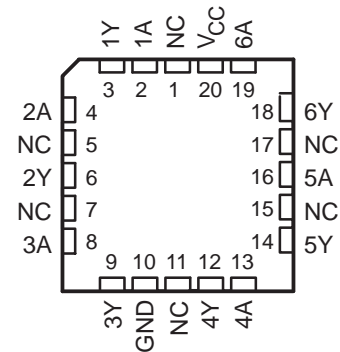
FUNCTION TABLE  
(each buffer)

INPUT A	OUTPUT Y
H	H
L	L

SN54ALS1034, SN54AS1034A . . . J PACKAGE  
SN74ALS1034, SN74AS1034A . . . D OR N PACKAGE  
(TOP VIEW)

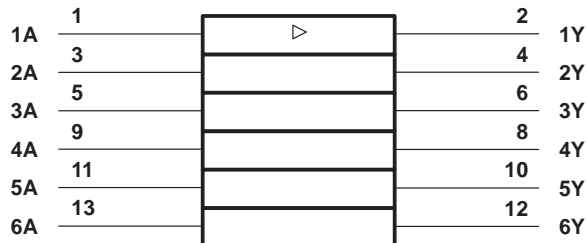


SN54ALS1034, SN54AS1034A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

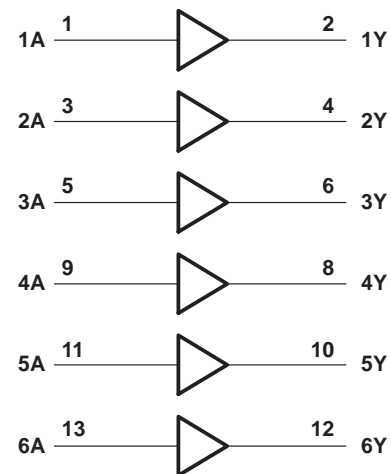
## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)



# SN54ALS1034, SN54AS1034A, SN74ALS1034, SN74AS1034A

## HEX DRIVERS

SDAS053B – APRIL 1982 – REVISED JANUARY 1995

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54ALS1034	–55°C to 125°C
SN74ALS1034	0°C to 70°C
Storage temperature range	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

		SN54ALS1034			SN74ALS1034			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			–12			–15	mA
$I_{OL}$	Low-level output current			12			24	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS1034			SN74ALS1034			UNIT
			MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IK}$	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			–1.2			–1.2	V
$V_{OH}$	$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -0.4$ mA	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	2.4	3.2		2.4	3.2		
		$I_{OH} = -12$ mA	2						
		$I_{OH} = -15$ mA				2			
$V_{OL}$	$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA		0.25	0.4				V
		$I_{OL} = 24$ mA				0.35	0.5		
$I_I$	$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20			20	μA
$I_{IL}$	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			–0.1			–0.1	mA
$I_{O}^{\S}$	$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	–20		–112	–30		–112	mA
$I_{CCH}$	$V_{CC} = 5.5$ V,	$V_I = 4.5$ V		3	6		3	6	mA
$I_{CCL}$	$V_{CC} = 5.5$ V,	$V_I = 0$		8	14		8	14	mA

<sup>‡</sup> All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

<sup>\S</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



# SN54ALS1034, SN54AS1034A, SN74ALS1034, SN74AS1034A HEX DRIVERS

SDAS053B – APRIL 1982 – REVISED JANUARY 1995

## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 4.5 V to 5.5 V, CL = 50 pF, RL = 500 Ω, TA = MIN to MAX†				UNIT
			SN54ALS1034		SN74ALS1034		
			MIN	MAX	MIN	MAX	
tPLH	A	Y	1	11	1	8	ns
tPHL			1	13	1	8	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub>	7 V
Operating free-air temperature range, T <sub>A</sub> : SN54AS1034A	–55°C to 125°C
SN74AS1034A	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions§

		SN54AS1034A			SN74AS1034A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			–40			–48	mA
I <sub>OL</sub>	Low-level output current			40			48	mA
T <sub>A</sub>	Operating free-air temperature	–55		125	0		70	°C

§ These high sink- or source-current devices are not recommended for use above 40 MHz.



# SN54ALS1034, SN54AS1034A, SN74ALS1034, SN74AS1034A HEX DRIVERS

SDAS053B – APRIL 1982 – REVISED JANUARY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS1034A			SN74AS1034A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = −18 mA		−1.2			−1.2			V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = −2 mA		V <sub>CC</sub> − 2			V <sub>CC</sub> − 2			V
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = −3 mA	2.4	3.2	2.4	3.2			
		I <sub>OH</sub> = −40 mA	2						
		I <sub>OH</sub> = −48 mA			2				
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 40 mA	0.25 0.5					V	
		I <sub>OL</sub> = 48 mA			0.35 0.5				
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V	0.1			0.1			mA	
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V	20			20			μA	
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V	−0.5			−0.5			mA	
I <sub>O</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	−50	−200		−50	−200		mA	
I <sub>CCH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 4.5 V	9 15		9 15		mA			
I <sub>CCL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0	21 35		21 35		mA			

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

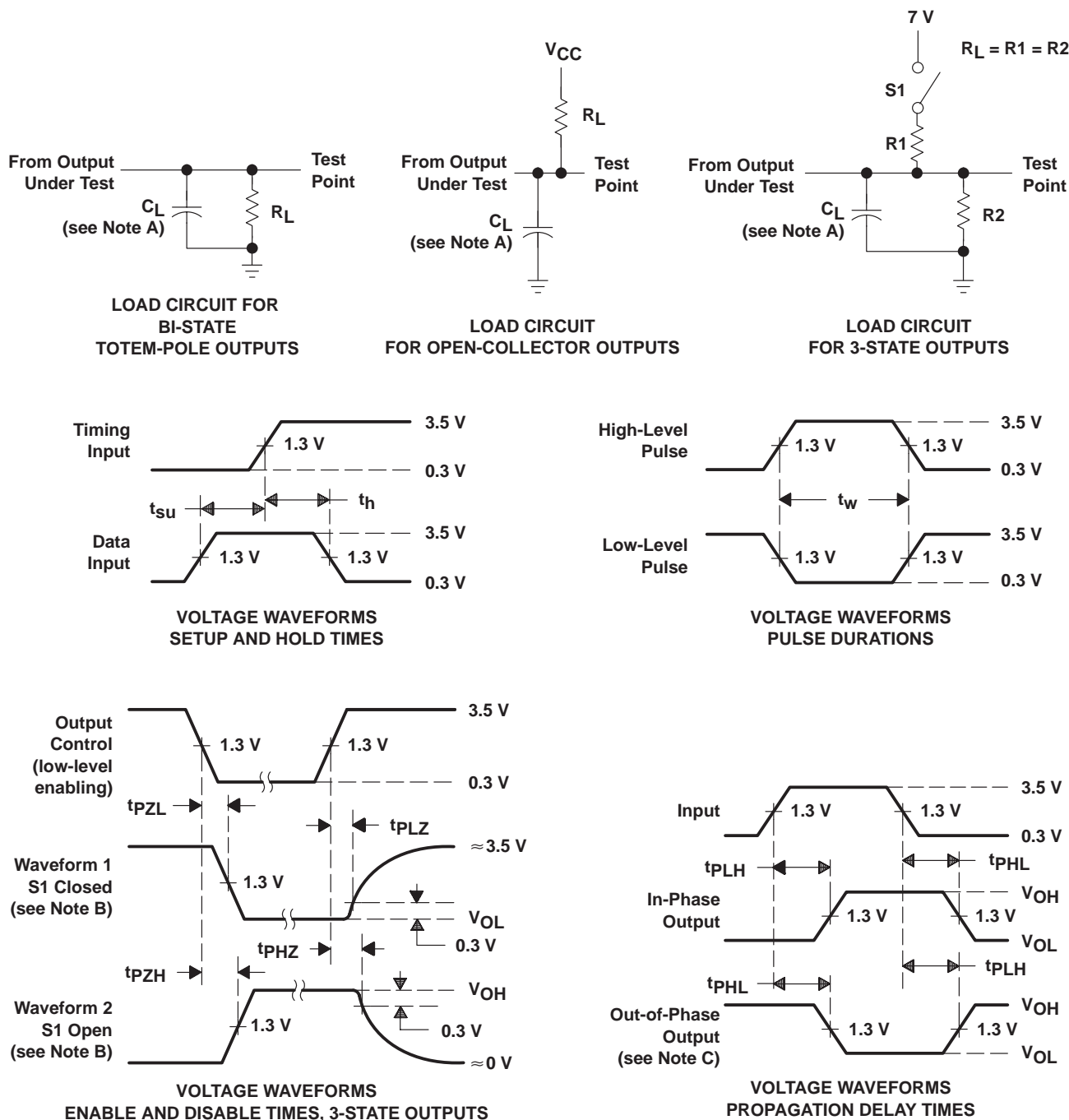
## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX§				UNIT
			SN54AS1034A		SN74AS1034A		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	1	6.5	1	6	ns
t <sub>PHL</sub>			1	6.5	1	6	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88731012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 88731012A SNJ54AS 1034AFK	<a href="#">Samples</a>
5962-8873101CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8873101CA SNJ54AS1034AJ	<a href="#">Samples</a>
5962-8873101DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8873101DA SNJ54AS1034AW	<a href="#">Samples</a>
84031012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84031012A SNJ54ALS 1034FK	<a href="#">Samples</a>
8403101CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8403101CA SNJ54ALS1034J	<a href="#">Samples</a>
8403101DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8403101DA SNJ54ALS1034W	<a href="#">Samples</a>
JM38510/38411B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 38411B2A	<a href="#">Samples</a>
JM38510/38411BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 38411BCA	<a href="#">Samples</a>
M38510/38411B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 38411B2A	<a href="#">Samples</a>
M38510/38411BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 38411BCA	<a href="#">Samples</a>
SN54ALS1034J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54ALS1034J	<a href="#">Samples</a>
SN54AS1034AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54AS1034AJ	<a href="#">Samples</a>
SN74ALS1034D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS1034	<a href="#">Samples</a>
SN74ALS1034DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS1034	<a href="#">Samples</a>
SN74ALS1034DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS1034	<a href="#">Samples</a>
SN74ALS1034DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS1034	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS1034DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS1034	<a href="#">Samples</a>
SN74ALS1034N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS1034N	<a href="#">Samples</a>
SN74ALS1034NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS1034	<a href="#">Samples</a>
SN74AS1034AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS1034A	<a href="#">Samples</a>
SN74AS1034ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS1034A	<a href="#">Samples</a>
SN74AS1034ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS1034A	<a href="#">Samples</a>
SN74AS1034ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS1034A	<a href="#">Samples</a>
SN74AS1034AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS1034AN	<a href="#">Samples</a>
SNJ54ALS1034FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84031012A SNJ54ALS 1034FK	<a href="#">Samples</a>
SNJ54ALS1034J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8403101CA SNJ54ALS1034J	<a href="#">Samples</a>
SNJ54ALS1034W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8403101DA SNJ54ALS1034W	<a href="#">Samples</a>
SNJ54AS1034AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 88731012A SNJ54AS 1034AFK	<a href="#">Samples</a>
SNJ54AS1034AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8873101CA SNJ54AS1034AJ	<a href="#">Samples</a>
SNJ54AS1034AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8873101DA SNJ54AS1034AW	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ALS1034, SN54AS1034A, SN74ALS1034, SN74AS1034A :**

● Catalog: [SN74ALS1034](#), [SN74AS1034A](#)

● Military: [SN54ALS1034](#), [SN54AS1034A](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product



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- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS1034DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ALS1034NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AS1034ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS1034DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74ALS1034NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74AS1034ADR	SOIC	D	14	2500	367.0	367.0	38.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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