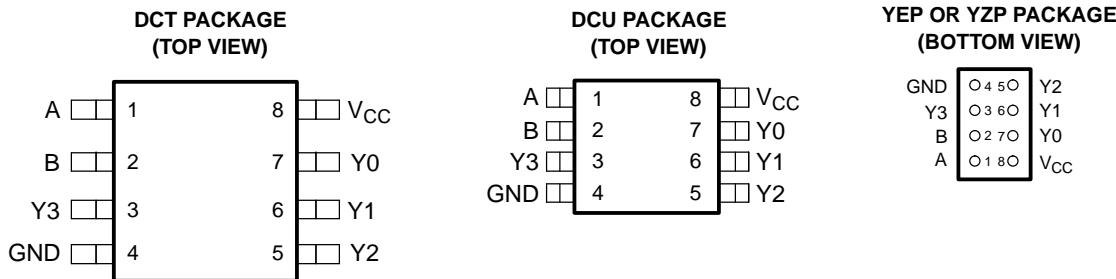


## FEATURES

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.9 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

## DESCRIPTION/ORDERING INFORMATION

This 2-to-4 line decoder is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC1G139 2-line to 4-line decoder is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
$-40^\circ\text{C}$ to $85^\circ\text{C}$	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Reel of 3000	SN74LVC1G139YEPR _ _ _ C9 _
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		
	SSOP – DCT	Reel of 3000	SN74LVC1G139DCTR C39 _ _
		Reel of 250	
	VSSOP – DCU	Reel of 3000	SN74LVC1G139DCUR C39 _
		Reel of 250	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.

DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar, NanoFree are trademarks of Texas Instruments.

## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

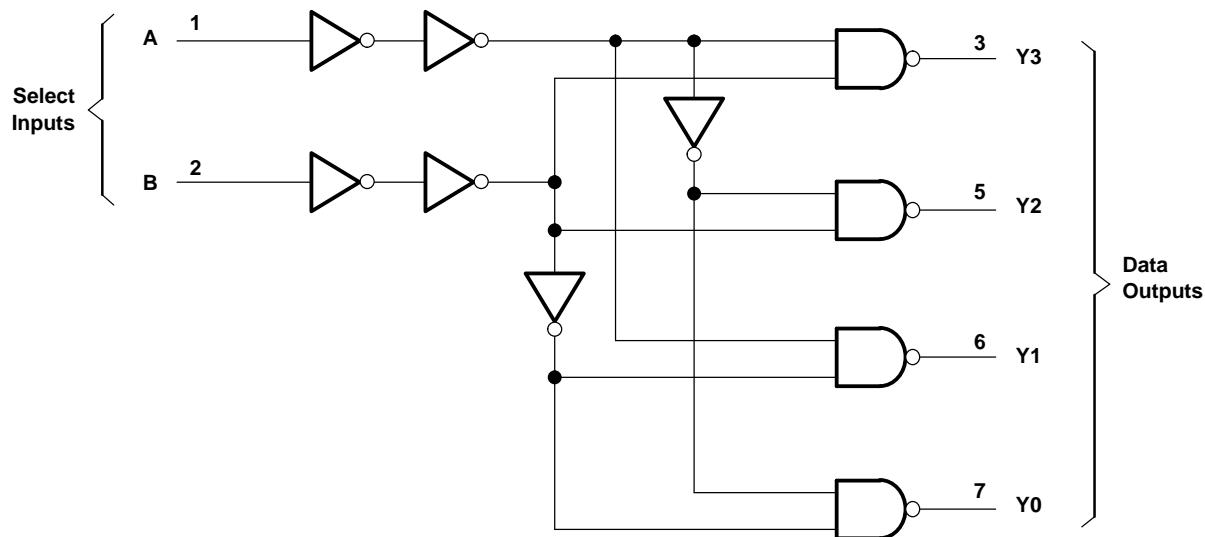
NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**FUNCTION TABLE**

SELECT INPUTS		OUTPUTS			
B	A	Y0	Y1	Y2	Y3
L	L	L	H	H	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	L

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	6.5	V
$V_I$	Input voltage range	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		$\pm 50$	mA
$I_{cc}$	Continuous current through $V_{CC}$ or GND		$\pm 100$	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DCT package	220	°C/W
		DCU package	227	
		YEP/YZP package	102	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**SN74LVC1G139**  
**2-TO-4 LINE DECODER**

SCES602B—AUGUST 2004—REVISED DECEMBER 2005

 **TEXAS  
INSTRUMENTS**  
[www.ti.com](http://www.ti.com)

**Recommended Operating Conditions<sup>(1)</sup>**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	2		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$		
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	0.8		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.3 \times V_{CC}$		
$V_I$	Input voltage		0	5.5	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 1.65\text{ V}$	-4		mA
		$V_{CC} = 2.3\text{ V}$	-8		
		$V_{CC} = 3\text{ V}$	-16		
		$V_{CC} = 4.5\text{ V}$	-24		
$I_{OL}$	Low-level output current	$V_{CC} = 1.65\text{ V}$	4		mA
		$V_{CC} = 2.3\text{ V}$	8		
		$V_{CC} = 3\text{ V}$	16		
		$V_{CC} = 4.5\text{ V}$	24		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}, 2.5\text{ V} \pm 0.2\text{ V}$	20		ns/V
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	15		
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	10		
$T_A$	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 $\mu$ A	1.65 V to 5.5 V	V <sub>CC</sub> - 0.1			V
	I <sub>OH</sub> = -4 mA	1.65 V		1.2		
	I <sub>OH</sub> = -8 mA	2.3 V		1.9		
	I <sub>OH</sub> = -16 mA			2.4		
	I <sub>OH</sub> = -24 mA	3 V		2.3		
	I <sub>OH</sub> = -32 mA	4.5 V		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 100 $\mu$ A	1.65 V to 5.5 V		0.1		V
	I <sub>OL</sub> = 4 mA	1.65 V		0.45		
	I <sub>OL</sub> = 8 mA	2.3 V		0.3		
	I <sub>OL</sub> = 16 mA			0.4		
	I <sub>OL</sub> = 24 mA	3 V		0.55		
	I <sub>OL</sub> = 32 mA	4.5 V		0.55		
I <sub>I</sub>	A or B inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		$\pm$ 1	$\mu$ A
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0		$\pm$ 5	$\mu$ A
I <sub>CC</sub>	V <sub>I</sub> = 5.5 V or GND,	I <sub>O</sub> = 0	1.65 V to 5.5 V		10	$\mu$ A
$\Delta I_{CC}$	One input at V <sub>CC</sub> - 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V		500	$\mu$ A
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V		4	pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> = 15 pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	2.7	15.3	1.5	7.5	0.9	4.9	0.8	3.6	ns

## Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> = 30 pF or 50 pF (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	3	16.7	1.6	8.2	1.2	5.9	1.1	4.2	ns

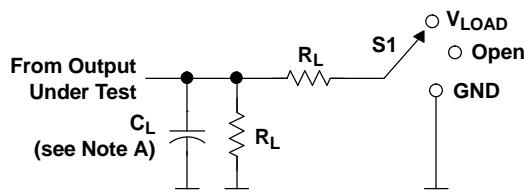
## Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V		V <sub>CC</sub> = 2.5 V		V <sub>CC</sub> = 3.3 V		V <sub>CC</sub> = 5 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
C <sub>pd</sub> <sup>(1)</sup>	Power dissipation capacitance	f = 10 MHz	31	34	36	39				pF

(1) Two outputs switching

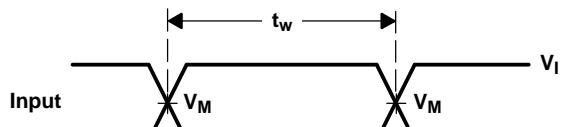
PARAMETER MEASUREMENT INFORMATION



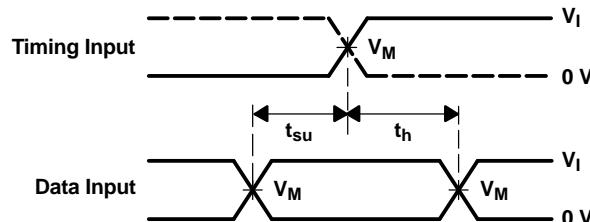
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT

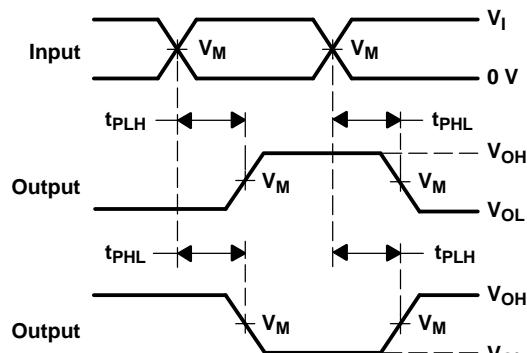
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_\Delta$
	$V_I$	$t_r/t_f$					
$1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	$1 \text{ M}\Omega$	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	$1 \text{ M}\Omega$	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	3 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	15 pF	$1 \text{ M}\Omega$	0.3 V
$5 \text{ V} \pm 0.5 \text{ V}$	$V_{CC}$	$\leq 2.5 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	$1 \text{ M}\Omega$	0.3 V



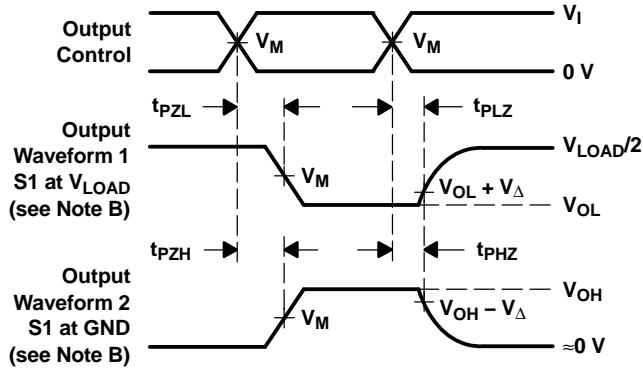
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



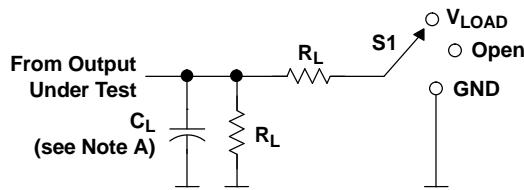
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

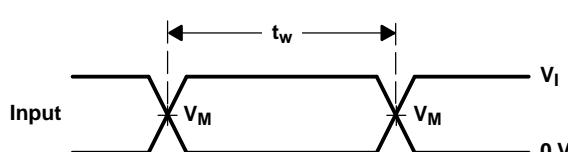
PARAMETER MEASUREMENT INFORMATION



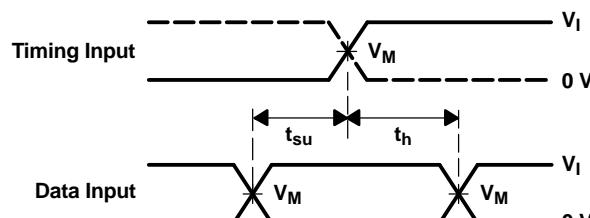
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT

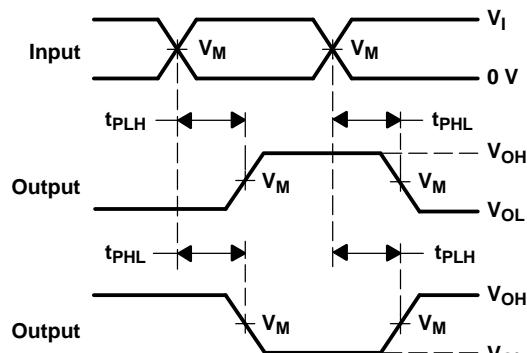
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_\Delta$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



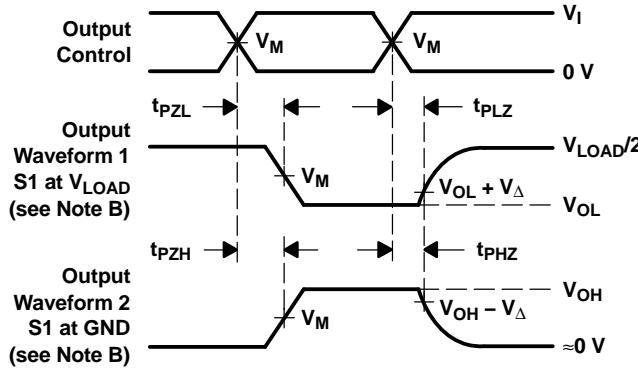
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74LVC1G139DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39Z	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
74LVC1G139DCTRG4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39Z	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
74LVC1G139DCTTE4	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39Z	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
74LVC1G139DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39R	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
74LVC1G139DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39R	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
74LVC1G139DCUTE4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39R	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
74LVC1G139DCUTG4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39R	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC1G139DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39Z	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC1G139DCTT	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39Z	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC1G139DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39R	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC1G139DCUT	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39R	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC1G139YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(DF7 ~ DFN)	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

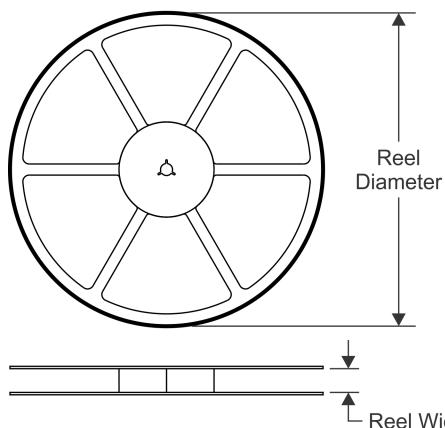
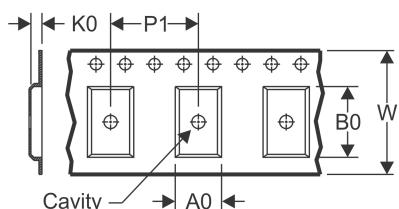
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

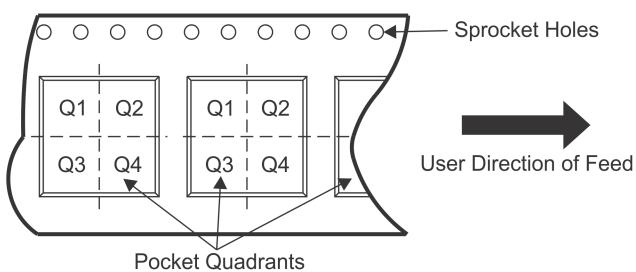
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G139DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G139YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

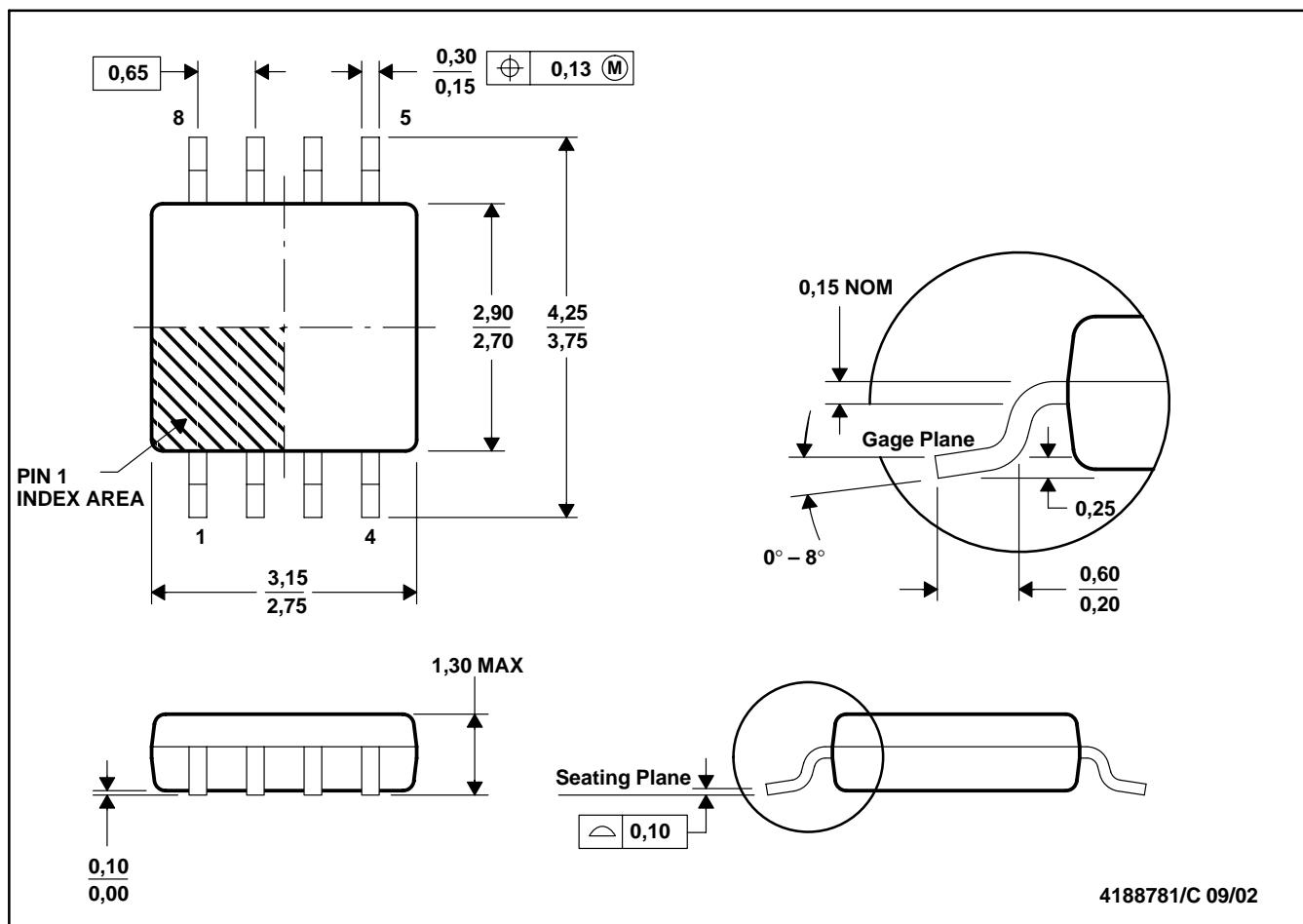
**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G139DCUR	US8	DCU	8	3000	202.0	201.0	28.0
SN74LVC1G139YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

## DCT (R-PDSO-G8)

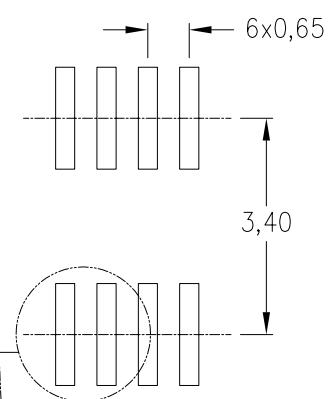
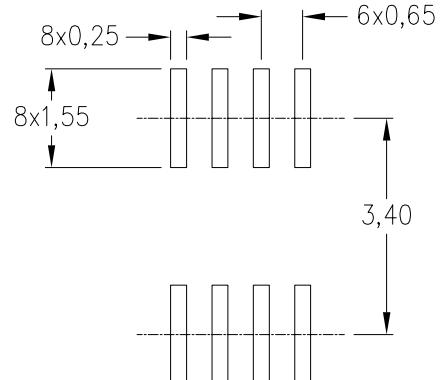
## PLASTIC SMALL-OUTLINE PACKAGE



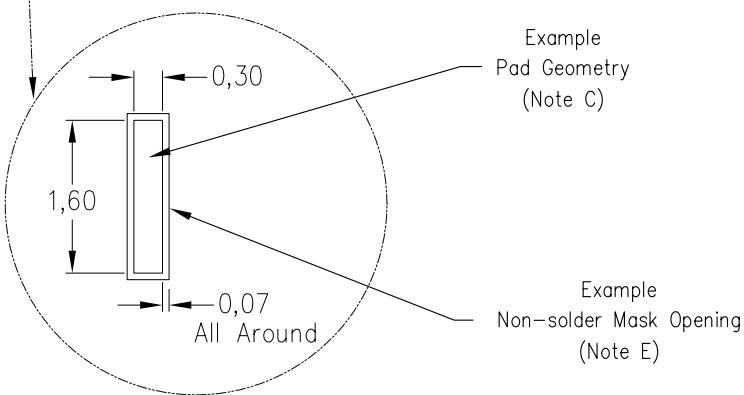
NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion  
 D. Falls within JEDEC MO-187 variation DA.

DCT (R-PDSO-G8)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C,E)Example Stencil Design  
(Note D)

Non Solder Mask Defined Pad

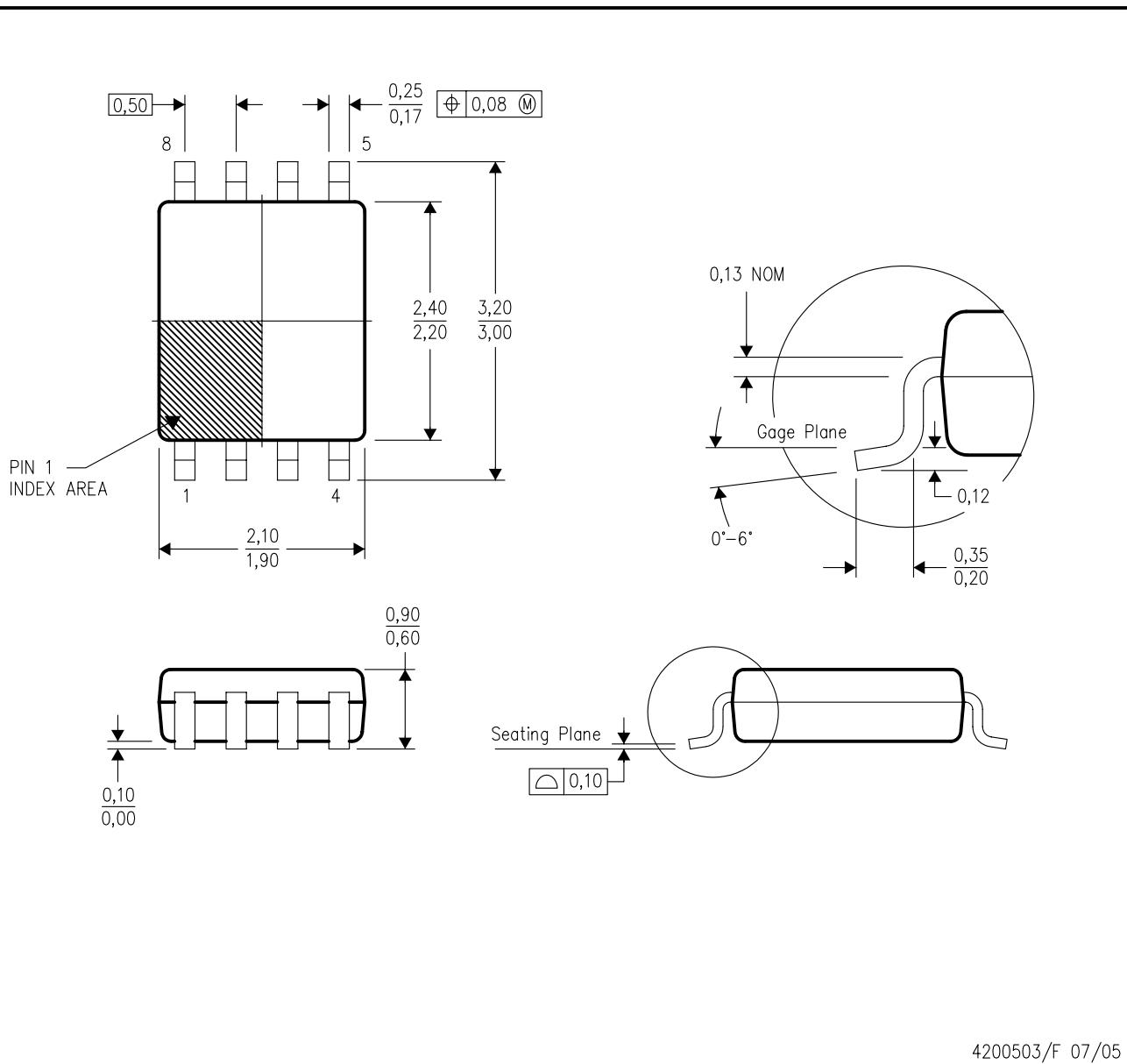
Example  
Pad Geometry  
(Note C)Example  
Non-solder Mask Opening  
(Note E)

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- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DCU (R-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)

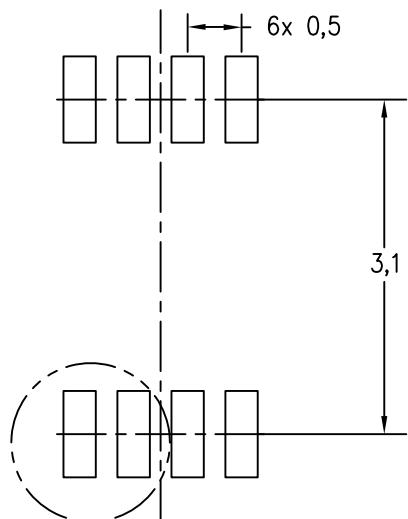
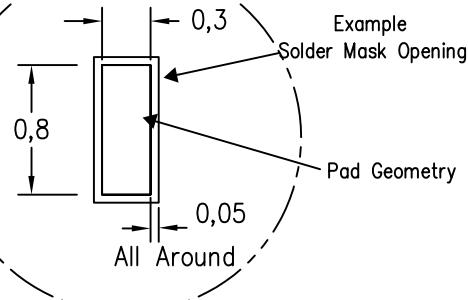
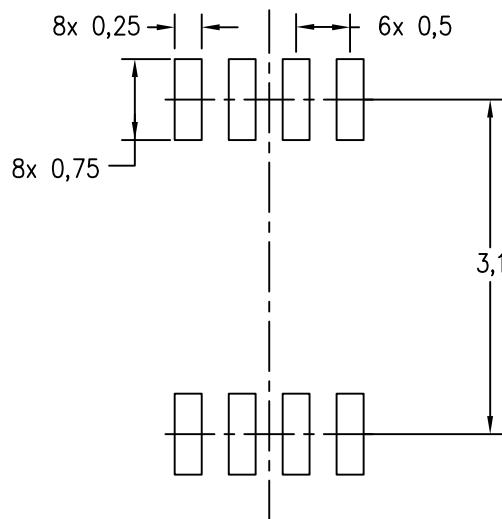


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)

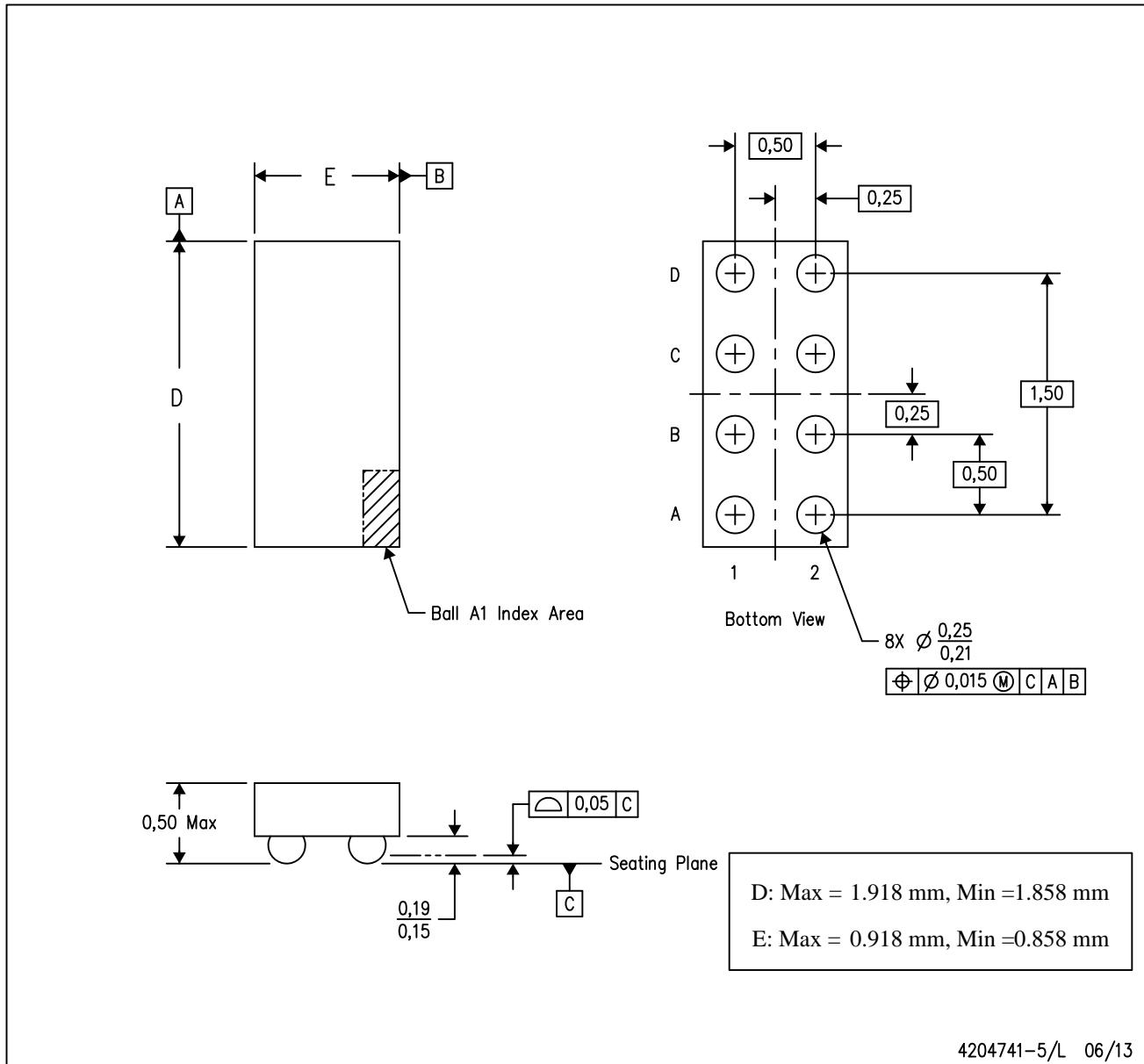
Example Board Layout  
(Note C,E)Example Stencil Design  
(Note D)

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- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



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OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
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