

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing and consumer applications.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- Consumer applications
- Desktop Voltage Regulator Module (VRM)
- Notebook Voltage Regulator Module (VRM)

1.4 Quick reference data

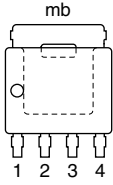
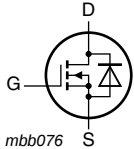
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	30	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 and 3	-	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	97	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}$; $I_D = 10\text{ A}$; $V_{DS} = 12\text{ V}$; see Figure 14 and 15	-	7.5	-	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5\text{ V}$; $I_D = 10\text{ A}$; $V_{DS} = 12\text{ V}$; see Figure 14	-	30	-	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$	-	1.55	2	mΩ

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

SOT669 (LPAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PH1930AL	LPAK	plastic single-ended surface-mounted package (LPAK); 4 leads	SOT669

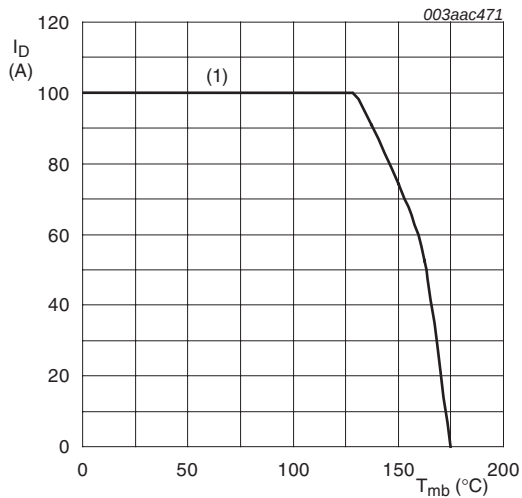
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

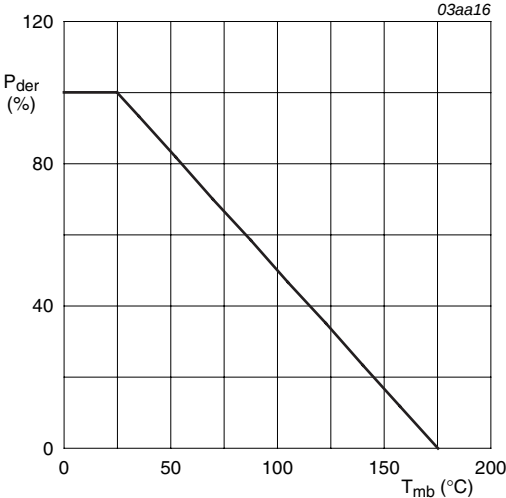
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1 ^[1]	-	100	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 and 3 ^[1]	-	100	A
I_{DM}	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$; see Figure 3	-	667	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	97	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$; ^[1]	-	100	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	667	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $I_D = 100\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped	-	151	mJ

[1] Continuous current is limited by package.



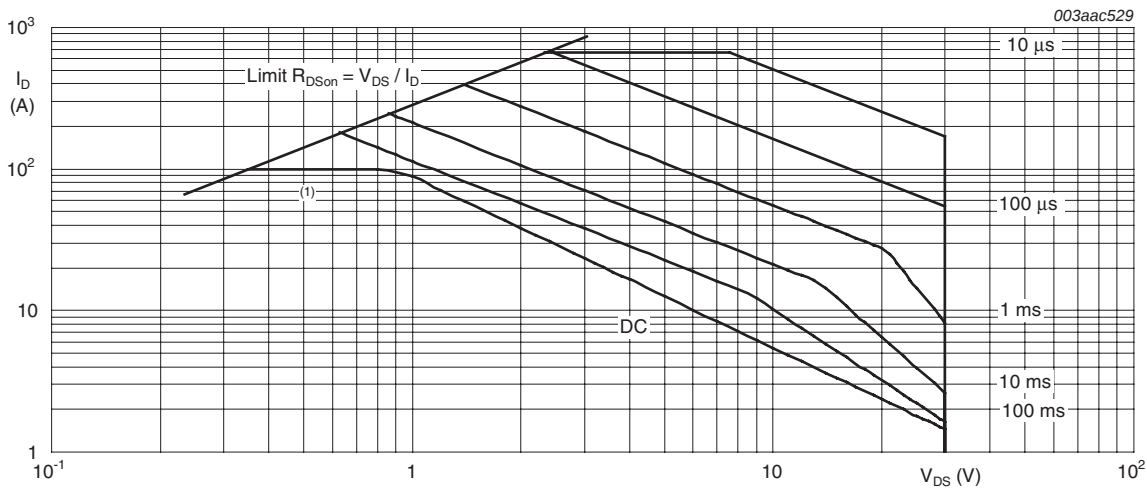
$V_{GS} \geq 10$ V; (1) Capped at 100 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse
(1) Capped at 100 A due to package.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.4	1.28	K/W

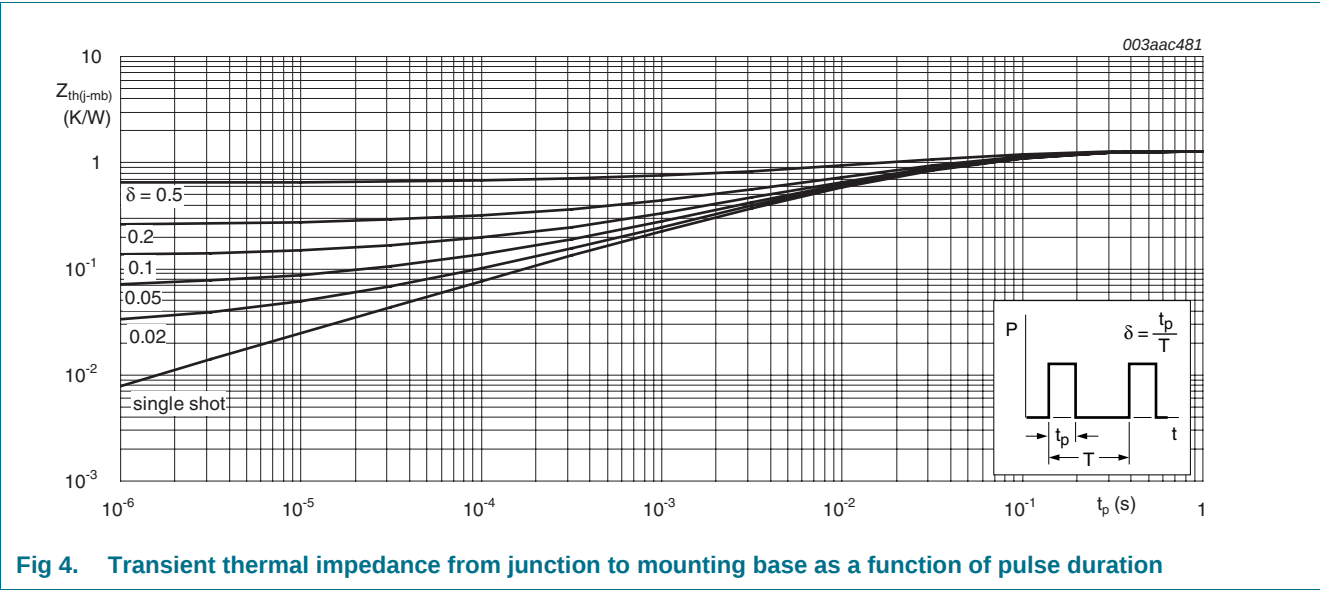


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

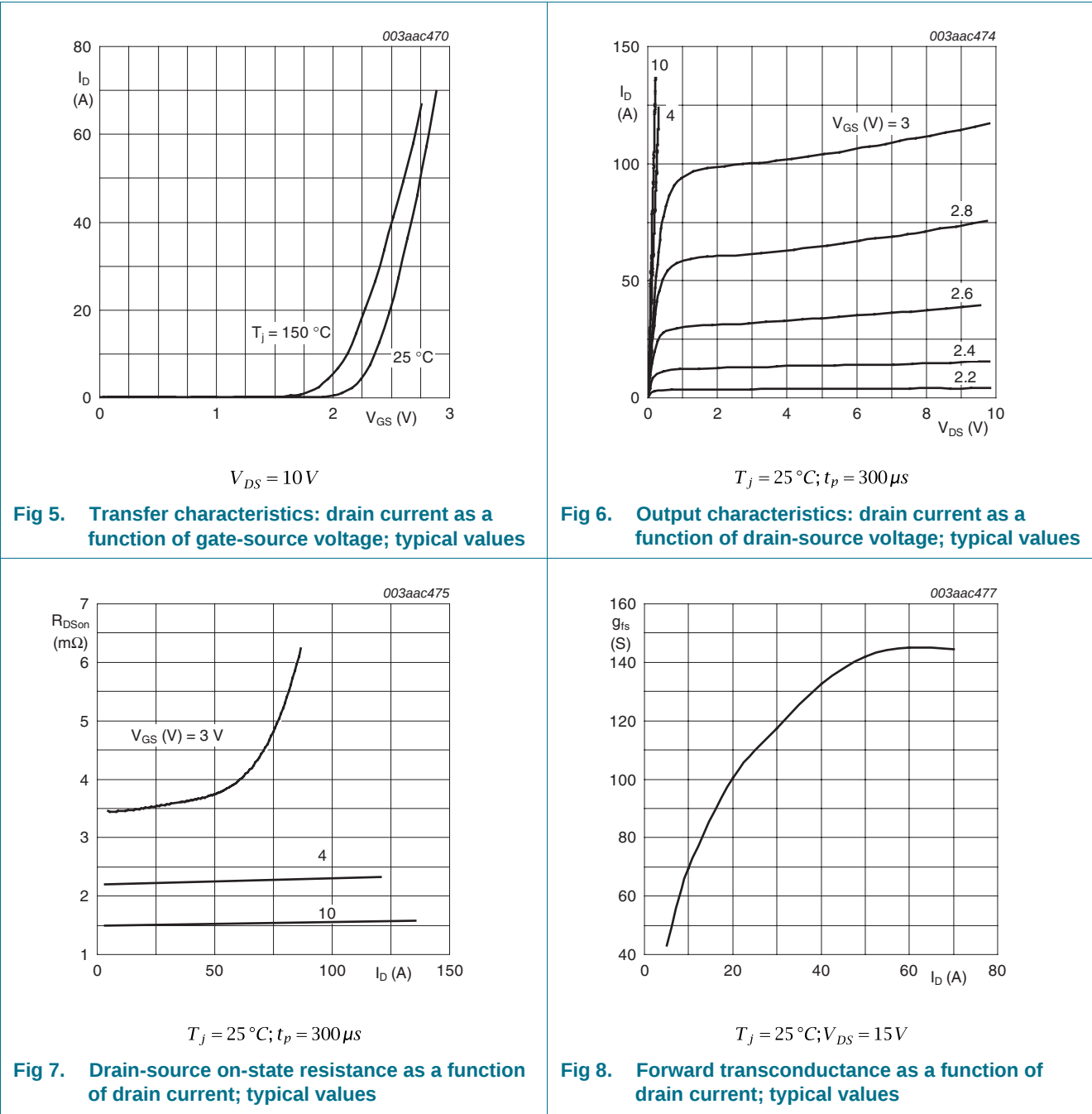
Table 6. Characteristics

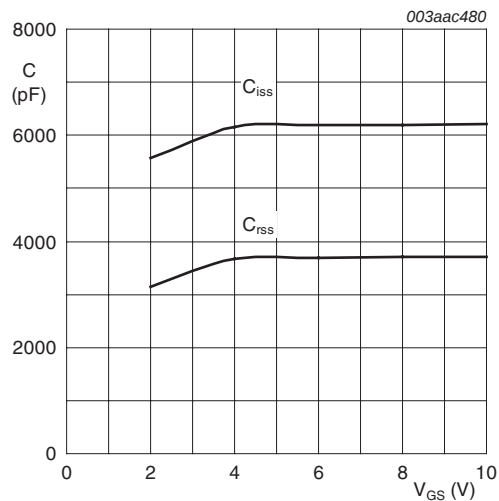
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	30	-	-	V
		$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = -55\ ^\circ\text{C}$	27	-	-	V
		$I_D = 20\ \text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$; $t_{av} = 100\ \text{ns}$	35	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ\text{C}$; see Figure 11 and 12	1.3	1.7	2.15	V
		$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = 150\ ^\circ\text{C}$; see Figure 12	0.65	-	-	V
		$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = -55\ ^\circ\text{C}$; see Figure 12	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 30\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 30\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 150\ ^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -16\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}$; $I_D = 15\ \text{A}$; $T_j = 25\ ^\circ\text{C}$	-	2.13	2.63	m Ω
		$V_{GS} = 10\ \text{V}$; $I_D = 15\ \text{A}$; $T_j = 150\ ^\circ\text{C}$; see Figure 13	-	-	3.3	m Ω
		$V_{GS} = 10\ \text{V}$; $I_D = 15\ \text{A}$; $T_j = 25\ ^\circ\text{C}$	-	1.55	2	m Ω
R_G	gate resistance	$f = 1\ \text{MHz}$	-	0.75	1.5	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 10\ \text{A}$; $V_{DS} = 12\ \text{V}$; $V_{GS} = 10\ \text{V}$; see Figure 14 and 15	-	64	-	nC
		$I_D = 0\ \text{A}$; $V_{DS} = 0\ \text{V}$; $V_{GS} = 10\ \text{V}$	-	59	-	nC
		$I_D = 10\ \text{A}$; $V_{DS} = 12\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; see Figure 14	-	30	-	nC
Q_{GS}	gate-source charge	$I_D = 10\ \text{A}$; $V_{DS} = 12\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; see Figure 14 and 15	-	9.8	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	6.6	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	3.2	-	nC
Q_{GD}	gate-drain charge		-	7.5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 12\ \text{V}$; see Figure 14 and 15	-	2.34	-	V
C_{iss}	input capacitance	$V_{DS} = 12\ \text{V}$; $V_{GS} = 0\ \text{V}$; $f = 1\ \text{MHz}$; $T_j = 25\ ^\circ\text{C}$; see Figure 16	-	3980	-	pF
C_{oss}	output capacitance		-	857	-	pF
C_{rss}	reverse transfer capacitance		-	347	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\ \text{V}$; $R_L = 0.5\ \Omega$; $V_{GS} = 4.5\ \text{V}$; $R_{G(ext)} = 4.7\ \Omega$	-	39	-	ns
t_r	rise time		-	65	-	ns
$t_{d(off)}$	turn-off delay time		-	63	-	ns
t_f	fall time		-	28	-	ns

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 17	-	0.78	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	43	-	ns
Q_r	recovered charge	$V_{DS} = 20\text{ V}$	-	49	-	nC

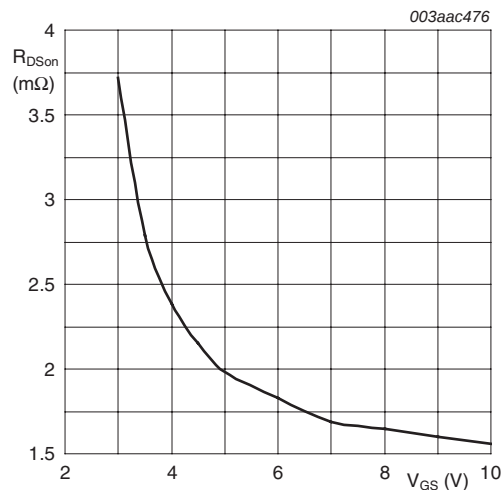
[1] Tested to JEDEC standards where applicable.





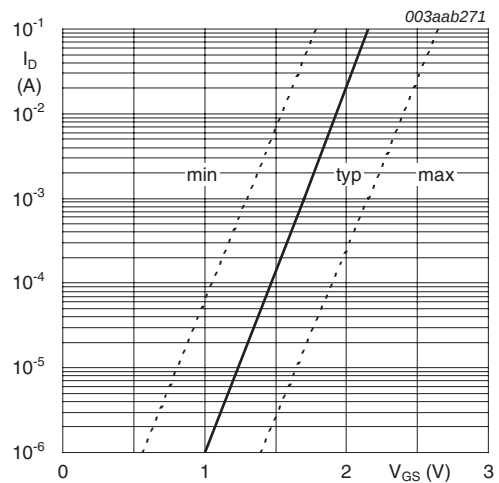
$V_{DS} = 0V; f = 1MHz$

Fig 9. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



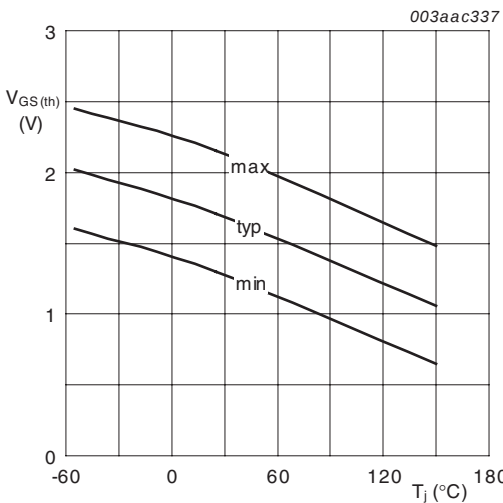
$T_j = 25^{\circ}C; I_D = 15A$

Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



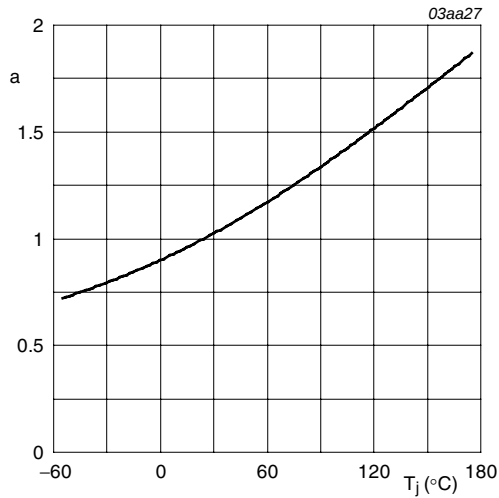
$T_j = 25^{\circ}C; V_{DS} = 5V$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1mA; V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

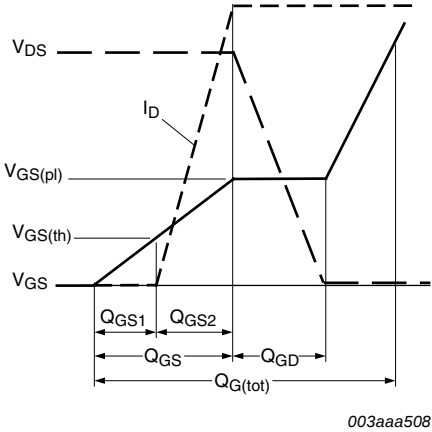
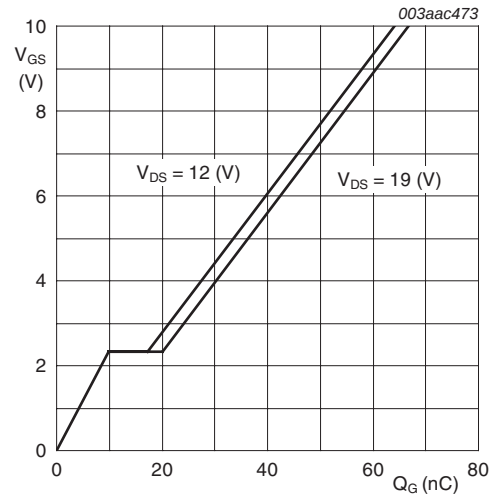
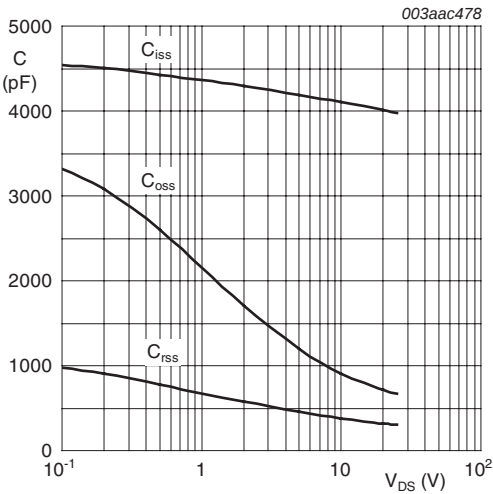


Fig 14. Gate charge waveform definitions



$$T_j = 25^{\circ}\text{C}; I_D = 10\text{ A}$$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

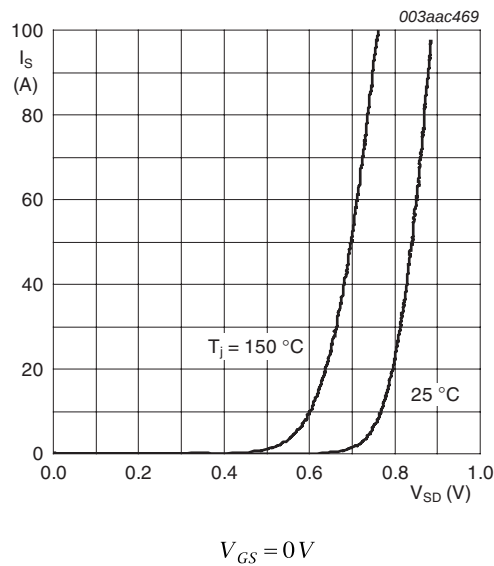


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

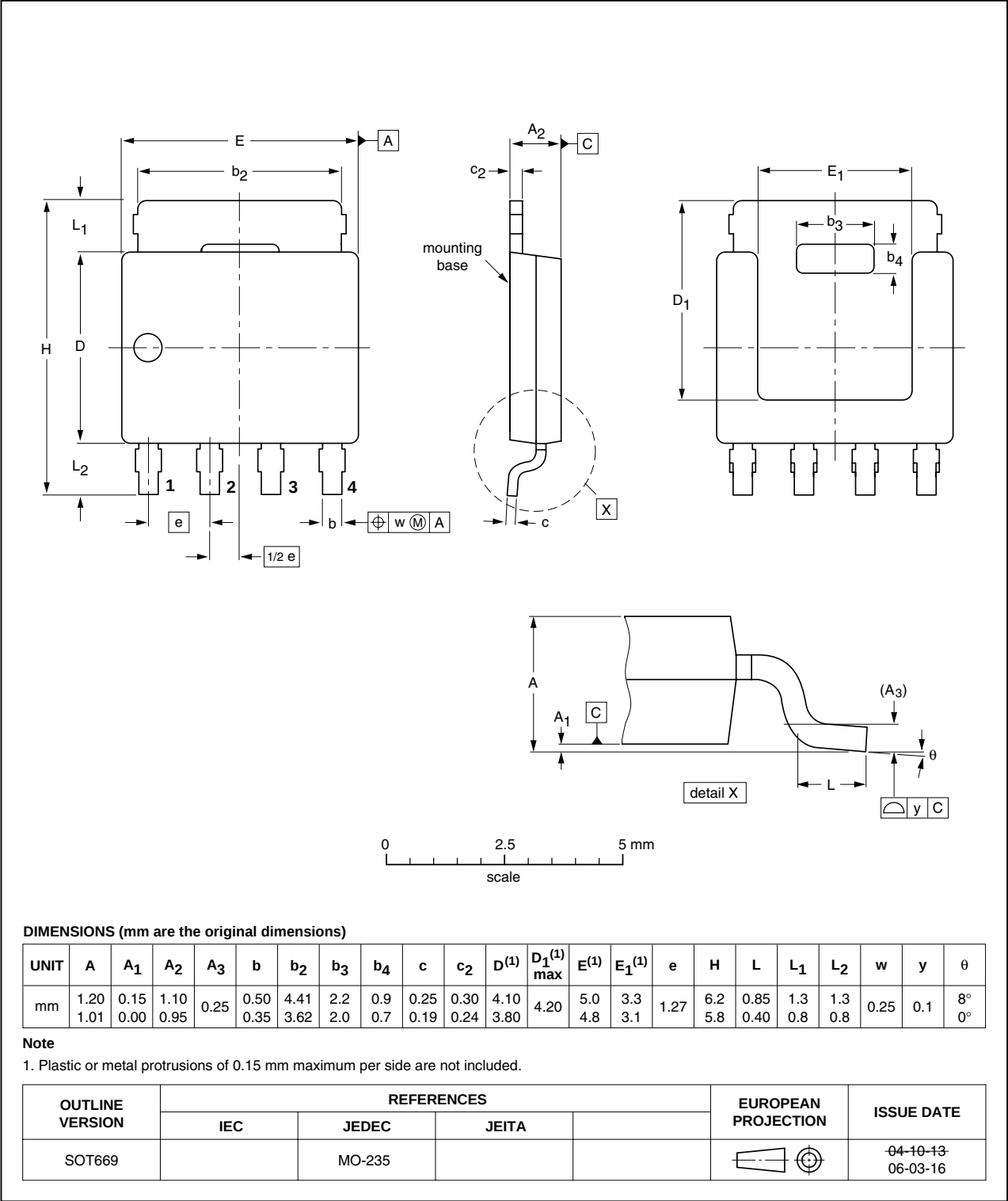


Fig 18. Package outline SOT669 (LPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH1930AL_3	20100112	Product data sheet	-	PH1930AL_2
Modifications:	• Various changes to content.			
PH1930AL_2	20090121	Product data sheet	-	PH1930AL_1
PH1930AL_1	20080909	Preliminary data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 12 January 2010

Document identifier: PH1930AL_3

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