LM5100A/B/C
LM5101A/B/C 3A, 2A and 1A High Voltage High-Side and Low-Side Gate Drivers

Check for Samples: LM5100A, LM5100B, LM5100C, LM5101A, LM5101B, LM5101C

FEATURES

- **Drives Both a High-side and Low-side N-Channel MOSFETs**
- **Independent High and Low Driver Logic Inputs**
- **Bootstrap Supply Voltage up to 118V DC**
- **Fast Propagation Times (25 ns Typical)**
- **Drives 1000 pF Load with 8 ns Rise and Fall Times**
- **Excellent Propagation Delay Matching (3 ns typical)**
- **Supply Rail Under-voltage Lockout**
- **Low Power Consumption**
- **Pin Compatible with HIP2100/HIP2101**

TYPICAL APPLICATIONS

- **Current Fed Push-pull Converters**
- **Half and Full Bridge Power Converters**
- **Synchronous Buck Converters**
- **Two Switch Forward Power Converters**
- **Forward with Active Clamp Converters**

DESCRIPTION

The LM5100A/B/C and LM5101A/B/C High Voltage Gate Drivers are designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half-bridge configuration. The floating high-side driver is capable of operating with supply voltages up to 100V. The “A” versions provide a full 3A of gate drive while the “B” and “C” versions provide 2A and 1A respectively. The outputs are independently controlled with CMOS input thresholds (LM5100A/B/C) or TTL input thresholds (LM5101A/B/C). An integrated high voltage diode is provided to charge the high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high-side gate driver. Under-voltage lockout is provided on both the low-side and the high-side power rails. These devices are available in the standard SOIC-8 pin, SO PowerPad-8 pin and the WSON-10 pin packages. The LM5100C and LM5101C are also available in MSOP-PowerPad-8 package. The LM5101A is also available in WSON-8 pin package.

Package

- SOIC-8
- SO PowerPad-8
- WSON-8 (4 mm x 4 mm)
- WSON-10 (4 mm x 4 mm)
- MSOP-PowerPad-8

Simplified Block Diagram

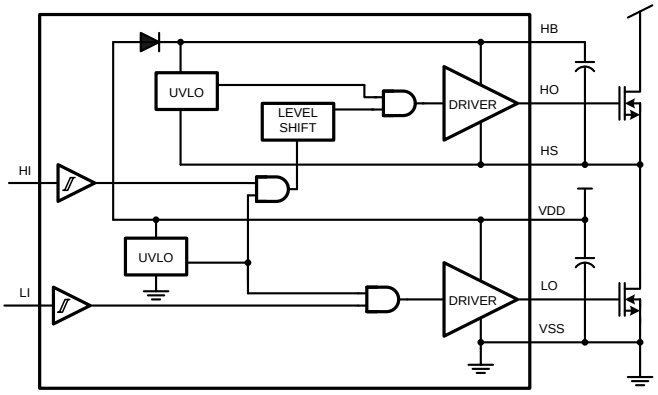
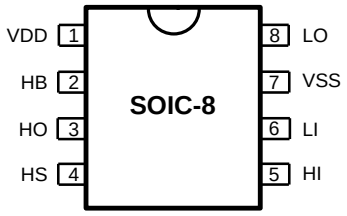
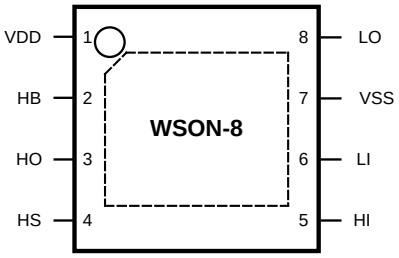


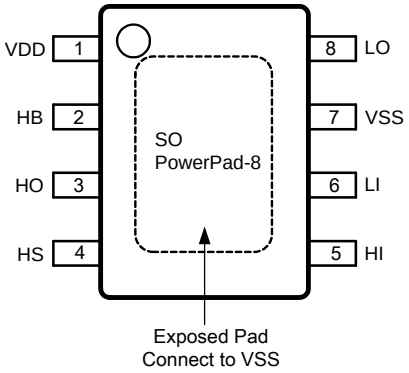
Table 1. Input/Output Options

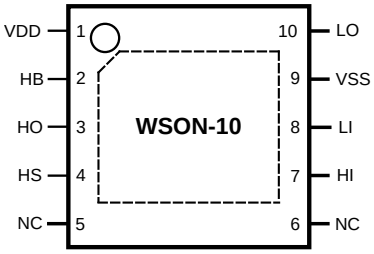
Part Number	Input Thresholds	Peak Output Current
LM5100A	CMOS	3A
LM5101A	TTL	3A
LM5100B	CMOS	2A
LM5101B	TTL	2A
LM5100C	CMOS	1A
LM5101C	TTL	1A

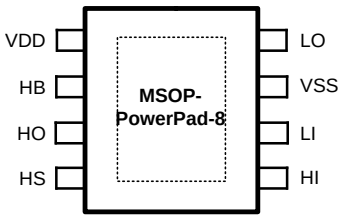
Connection Diagrams











PIN DESCRIPTIONS (1)

Pin #					Name	Description	Application Information
SOIC-8	SO PowerPad-8	WSON-8 (1)	WSON-10 (1)	MSOP-PowerPad-8 (1)			
1	1	1	1	1	VDD	Positive gate drive supply	Locally decouple to VSS using low ESR/ESL capacitor located as close to the IC as possible.
2	2	2	2	2	HB	High-side gate driver bootstrap rail	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The bootstrap capacitor should be placed as close to the IC as possible.
3	3	3	3	3	HO	High-side gate driver output	Connect to the gate of high-side MOSFET with a short, low inductance path.

(1) **Note: For WSON-8, WSON-10 and MSOP-PowerPad-8 package, it is recommended that the exposed pad on the bottom of the package is soldered to ground plane on the PC board, and that ground plane should extend out from beneath the IC to help dissipate heat. For WSON-10 package, pins 5 and 6 have no connection.**

PIN DESCRIPTIONS(1) (continued)

Pin #					Name	Description	Application Information
SOIC-8	SO Power Pad-8	WSON-8(1)	WSON-10(1)	MSOP-PowerPad-8(1)			
4	4	4	4	4	HS	High-side MOSFET source connection	Connect to the bootstrap capacitor negative terminal and the source of the high-side MOSFET.
5	5	5	7	5	HI	High-side driver control input	The LM5100A/B/C inputs have CMOS type thresholds. The LM5101A/B/C inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
6	6	6	8	6	LI	Low-side driver control input	The LM5100A/B/C inputs have CMOS type thresholds. The LM5101A/B/C inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
7	7	7	9	7	VSS	Ground return	All signals are referenced to this ground.
8	8	8	10	8	LO	Low-side gate driver output	Connect to the gate of the low-side MOSFET with a short, low inductance path.
	EP	EP	EP	EP	EP (WSON and SO PowerPad and MSOP-PowerPad packages)		Solder to the ground plane under the IC to aid in heat dissipation.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

VDD to VSS	−0.3V to +18V
HB to HS	−0.3V to +18V
LI or HI Input	−0.3V to V_{DD} +0.3V
LO Output	−0.3V to V_{DD} +0.3V
HO Output	V_{HS} −0.3V to V_{HB} +0.3V
HS to VSS (3)	−5V to +100V
HB to VSS	118V
Junction Temperature	+150°C
Storage Temperature Range	−55°C to +150°C
ESD Rating HBM (4)	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics Electrical Characteristics tables.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS node will generally not exceed -1V. However, in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur, the HS voltage must never be more negative than VDD-15V. For example if VDD = 10V, the negative transients at HS must not exceed -5V.

(4) The Human Body Model (HBM) is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. 2 kV for all pins except Pin 2, Pin 3 and Pin 4 which are rated at 1000V for HBM. Machine Model (MM) ratings are : 100V(MM) for Options B and C; 50V(MM) for Option A.

Recommended Operating Conditions

VDD	+9V to +14V
HS	−1V to 100V
HB	V_{HS} +8V to V_{HS} +14V
HS Slew Rate	< 50 V/ns
Junction Temperature	−40°C to +125°C

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO (1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SUPPLY CURRENTS						
I_{DD}	VDD Quiescent Current, LM5100A/B/C	LI = HI = 0V		0.1	**0.2**	mA
	VDD Quiescent Current, LM5101A/B/C	LI = HI = 0V		0.25	**0.4**	
I_{DDO}	VDD Operating Current	f = 500 kHz		2.0	**3**	mA
I_{HB}	Total HB Quiescent Current	LI = HI = 0V		0.06	**0.2**	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.6	**3**	mA
I_{HBS}	HB to VSS Current, Quiescent	HS = HB = 100V		0.1	**10**	µA
I_{HBSO}	HB to VSS Current, Operating	f = 500 kHz		0.4		mA
INPUT PINS						
V_{IL}	Input Voltage Threshold LM5100A/B/C	Rising Edge	**4.5**	5.4	**6.3**	V
V_{IL}	Input Voltage Threshold LM5101A/B/C	Rising Edge	**1.3**	1.8	**2.3**	V
V_{IHYS}	Input Voltage Hysteresis LM5100A/B/C			500		mV
V_{IHYS}	Input Voltage Hysteresis LM5101A/B/C			50		mV
R_I	Input Pulldown Resistance		**100**	200	**400**	kΩ
UNDER VOLTAGE PROTECTION						
V_{DDR}	VDD Rising Threshold		**6.0**	6.9	**7.4**	V
V_{DDH}	VDD Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold		**5.7**	6.6	**7.1**	V
V_{HBH}	HB Threshold Hysteresis			0.4		V
BOOT STRAP DIODE						
V_{DL}	Low-Current Forward Voltage	I_{VDD-HB} = 100 µA		0.52	**0.85**	V
V_{DH}	High-Current Forward Voltage	I_{VDD-HB} = 100 mA		0.8	**1**	V
R_D	Dynamic Resistance LM5100A/B/C, LM5101A/B/C	I_{VDD-HB} = 100 mA		1.0	**1.65**	Ω
LO & HO GATE DRIVER						
V_{OL}	Low-Level Output Voltage LM5100A/LM5101A	I_{HO} = I_{LO} = 100 mA		0.12	**0.25**	V
	Low-Level Output Voltage LM5100B/LM5101B			0.16	**0.4**	
	Low-Level Output Voltage LM5100C/LM5101C			0.28	**0.65**	
V_{OH}	High-Level Output Voltage LM5100A/LM5101A	I_{HO} = I_{LO} = 100 mA V_{OH} = VDD– LO or V_{OH} = HB - HO		0.24	**0.45**	V
	High-Level Output Voltage LM5100B/LM5101B			0.28	**0.60**	
	High-Level Output Voltage LM5100C/LM5101C			0.60	**1.10**	
I_{OHL}	Peak Pullup Current LM5100A/LM5101A	HO, LO = 0V		3		A
	Peak Pullup Current LM5100B/LM5101B			2		
	Peak Pullup Current LM5100C/LM5101C			1		
I_{OLL}	Peak Pulldown Current LM5100A/LM5101A	HO, LO = 12V		3		A
	Peak Pulldown Current LM5100B/LM5101B			2		
	Peak Pulldown Current LM5100C/LM5101C			1		

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO (1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
THERMAL RESISTANCE						
θ_{JA} (2)	Junction to Ambient	SOIC-8		170		°C/W
		WSON-8 (3)		40		
		WSON-10 (3)		40		
		SO PowerPad-8		40		
		MSOP-PowerPad-8 (3)		80		

(2) The θ_{JA} is not a given constant for the package and depends on the printed circuit board design and the operating environment.
(3) 4 layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187.

Switching Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO (1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LPHL}	LO Turn-Off Propagation Delay LM5100A/B/C	LI Falling to LO Falling		20	**45**	ns
	LO Turn-Off Propagation Delay LM5101A/B/C			22	**56**	
t_{LPLH}	LO Turn-On Propagation Delay LM5100A/B/C	LI Rising to LO Rising		20	**45**	ns
	LO Turn-On Propagation Delay LM5101A/B/C			26	**56**	
t_{HPHL}	HO Turn-Off Propagation Delay LM5100A/B/C	HI Falling to HO Falling		20	**45**	ns
	HO Turn-Off Propagation Delay LM5101A/B/C			22	**56**	
t_{HPLH}	LO Turn-On Propagation Delay LM5100A/B/C	HI Rising to HO Rising		20	**45**	ns
	LO Turn-On Propagation Delay LM5101A/B/C			26	**56**	
t_{MON}	Delay Matching: LO on & HO off LM5100A/B/C			1	**10**	ns
	Delay Matching: LO on & HO off LM5101A/B/C			4	**10**	
t_{MOFF}	Delay Matching: LO off & HO on LM5100A/B/C			1	**10**	ns
	Delay Matching: LO on & HO off LM5101A/B/C			4	**10**	
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000 pF		8		ns
t_R	Output Rise Time (3V to 9V) LM5100A/LM5101A	C_L = 0.1 µF		430		ns
	Output Rise Time (3V to 9V) LM5100B/LM5101B			570		
	Output Rise Time (3V to 9V) LM5100C/LM5101C			990		
t_F	Output Fall Time (3V to 9V) LM5100A/LM5101A	C_L = 0.1 µF		260		ns
	Output Fall Time (3V to 9V) LM5100B/LM5101B			430		
	Output Fall Time (3V to 9V) LM5100C/LM5101C			715		
t_{PW}	Minimum Input Pulse Width that Changes the Output			50		ns
t_{BS}	Bootstrap Diode Reverse Recovery Time	I_F = 100 mA, I_R = 100 mA		37		ns

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

Typical Performance Characteristics

Peak Sourcing Current vs VDD

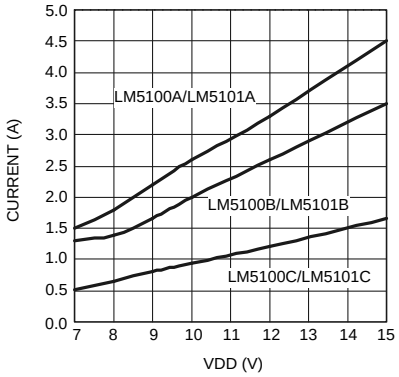


Figure 1.

Peak Sinking Current vs VDD

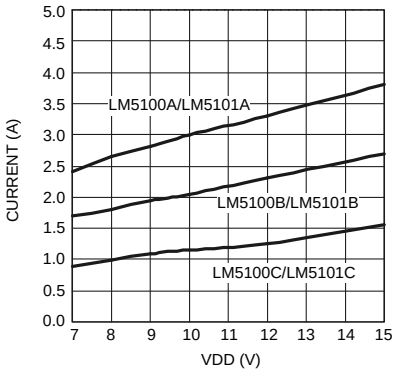


Figure 2.

Sink Current vs Output Voltage

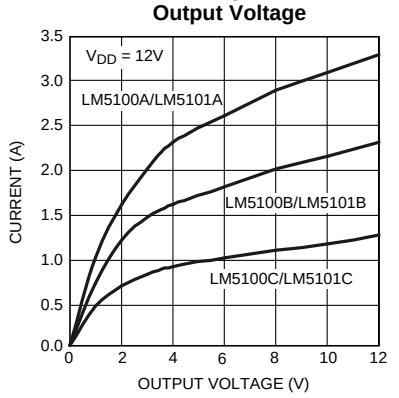


Figure 3.

Source Current vs Output Voltage

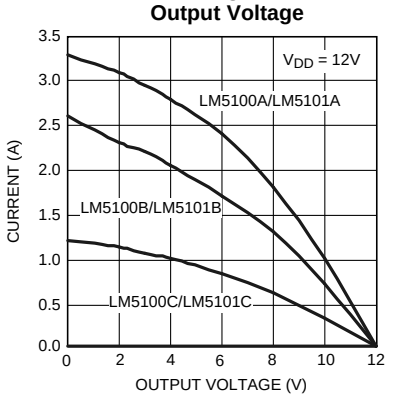


Figure 4.

LM5100A/B/C I_{DD} vs Frequency

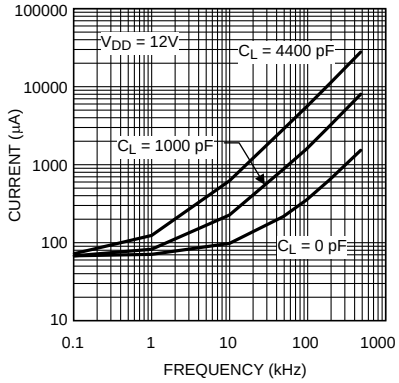


Figure 5.

LM5101A/B/C I_{DD} vs Frequency

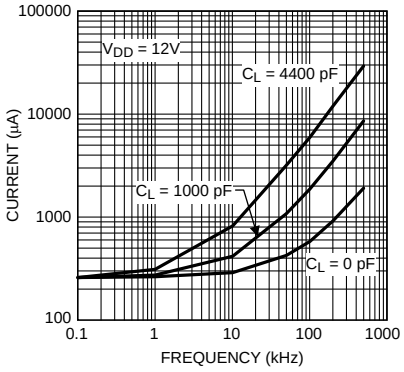


Figure 6.

Typical Performance Characteristics (continued)

Operating Current vs Temperature

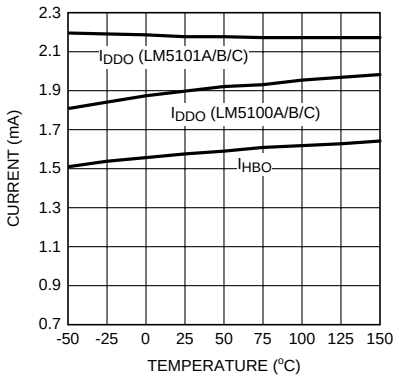


Figure 7.

I_{HB} vs Frequency

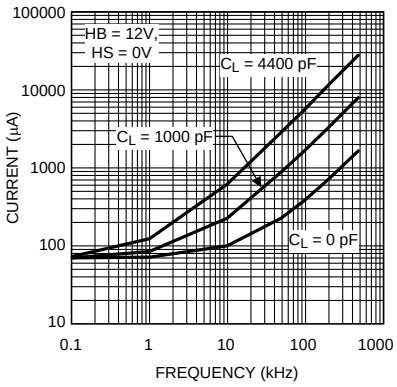


Figure 8.

Quiescent Current vs Supply Voltage

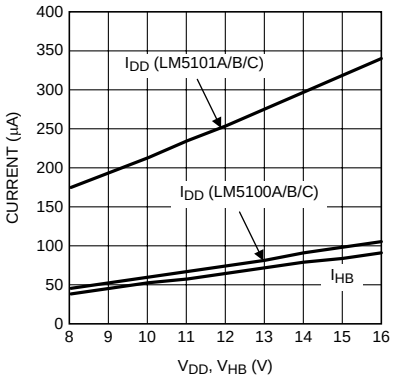


Figure 9.

Quiescent Current vs Temperature

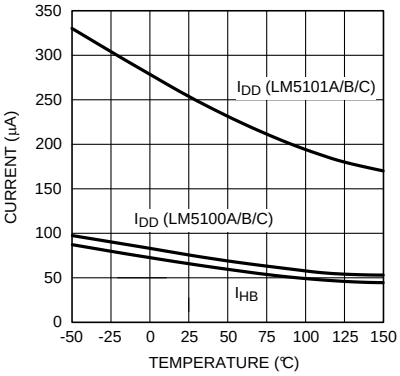


Figure 10.

Undervoltage Rising Thresholds vs Temperature

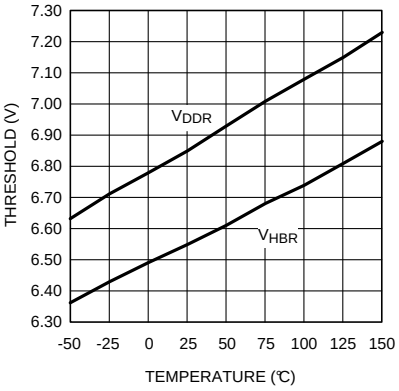


Figure 11.

Undervoltage Threshold Hysteresis vs Temperature

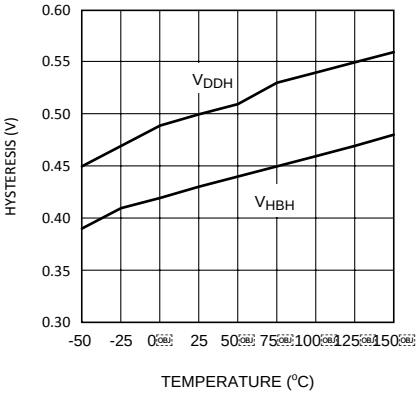


Figure 12.

Typical Performance Characteristics (continued)

Bootstrap Diode Forward Voltage

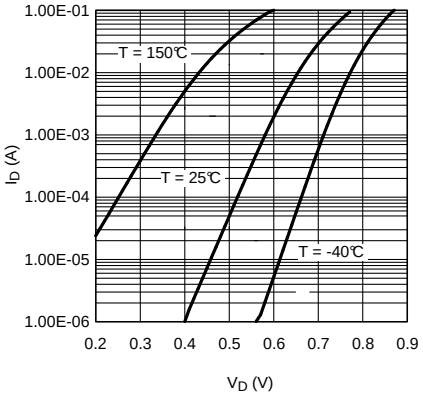


Figure 13.

LM5100A/B/C Input Threshold vs Temperature

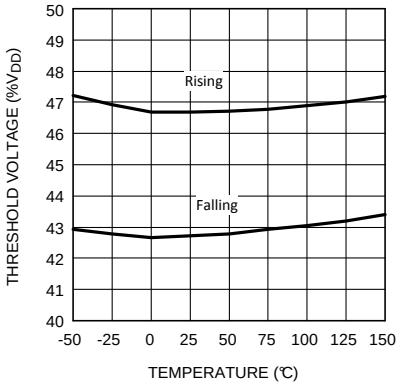


Figure 14.

LM5101A/B/C Input Threshold vs Temperature

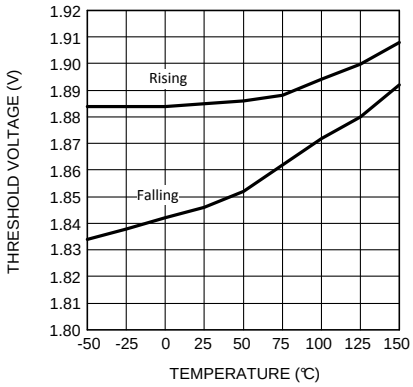


Figure 15.

LM5100A/B/C Input Threshold vs VDD

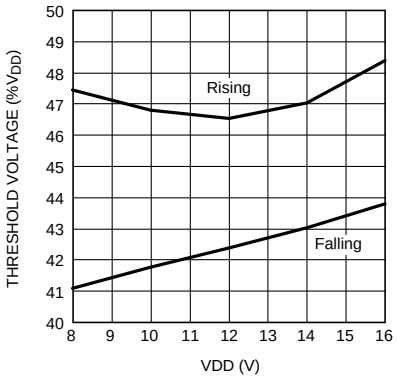


Figure 16.

LM5101A/B/C Input Threshold vs VDD

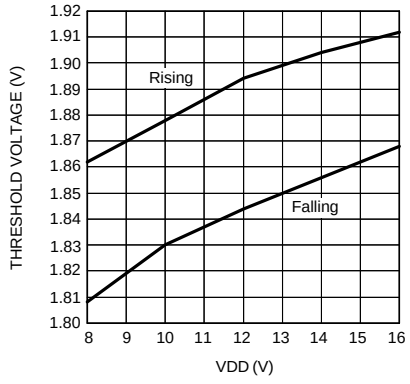


Figure 17.

LM5100A/B/C Propagation Delay vs Temperature

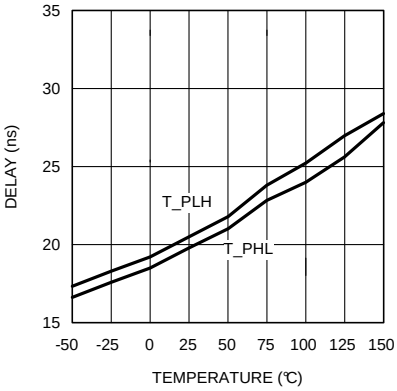


Figure 18.

Typical Performance Characteristics (continued)

LM5101A/B/C Propagation Delay vs Temperature

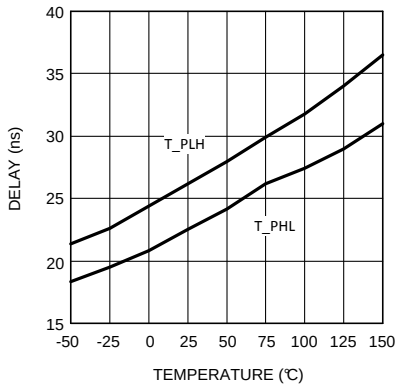


Figure 19.

LO & HO Gate Drive - High Level Output Voltage vs Temperature

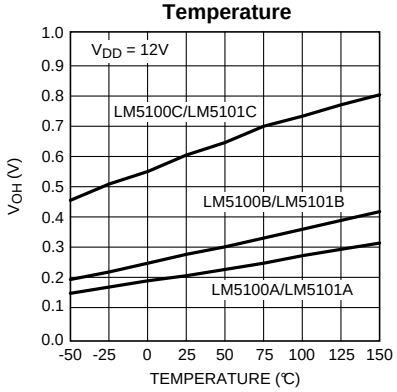


Figure 20.

LO & HO Gate Drive - Low Level Output Voltage vs Temperature

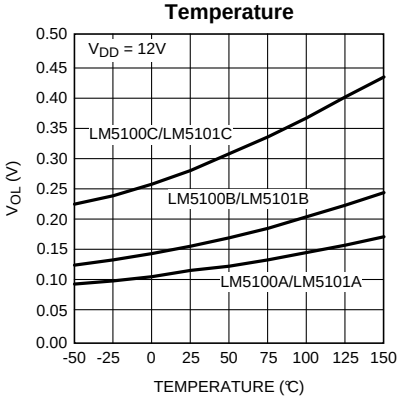


Figure 21.

LO & HO Gate Drive - Output High Voltage vs VDD

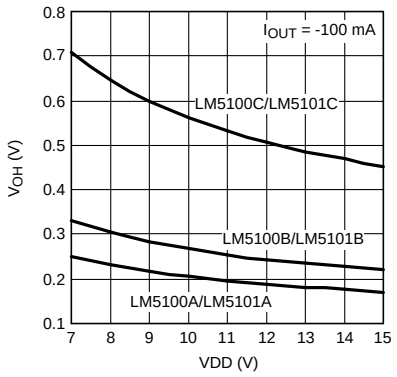


Figure 22.

LO & HO Gate Drive - Output Low Voltage vs VDD

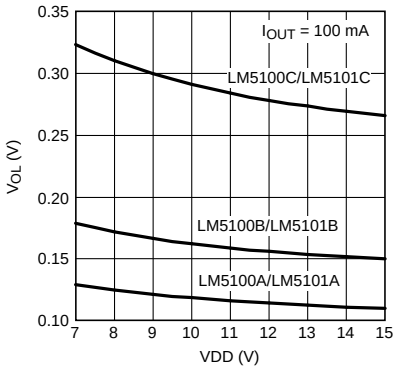


Figure 23.

TIMING DIAGRAM

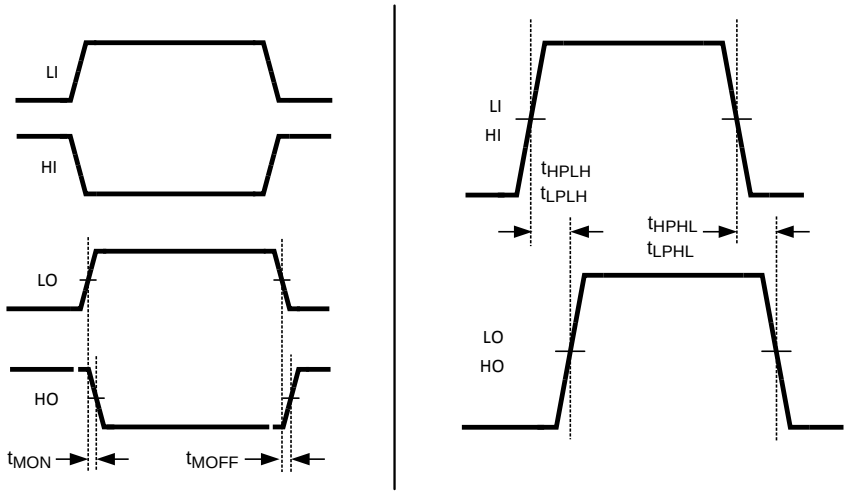


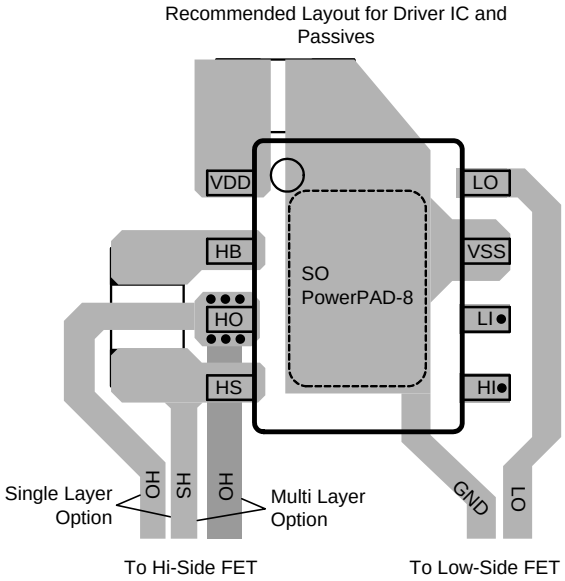
Figure 24.

Layout Considerations

The optimum performance of high and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. Low ESR / ESL capacitors must be connected close to the IC, between VDD and VSS pins and between the HB and HS pins to support the high peak currents being drawn from VDD during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (VSS).
3. In order to avoid large negative transients on the switch node (HS pin), the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding Considerations:
   - a) The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
   - b) The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

A recommended layout pattern for the driver is shown in the following figure. If possible a single layer placement is preferred.



Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (VDD) and can be roughly calculated as:

$$P_{DGATES} = 2 \bullet f \bullet C_L \bullet V_{DD}^2 \quad (1)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equation.Equation 1 This plot can be used to approximate the power losses due to the gate drivers.

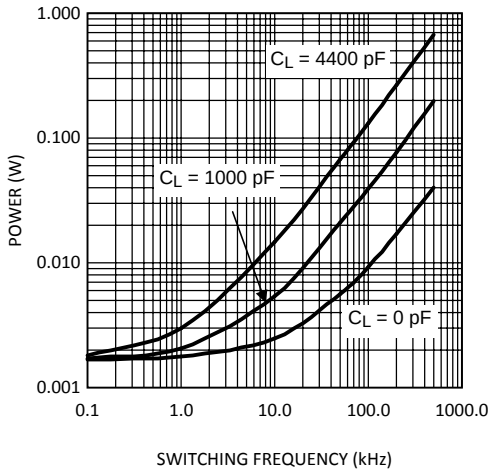


Figure 25. Gate Driver Power Dissipation (LO + HO)
V_{DD} = 12V, Neglecting Diode Losses

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more energy to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation.

The total IC power dissipation can be estimated from the previous plots by summing the gate drive losses with the bootstrap diode losses for the intended application.

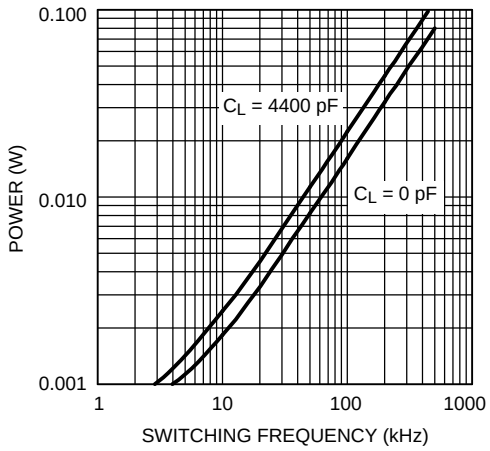


Figure 26. Diode Power Dissipation V_{IN} = 50V

REVISION HISTORY

Changes from Revision O (March 2013) to Revision P	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5100AM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	L5100 AM	Samples
LM5100AMR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-3-260C-168 HR		L5100 AMR	Samples
LM5100AMRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR		L5100 AMR	Samples
LM5100AMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	L5100 AM	Samples
LM5100ASD	NRND	WSON	DPR	10	1000	TBD	Call TI	Call TI	-40 to 125	5100ASD	
LM5100ASD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5100ASD	Samples
LM5100ASDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5100ASD	Samples
LM5100BMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	L5100 BMA	Samples
LM5100BMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	L5100 BMA	Samples
LM5100BSD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5100BSD	Samples
LM5100BSDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5100BSD	Samples
LM5100CMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	L5100 CMA	Samples
LM5100CMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5100 CMA	Samples
LM5100CMY/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SXCB	Samples
LM5100CMYE/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SXCB	Samples
LM5100CMYX/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SXCB	Samples
LM5100CSD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5100CSD	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5100CSDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5100CSD	Samples
LM5101AM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	L5101 AM	
LM5101AM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	L5101 AM	Samples
LM5101AMR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-3-260C-168 HR		L5101 AMR	Samples
LM5101AMRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-3-260C-168 HR		L5101 AMR	Samples
LM5101AMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	L5101 AM	Samples
LM5101ASD	NRND	WSON	DPR	10	1000	TBD	Call TI	Call TI	-40 to 125	5101ASD	
LM5101ASD-1/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM		5101A-1	Samples
LM5101ASD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	5101ASD	Samples
LM5101ASDX	NRND	WSON	DPR	10	4500	TBD	Call TI	Call TI	-40 to 125	5101ASD	
LM5101ASDX-1/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		5101A-1	Samples
LM5101ASDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	5101ASD	Samples
LM5101BMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5101 BMA	Samples
LM5101BMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	L5101 BMA	Samples
LM5101BSD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	(5101ASD ~ 5101BSD)	Samples
LM5101BSDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5101BSD	Samples
LM5101CMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 125	L5101 CMA	Samples
LM5101CMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5101 CMA	Samples
LM5101CMY/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SXDB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5101CMYE/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SXDB	Samples
LM5101CMYX/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SXDB	Samples
LM5101CSD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	5101CSD	Samples
LM5101CSDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5101CSD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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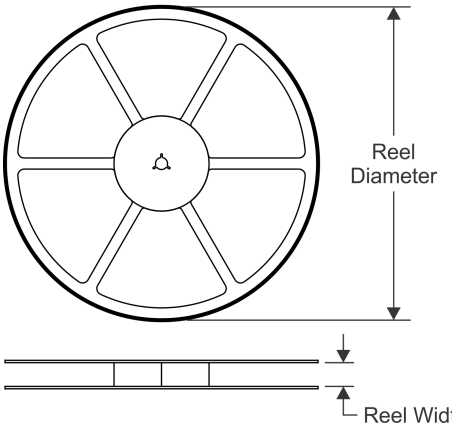
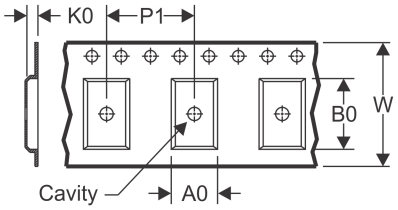
TAPE AND REEL INFORMATION

REEL DIMENSIONS

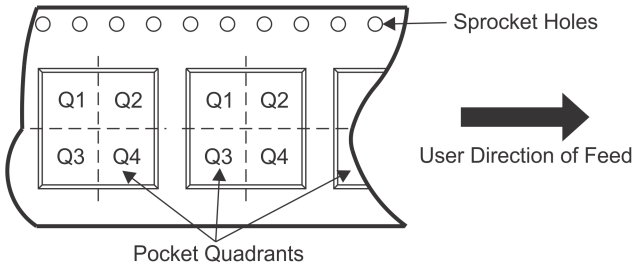


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

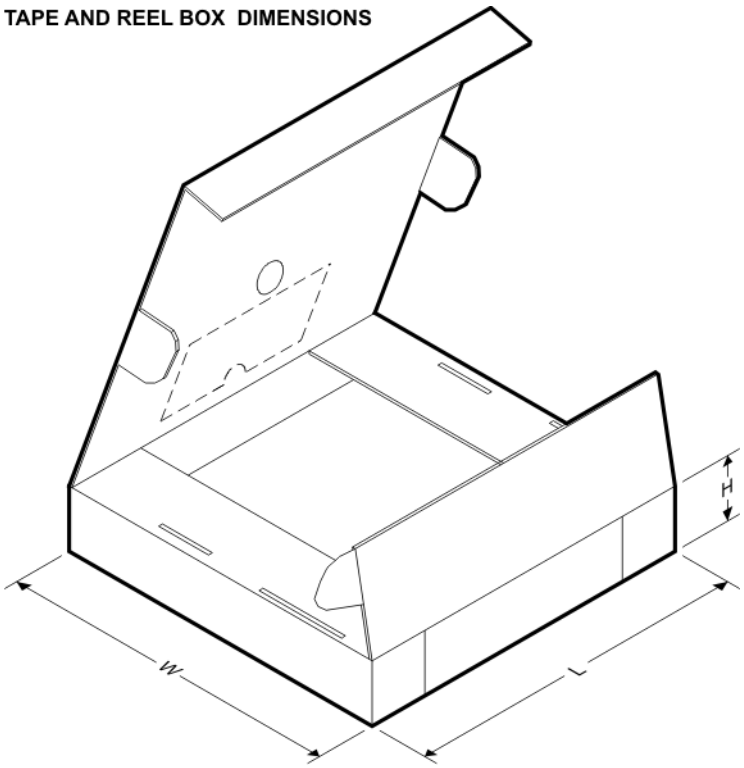


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5100AMRX/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5100AMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5100ASD	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5100ASD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5100ASDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5100BMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5100BSD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5100BSDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5100CMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5100CMY/NOPB	MSOP-Power PAD	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5100CMYE/NOPB	MSOP-Power PAD	DGN	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5100CMYX/NOPB	MSOP-Power PAD	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5100CSD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5100CSDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101AMRX/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5101AMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5101ASD	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101ASD-1/NOPB	WSON	NGT	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101ASD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101ASDX	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101ASDX-1/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101ASDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101BMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5101BSD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101BSDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101CMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5101CMY/NOPB	MSOP-Power PAD	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5101CMYE/NOPB	MSOP-Power PAD	DGN	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5101CMYX/NOPB	MSOP-Power PAD	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5101CSD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101CSDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

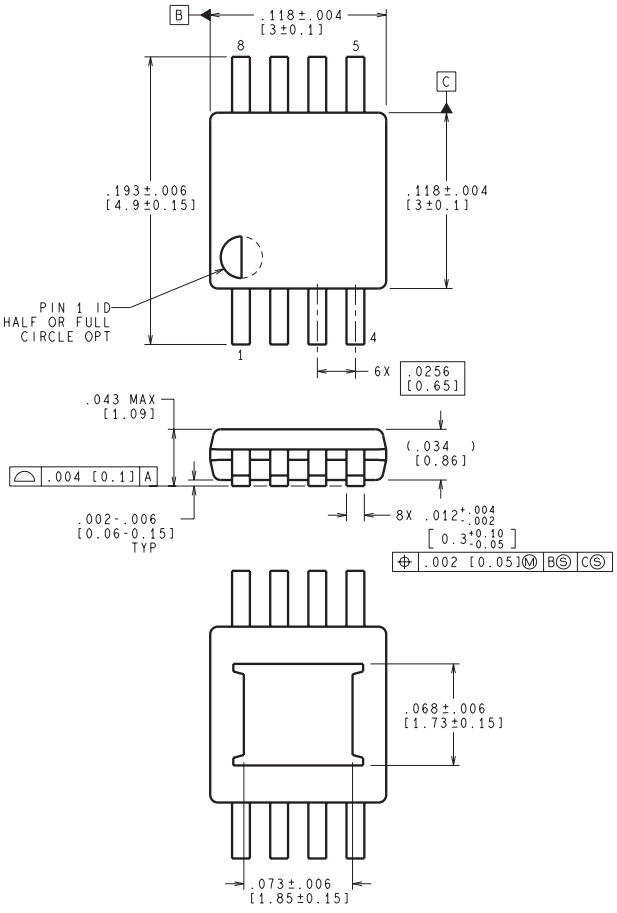


*All dimensions are nominal

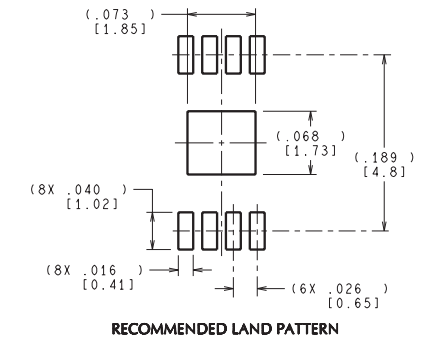
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5100AMRX/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LM5100AMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5100ASD	WSON	DPR	10	1000	210.0	185.0	35.0
LM5100ASD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5100ASDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0
LM5100BMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5100BSD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5100BSDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0
LM5100CMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5100CMY/NOPB	MSOP-PowerPAD	DGN	8	1000	210.0	185.0	35.0
LM5100CMYE/NOPB	MSOP-PowerPAD	DGN	8	250	210.0	185.0	35.0
LM5100CMYX/NOPB	MSOP-PowerPAD	DGN	8	3500	367.0	367.0	35.0
LM5100CSD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5100CSDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0
LM5101AMRX/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LM5101AMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5101ASD	WSON	DPR	10	1000	210.0	185.0	35.0
LM5101ASD-1/NOPB	WSON	NGT	8	1000	210.0	185.0	35.0
LM5101ASD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5101ASDX	WSON	DPR	10	4500	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5101ASDX-1/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0
LM5101ASDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0
LM5101BMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5101BSD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5101BSDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0
LM5101CMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5101CMY/NOPB	MSOP-PowerPAD	DGN	8	1000	210.0	185.0	35.0
LM5101CMYE/NOPB	MSOP-PowerPAD	DGN	8	250	210.0	185.0	35.0
LM5101CMYX/NOPB	MSOP-PowerPAD	DGN	8	3500	367.0	367.0	35.0
LM5101CSD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5101CSDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0

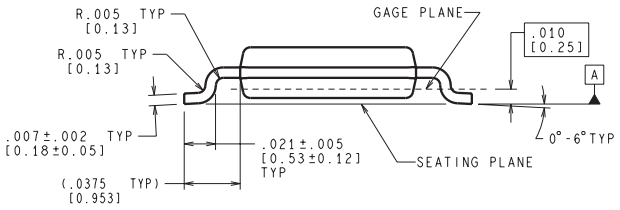
DGN0008A



BOTTOM VIEW



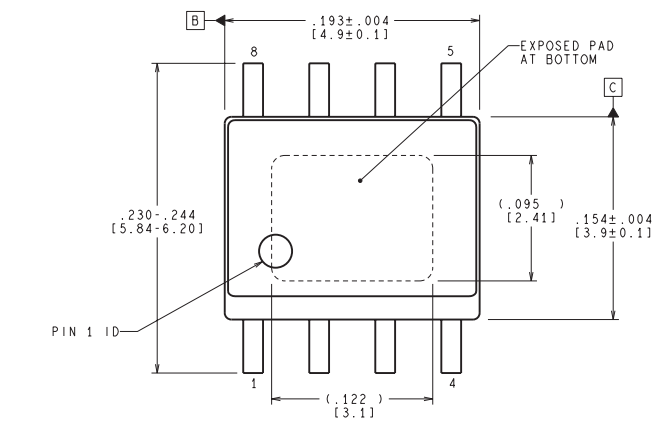
RECOMMENDED LAND PATTERN

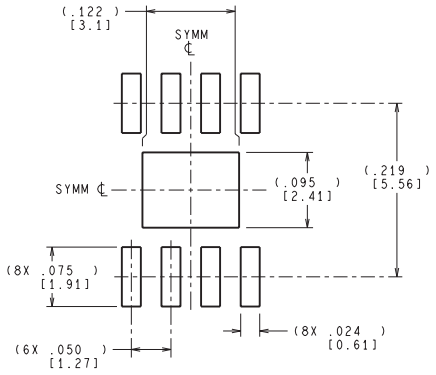


CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MUY08A (Rev A)

DDA0008B





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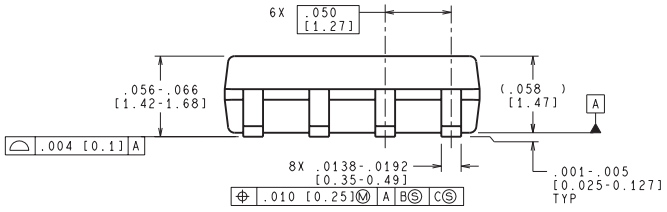
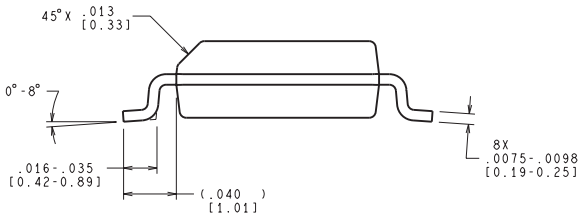
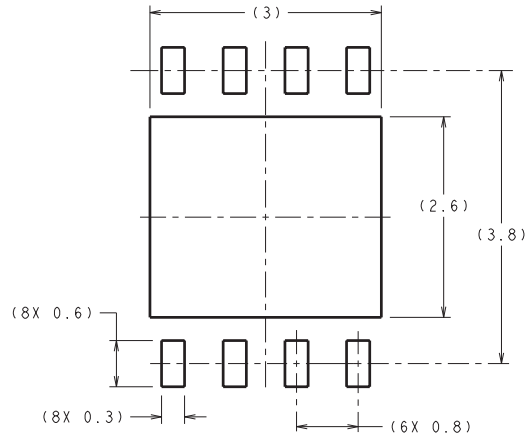




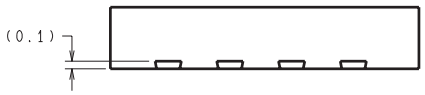
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MRA08B (Rev B)

NGT0008A



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



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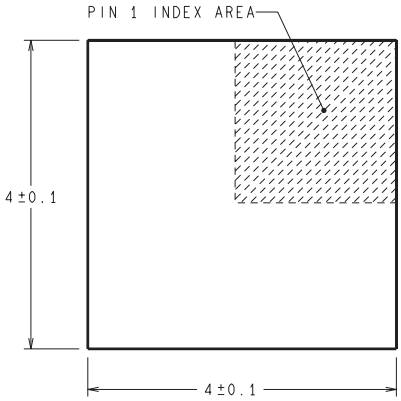
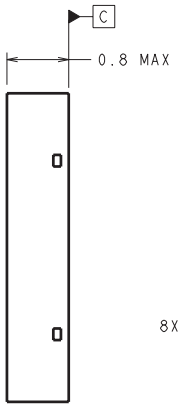
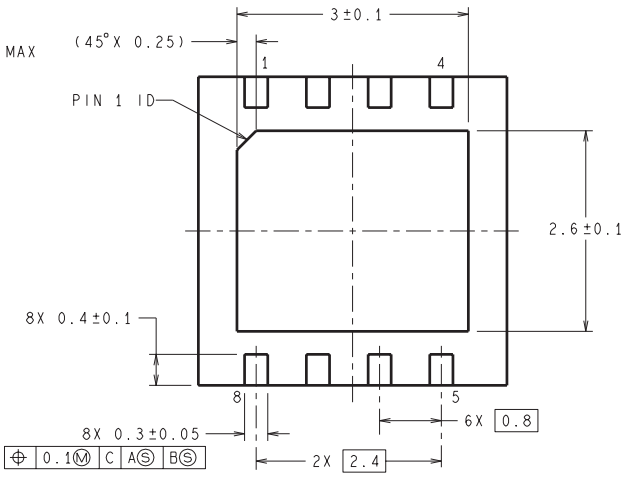






SDC08A (Rev A)

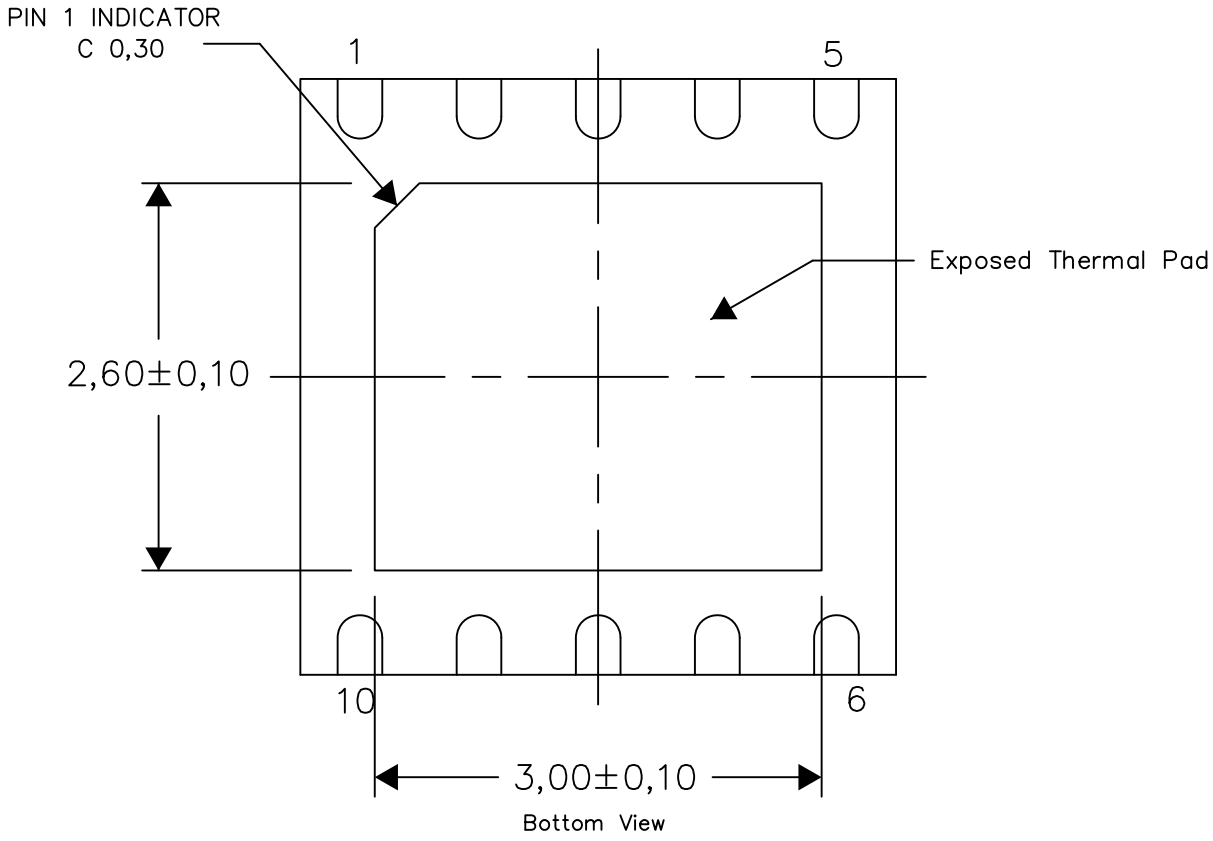
DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

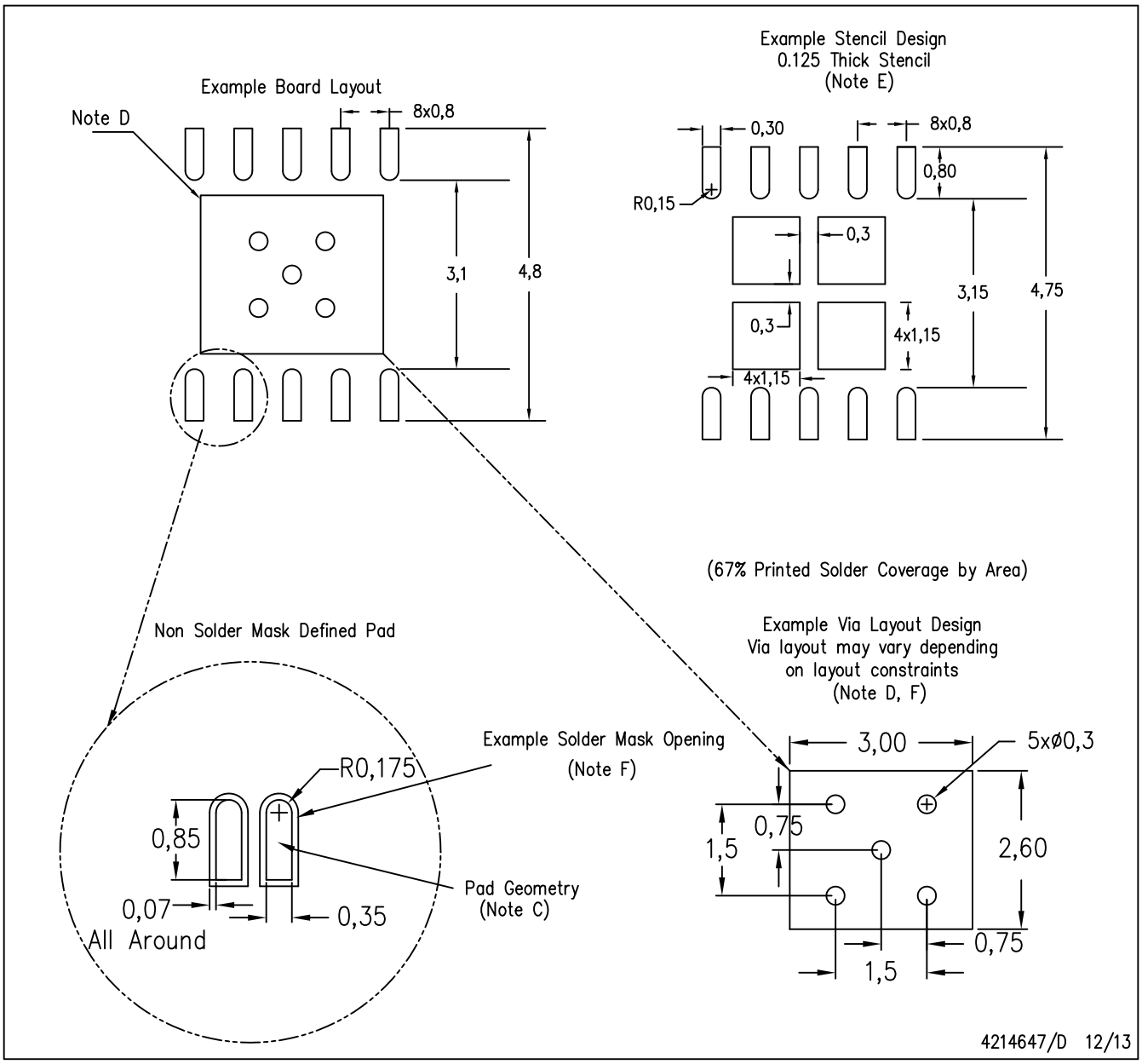


Exposed Thermal Pad Dimensions

4211551/C 12/13

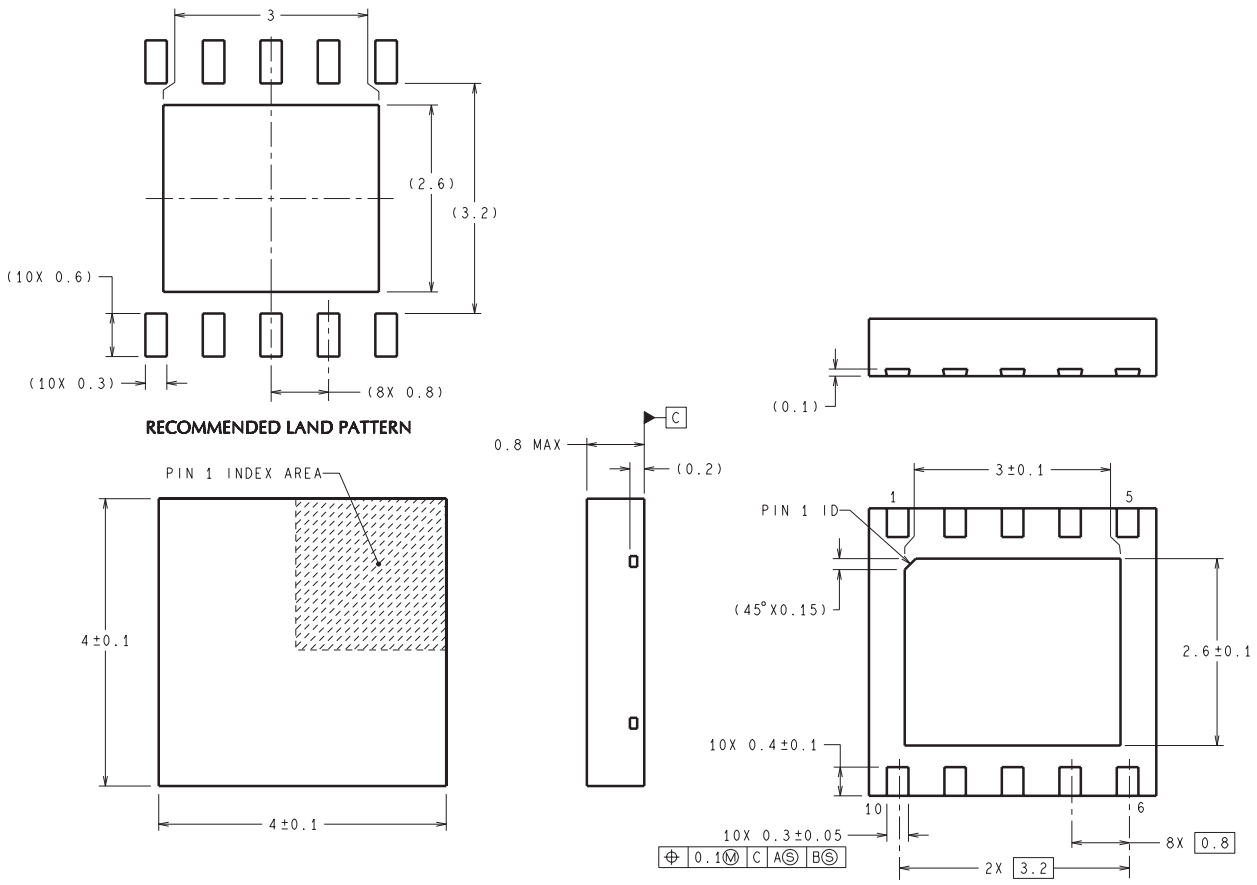
NOTES: All linear dimensions are in millimeters

DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



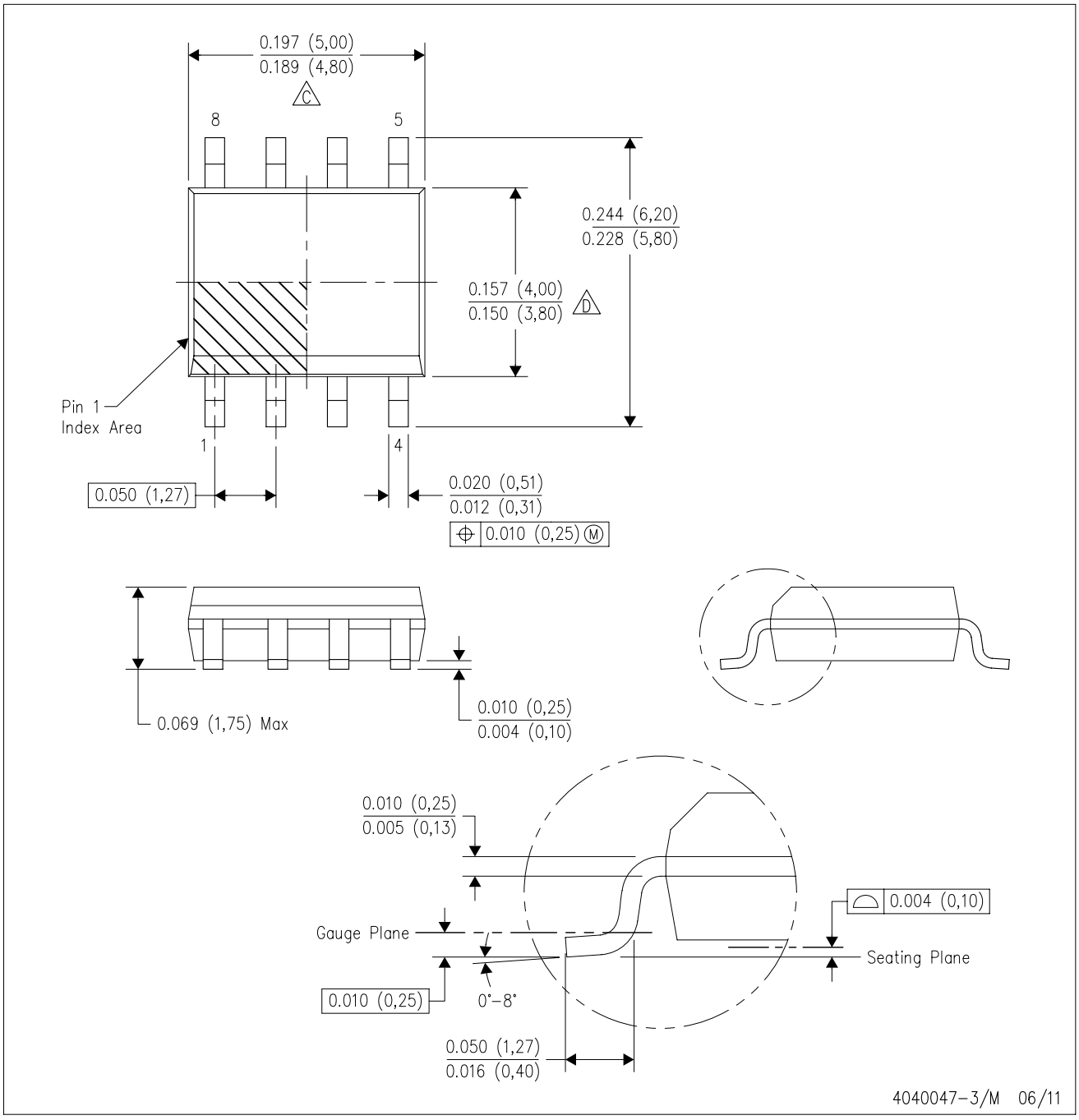
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DPR0010A



SDC10A (Rev A)

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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