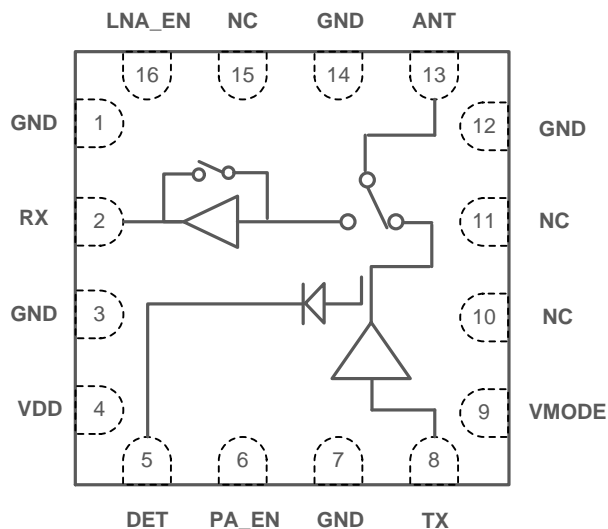


# CMOS 5GHz WLAN 802.11a/n/ac RFeIC with PA, LNA, and SPDT



## Description

RFX8055 is a highly integrated, single-chip, single-die RFeIC (RF Front-end Integrated Circuit) which incorporates key RF functionality needed for IEEE 802.11a/n/ac WLAN systems operating in the 5.1-5.95GHz range. The RFX8055 architecture integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network, LO rejection, and harmonic filters all in a CMOS single-chip device.

RFX8055 has simple and low-voltage CMOS control logic, and requires minimal external components. A directional coupler based power detect circuit is also integrated for accurate monitoring of output power from the PA.

RFX8055 is assembled in an ultra-compact low-profile 2.3x2.3x0.4 mm 16-lead QFN package. With support to direct battery operation, the RFX8055 is ideal RF front-end solution for implementing 5GHz WLAN in smartphones and other mobile platforms.

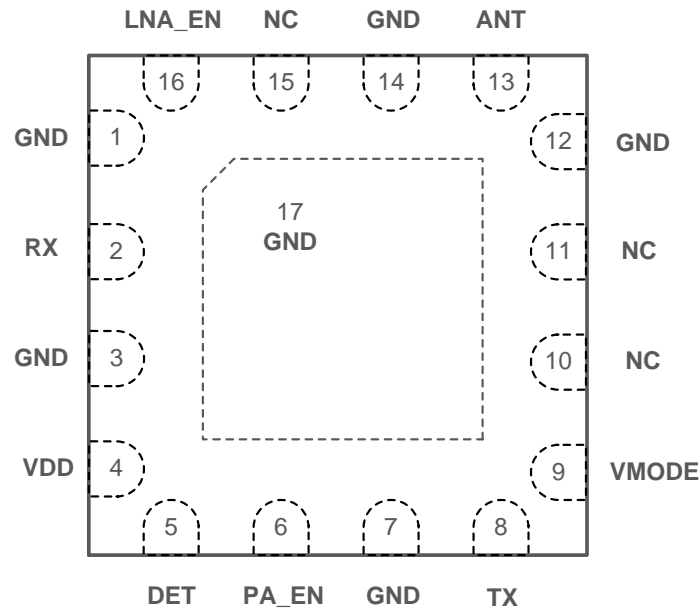
## Applications

- ▶ 802.11a/n/ac
- ▶ Smartphones
- ▶ Tablets/MIDs
- ▶ Consumer Electronics
- ▶ Notebook/Netbook/Ultrabooks
- ▶ Mobile/Portable Devices
- ▶ Access Points / Gateways
- ▶ Other 5GHz ISM Platforms

## FEATURES

- ▶ 5GHz WLAN Single Chip, Single-Die RF Front-End IC
- ▶ High Transmit Signal Linearity Meeting Standards for 802.11ac OFDM /MCS9 Modulation
- ▶ Separate TX, RX Transceiver Ports, Single Antenna Port
- ▶ 5GHz Power Amplifier with Low-Pass Harmonic Filter
- ▶ Low Noise Amplifier with Bypass Mode
- ▶ Transmit/Receive Switch Circuitry
- ▶ Integrated Power Detector for Transmit Power Monitor and Control
- ▶ Low Voltage (1.2V) CMOS Control Logic
- ▶ Low-Current Mode in TX for Battery Current Savings
- ▶ ESD Protection Circuitry on all Pins
- ▶ DC Decoupled RF Ports
- ▶ Internal RF Decoupling on All VDD Bias Pins
- ▶ Low Noise Figure for the Receive Chain
- ▶ High Power Capability for Received Signals in Bypass Mode
- ▶ Low DC Power Consumption
- ▶ On-chip Matching Circuit with 50Ω Input/Output
- ▶ Minimal External Components Required
- ▶ Market Proven Bulk CMOS Technology
- ▶ 2.3mm x 2.3mm x 0.4mm Small Outline 16L QFN Package with Exposed Ground Pad
- ▶ RoHS and REACH Compliant

### PIN-OUT DIAGRAM:



(Top "See-Through" View)

### PIN ASSIGNMENTS:

| Pin Number      | Pin Name | Description  |
|-----------------|----------|--|
| 10, 11, 15      | NC       | Internally Not Connected   |
| 2               | RX       | RF Output Port from LNA or Bypass – DC Shorted to GND                                    |
| 4               | VDD      | DC Supply Voltage  |
| 5               | DET      | Analog Voltage Proportional to the PA Power Output                                       |
| 6               | PA_EN    | CMOS Input to Control TX Enable  |
| 8               | TX       | RF Input Port from the Transceiver – DC Shorted to GND                                   |
| 9               | VMODE    | CMOS Input to Control High-Linearity/Low-Current Mode                                    |
| 13              | ANT      | Antenna Port (RF Signal from the PA or RF Signal Applied to the LNA) – DC Shorted to GND |
| 16              | LNA_EN   | CMOS Input to Control RX Enable  |
| 1, 3, 7, 12, 14 | GND      | Ground – Must Be Connected to GND in the Application Circuit                             |

**ABSOLUTE MAXIMUM RATINGS:**

| Parameters                    | Units | Min  | Max  | Conditions   |
|-------------------------------|-------|------|------|--|
| DC VDD Voltage Supply         | V     | -0.3 | 4.0  | At VDD Pin   |
| DC Control Pin Voltage        | V     | -0.3 | 3.6  | All Control Pins   |
| DC Voltage at Det Pin         | V     | -0.3 | 3.6  | External voltage applied to Detector Pin                             |
| DC VDD Current Consumption    | mA    |      | 400  | Through VDD Pin when TX is "ON"                                      |
| TX RF Input Power             | dBm   |      | +7   | CW and all modulation types in accordance with 802.11a/n/ac standard |
| ANT RF Input Power            | dBm   |      | +10  |  |
| Junction Temperature          | °C    |      | 150  |  |
| Storage Ambient Temperature   | °C    | -40  | +150 | Appropriate care required according to JEDEC Standards               |
| Operating Ambient Temperature | °C    | -20  | +85  |  |
| Moisture Sensitivity          |       |      |      | MSL1   |

*Note: Sustained operation at or above the Absolute Maximum Ratings for any one or combinations of the above parameters may result in permanent damage to the device and is not recommended. All Maximum RF Input Power Ratings assume 50-Ohm terminal impedance.*

**NOMINAL OPERATING CONDITIONS:**

| Parameters                         | Units | Min | Typ | Max | Conditions                       |
|------------------------------------|-------|-----|-----|-----|----------------------------------|
| DC VDD Voltage Supply (Note 1)     | V     | 3.0 | 3.3 | 3.6 | All VDD Pins                     |
| Control Voltage "High" (Note 2)    | V     | 1.2 |     | *   | * 3.6V or VDD Whichever is Lower |
| Control Voltage "Low"              | V     | 0   |     | 0.4 |                                  |
| DC Control Pin Current Consumption | μA    |     | 1   |     |                                  |
| DC Shutdown Current                | μA    |     | 3   |     |                                  |
| PA Turn On/Off Time                | μsec  |     | 0.4 |     |                                  |
| LNA Turn On/Off Time               | μsec  |     | 0.4 |     |                                  |
| θ <sub>jc</sub> (Note 3)           | °C/W  |     | 27  |     |                                  |
| θ <sub>ja</sub>                    | °C/W  |     | 64  |     |                                  |

*Note 1: For normal operation of the RFX8055, VDD must be continuously applied to VDD supply pin.*

*Note 2: If control voltage can exceed 1.8V, a 1KΩ – 10KΩ series resistor is recommended for the application circuit on each control line.*

*Note 3: Thermal measurements were performed on an RFAxis test EVB under typical use conditions. Please contact RFAxis for details regarding the test conditions and the configuration of the thermal vias on the EVB. Refer to "PCB Land Pattern" for recommended thermal vias.*

**TRANSMIT PATH CHARACTERISTICS HIGH LINEARITY MODE (VDD=3.3V; T=+25 °C)**

| Parameters                    | Units   | Min | Typ      | Max  | Conditions  |
|-------------------------------|---------|-----|----------|------|---|
| Operating Frequency Band      | GHz     | 5.1 |          | 5.95 |   |
| Linear Output Power 1         | dBm     |     | +16.5    |      | For DEVM<1.8%, 802.11ac, MCS9/VHT80                       |
| Linear Output Power 2         | dBm     |     | +17      |      | For DEVM<2.5%, 802.11n, MCS7/HT40                         |
| Linear Output Power 3         | dBm     |     | +17.5    |      | For DEVM<3%, 802.11a, 64QAM/54Mbps                        |
| Linear Output Power 4         | dBm     |     | +20.5    |      | For MCS0/6Mbps, 802.11a Mask Compliance with 1.5dB Margin |
| Small-Signal Power Gain       | dB      |     | 27       |      |   |
| TX Quiescent Current          | mA      |     | 150      |      | No RF Applied   |
| TX Linear Current             | mA      |     | 230      |      | P <sub>OUT</sub> = +18dBm                                 |
| Power Detector Voltage Output | mV      |     | 200-1400 |      | P <sub>OUT</sub> = +8 to +20dBm, 10kΩ Load                |
| Second Harmonic               | dBm/MHz |     | -30      |      | P <sub>OUT</sub> =+20dBm, 802.11a, MCS0, 6Mbps            |
| Third Harmonic                | dBm/MHz |     | -25      |      | P <sub>OUT</sub> =+20dBm, 802.11a, MCS0, 6Mbps            |
| Input Return Loss             | dB      |     | -10      |      | At TX Pin   |
| Output Return Loss            | dB      |     | -10      |      | At ANT Pin  |

**TRANSMIT PATH CHARACTERISTICS LOW CURRENT MODE (VDD=3.3V; T=+25 °C)**

| Parameters               | Units | Min | Typ   | Max  | Conditions  |
|--------------------------|-------|-----|-------|------|---|
| Operating Frequency Band | GHz   | 5.1 |       | 5.95 |   |
| Linear Output Power 1    | dBm   |     | +14.5 |      | For DEVM<1.8%, 802.11ac, MCS9/VHT80                       |
| Linear Output Power 2    | dBm   |     | +15   |      | For DEVM<2.5%, 802.11n, MCS7/HT40                         |
| Linear Output Power 3    | dBm   |     | +16   |      | For DEVM<3%, 802.11a, 64QAM/54Mbps                        |
| Linear Output Power 4    | dBm   |     | +20   |      | For MCS0/6Mbps, 802.11a Mask Compliance with 1.5dB Margin |
| Small-Signal Power Gain  | dB    |     | 26    |      |   |
| TX Quiescent Current     | mA    |     | 110   |      | No RF Applied   |
| TX Linear Current        | mA    |     | 205   |      | P <sub>OUT</sub> = +18dBm                                 |

**RECEIVE PATH CHARACTERISTICS (VDD=3.3V; T=+25 °C)**

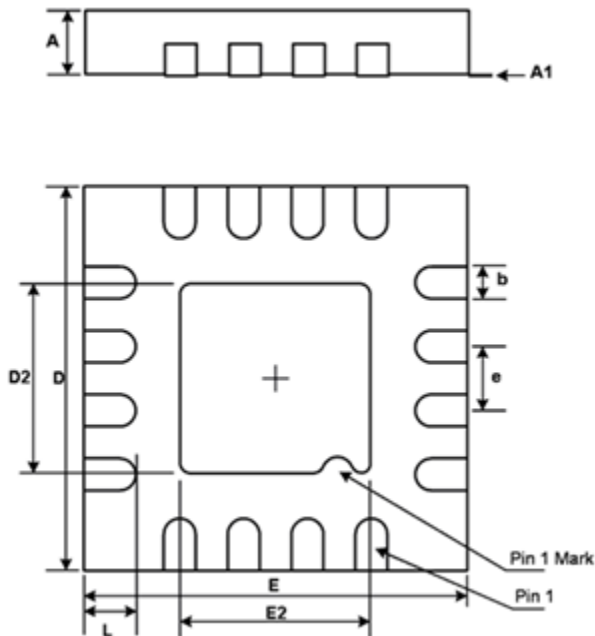
| Parameters                     | Units | Min | Typ | Max  | Conditions                              |
|--------------------------------|-------|-----|-----|------|---|
| Operating Frequency Band       | GHz   | 5.1 |     | 5.95 | All RF Pins are Loaded by 50-Ohm        |
| Gain                           | dB    |     | 13  |      | Receive Mode, LNA On                    |
| Noise Figure                   | dB    |     | 2.9 |      | Receive Mode, LNA On                    |
| DC Quiescent Current           | mA    |     | 13  |      | No RF Applied, Through VDD Pin          |
| Receive IIP3                   | dBm   |     | +5  |      | Minimum value over PVT<br>IIP3=0dBm     |
| LNA Bypass Mode Insertion Loss | dB    |     | 6   |      |   |
| LNA Bypass Mode Current        | μA    |     | 3   |      | LNA Off, No RF applied, through VDD Pin |
| Input Return Loss              | dB    |     | -9  |      | At ANT Pin                              |
| Output Return Loss             | dB    |     | -9  |      | At RX Pin                               |
| RF Port Impedance              | Ohm   |     | 50  |      |   |

**CONTROL LOGIC TRUTH TABLE**

| PA_EN      | LNA_EN | VMODE | Mode Of Operation            |
|------------|--------|-------|------------------------------|
| 0          | 0      | X     | Shutdown/LNA Bypass Mode     |
| 1          | 0      | 0     | High Linearity Transmit Mode |
| 0          | 1      | X     | Receive Mode, LNA On         |
| 1          | 0      | 1     | Low Current Transmit Mode    |
| 1          | 1      | X     | Low Current Transmit Mode    |
| All Others |        |       | Unsupported (No Damage)      |

Note: "1" denotes high voltage state (> 1.2V)  
 "0" denotes low voltage state (<0.4V) at Control Pins  
 "X" denotes the don't care state  
 1KΩ – 10KΩ series resistor may be required for each control line

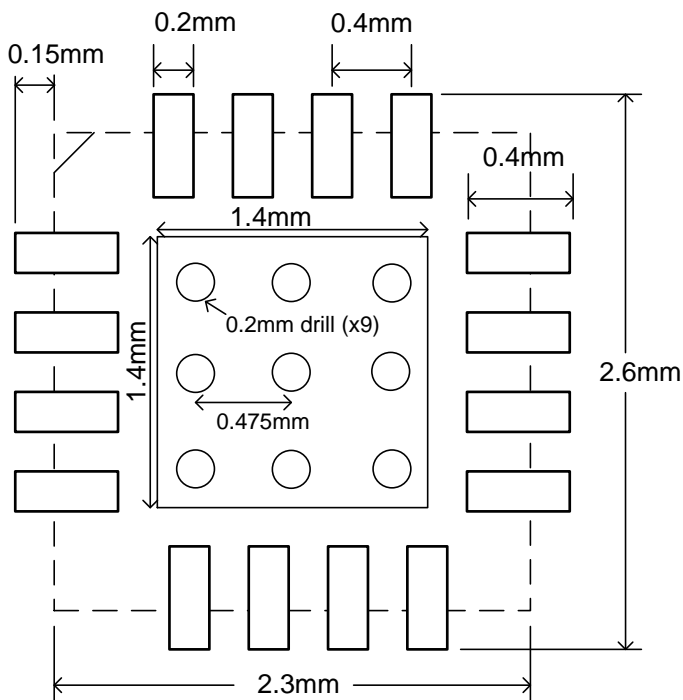
PACKAGE DIMENSIONS (All Dimensions in mm):



| Dimensional Ref. |           |       |       |
|------------------|-----------|-------|-------|
| REF.             | Min.      | Nom.  | Max.  |
| A                | -         | -     | 0.400 |
| A1               | 0.000     | -     | 0.050 |
| D                | 2.300 BSC |       |       |
| E                | 2.300 BSC |       |       |
| D2               | 1.350     | 1.400 | 1.450 |
| E2               | 1.350     | 1.400 | 1.450 |
| b                | 0.150     | 0.200 | 0.250 |
| e                | 0.400 BSC |       |       |
| L                | 0.200     | 0.250 | 0.300 |

### PCB LAND PATTERN

(With Recommended Thermal Vias)



### PACKAGE MARKING

