

AD7476/AD7477/AD7478*

FEATURES

Fast Throughput Rate: 1 MSPS

Specified for V_{DD} of 2.35 V to 5.25 V

Low Power:

3.6 mW Typ at 1 MSPS with 3 V Supplies

15 mW Typ at 1 MSPS with 5 V Supplies

Wide Input Bandwidth:

70 dB SNR at 100 kHz Input Frequency

Flexible Power/Serial Clock Speed Management

No Pipeline Delays

High Speed Serial Interface

SPI®/QSPI™/MICROWIRE™/DSP Compatible

Standby Mode: 1 μ A Max

6-Lead SOT-23 Package

APPLICATIONS

Battery-Powered Systems

Personal Digital Assistants

Medical Instruments

Mobile Communications

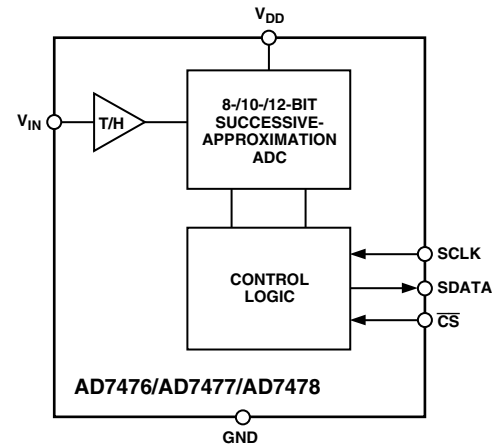
Instrumentation and Control Systems

Data Acquisition Systems

High Speed Modems

Optical Sensors

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7476/AD7477/AD7478 are, respectively, 12-bit, 10-bit, and 8-bit, high speed, low power, successive-approximation ADCs. The parts operate from a single 2.35 V to 5.25 V power supply and feature throughput rates up to 1 MSPS. The parts contain a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 6 MHz.

The conversion process and data acquisition are controlled using \overline{CS} and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of \overline{CS} and the conversion is also initiated at this point. There are no pipeline delays associated with the part.

The AD7476/AD7477/AD7478 use advanced design techniques to achieve very low power dissipation at high throughput rates.

The reference for the part is taken internally from V_{DD} . This allows the widest dynamic input range to the ADC. Thus the analog input range for the part is 0 V to V_{DD} . The conversion rate is determined by the SCLK.

PRODUCT HIGHLIGHTS

1. First 12-/10-/8-Bit ADCs in a SOT-23 Package.
2. High Throughput with Low Power Consumption.
3. Flexible Power/Serial Clock Speed Management.
The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through the serial clock speed increase. This allows the average power consumption to be reduced while not converting. The part also features a shutdown mode to maximize power efficiency at lower throughput rates. Current consumption is 1 μ A maximum when in shutdown.
4. Reference Derived from the Power Supply.
5. No Pipeline Delay.
The parts feature a standard successive-approximation ADC with accurate control of the sampling instant via a \overline{CS} input and once-off conversion control.

*Protected by U.S. Patent No. 6,681,332.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
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AD7476—SPECIFICATIONS

(A Version: $V_{DD} = 2.7\text{ V to }5.25\text{ V}$, $f_{SCLK} = 20\text{ MHz}$, $f_{SAMPLE} = 1\text{ MSPS}$, unless otherwise noted; S and B Versions: $V_{DD} = 2.35\text{ V to }5.25\text{ V}$, $f_{SCLK} = 12\text{ MHz}$, $f_{SAMPLE} = 600\text{ kSPS}$, unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

Parameter	A Version ^{1,2}	B Version ^{1,2}	S Version ^{1,2}	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Signal-to-(Noise + Distortion) (SINAD) ³	69 70	70	69 70	dB min dB min	$f_{IN} = 100\text{ kHz}$ Sine Wave B Version, $V_{DD} = 2.4\text{ V to }5.25\text{ V}$ $T_A = 25^\circ\text{C}$
Signal-to-Noise Ratio (SNR) ³	70	71.5 71 72.5	70	dB typ dB min dB typ	B Version, $V_{DD} = 2.4\text{ V to }5.25\text{ V}$
Total Harmonic Distortion (THD) ³	-80	-78	-78	dB typ	
Peak Harmonic or Spurious Noise (SFDR) ³	-82	-80	-80	dB typ	
Intermodulation Distortion (IMD) ³					
Second-Order Terms	-78	-78	-78	dB typ	$f_a = 103.5\text{ kHz}$, $f_b = 113.5\text{ kHz}$
Third-Order Terms	-78	-78	-78	dB typ	$f_a = 103.5\text{ kHz}$, $f_b = 113.5\text{ kHz}$
Aperture Delay	10	10	10	ns typ	
Aperture Jitter	30	30	30	ps typ	
Full Power Bandwidth	6.5	6.5	6.5	MHz typ	@ 3 dB
DC ACCURACY					
Resolution	12	12	12	Bits	S, B Versions, $V_{DD} = (2.35\text{ V to }3.6\text{ V})^4$; A Version, $V_{DD} = (2.7\text{ V to }3.6\text{ V})$
Integral Nonlinearity ³		± 1.5	± 1.5	LSB max	
	± 1	± 0.6	± 0.6	LSB typ	
Differential Nonlinearity ³		$-0.9/+1.5$	$-0.9/+1.5$	LSB max	Guaranteed No Missed Codes to 12 Bits
	± 0.75	± 0.75	± 0.75	LSB typ	
Offset Error ³		± 1.5	± 2	LSB max	
	± 0.5			LSB typ	
Gain Error ³		± 1.5	± 2	LSB max	
	± 0.5			LSB typ	
ANALOG INPUT					
Input Voltage Ranges	0 to V_{DD}	0 to V_{DD}	0 to V_{DD}	V	
DC Leakage Current	± 1	± 1	± 1	$\mu\text{A max}$	
Input Capacitance	30	30	30	pF typ	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4 1.8	2.4 1.8	2.4 1.8	V min V min	$V_{DD} = 2.35\text{ V}$
Input Low Voltage, V_{INL}	0.4 0.8	0.4 0.8	0.4 0.8	V max V max	$V_{DD} = 3\text{ V}$ $V_{DD} = 5\text{ V}$
Input Current, I_{IN} , SCLK Pin	± 1	± 1	± 1	$\mu\text{A max}$	Typically 10 nA, $V_{IN} = 0\text{ V or }V_{DD}$
Input Current, I_{IN} , $\overline{\text{CS}}$ Pin	± 1	± 1	± 1	$\mu\text{A typ}$	
Input Capacitance, C_{IN}^5	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	$V_{DD} - 0.2$	$V_{DD} - 0.2$	$V_{DD} - 0.2$	V min	$I_{SOURCE} = 200\text{ }\mu\text{A}$; $V_{DD} = 2.35\text{ V to }5.25\text{ V}$
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	$I_{SINK} = 200\text{ }\mu\text{A}$
Floating-State Leakage Current	± 10	± 10	± 10	$\mu\text{A max}$	
Floating-State Output Capacitance ⁵	10	10	10	pF max	
Output Coding	Straight (Natural) Binary				
CONVERSION RATE					
Conversion Time	0.8	1.33	1.33	$\mu\text{s max}$	16 SCLK Cycles
Track-and-Hold Acquisition Time	500 350	500 400	500 400	ns max ns max	Full-Scale Step Input Sine Wave Input $\leq 100\text{ kHz}$
Throughput Rate	1000	600	600	kSPS max	See Serial Interface Section
POWER REQUIREMENTS					
V_{DD}	2.35/5.25	2.35/5.25	2.35/5.25	V min/max	Digital I/Ps = 0 V or V_{DD}
I_{DD}					$V_{DD} = 4.75\text{ V to }5.25\text{ V}$. SCLK On or Off
Normal Mode (Static)	2	2	2	mA typ	$V_{DD} = 2.35\text{ V to }3.6\text{ V}$. SCLK On or Off
Normal Mode (Operational)	1 3.5	1 3	1 3	mA typ mA max	$V_{DD} = 4.75\text{ V to }5.25\text{ V}$; $f_{SAMPLE} = f_{SAMPLE}^{MAX6}$
Full Power-Down Mode	1.6	1.4	1.4	mA max	$V_{DD} = 2.35\text{ V to }3.6\text{ V}$; $f_{SAMPLE} = f_{SAMPLE}^{MAX6}$
Power Dissipation ⁷	1	1	1	$\mu\text{A max}$	SCLK Off
Normal Mode (Operational)	80	80	80	$\mu\text{A max}$	SCLK On
Full Power-Down					
Normal Mode (Operational)	17.5	15	15	mW max	$V_{DD} = 5\text{ V}$; $f_{SAMPLE} = f_{SAMPLE}^{MAX6}$
Full Power-Down	4.8	4.2	4.2	mW max	$V_{DD} = 3\text{ V}$; $f_{SAMPLE} = f_{SAMPLE}^{MAX6}$
Normal Mode (Operational)	5	5	5	$\mu\text{W max}$	$V_{DD} = 5\text{ V}$; SCLK Off
Full Power-Down	3	3	3	$\mu\text{W max}$	$V_{DD} = 3\text{ V}$; SCLK Off

NOTES

¹Temperature ranges as follows: A, B Versions: $-40^\circ\text{C to }+85^\circ\text{C}$; S Version: $-55^\circ\text{C to }+125^\circ\text{C}$.

²Operational from $V_{DD} = 2.0\text{ V}$.

³See Terminology section.

⁴Maximum B, S version specifications apply as typical figures when $V_{DD} = 5.25\text{ V}$.

⁵Guaranteed by characterization.

⁶A Version: $f_{SAMPLE}^{MAX} = 1\text{ MSPS}$; B, S Versions: $f_{SAMPLE}^{MAX} = 600\text{ kSPS}$.

⁷See Power vs. Throughput Rate section.

Specifications subject to change without notice.

AD7477—SPECIFICATIONS¹ ($V_{DD} = 2.7\text{ V to }5.25\text{ V}$, $f_{SCLK} = 20\text{ MHz}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

Parameter	A Version ^{1,2}	S Version ^{1,2}	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal-to-(Noise + Distortion) (SINAD)	61	61	dB min	$f_{IN} = 100\text{ kHz}$ Sine Wave, $f_{SAMPLE} = 1\text{ MSPS}$
Total Harmonic Distortion (THD)	-73	-73	dB max	
Peak Harmonic or Spurious Noise (SFDR)	-74	-74	dB max	
Intermodulation Distortion (IMD)				
Second-Order Terms	-78	-78	dB typ	$f_a = 103.5\text{ kHz}$, $f_b = 113.5\text{ kHz}$
Third-Order Terms	-78	-78	dB typ	$f_a = 103.5\text{ kHz}$, $f_b = 113.5\text{ kHz}$
Aperture Delay	10	10	ns typ	
Aperture Jitter	30	30	ps typ	
Full Power Bandwidth	6.5	6.5	MHz typ	@ 3 dB
DC ACCURACY				
Resolution	10	10	Bits	
Integral Nonlinearity	±1	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	LSB max	Guaranteed No Missed Codes to 10 Bits
Offset Error	±1	±1	LSB max	
Gain Error	±1	±1	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{DD}	0 to V_{DD}	V	
DC Leakage Current	±1	±1	μA max	
Input Capacitance	30	30	pF typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	$V_{DD} = 5\text{ V}$
	0.4	0.4	V max	$V_{DD} = 3\text{ V}$
Input Current, I_{IN} , SCLK Pin	±1	±1	μA max	Typically 10 nA, $V_{IN} = 0\text{ V}$ or V_{DD}
Input Current, I_{IN} , \overline{CS} Pin	±1	±1	μA typ	
Input Capacitance, C_{IN}^4	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	$V_{DD} - 0.2$	$V_{DD} - 0.2$	V min	$I_{SOURCE} = 200\text{ μA}$; $V_{DD} = 2.7\text{ V to }5.25\text{ V}$
Output Low Voltage, V_{OL}	0.4	0.4	V max	$I_{SINK} = 200\text{ μA}$
Floating-State Leakage Current	±10	±10	μA max	
Floating-State Output Capacitance ⁴	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	800	800	ns max	16 SCLK Cycles with SCLK at 20 MHz
Track-and-Hold Acquisition Time	400	400	ns max	
Throughput Rate	1	1	MSPS max	See Serial Interface Section
POWER REQUIREMENTS				
V_{DD}	2.7/5.25	2.7/5.25	V min/max	
I_{DD}				Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	2	2	mA typ	$V_{DD} = 4.75\text{ V to }5.25\text{ V}$; SCLK On or Off
Normal Mode (Operational)	1	1	mA typ	$V_{DD} = 2.7\text{ V to }3.6\text{ V}$; SCLK On or Off
Full Power-Down Mode	3.5	3.5	mA max	$V_{DD} = 4.75\text{ V to }5.25\text{ V}$; $f_{SAMPLE} = 1\text{ MSPS}$
Power Dissipation ⁵	1.6	1.6	mA max	$V_{DD} = 2.7\text{ V to }3.6\text{ V}$; $f_{SAMPLE} = 1\text{ MSPS}$
Normal Mode (Operational)	1	1	μA max	SCLK Off
Full Power-Down	80	80	μA max	SCLK On
Power Dissipation ⁵				
Normal Mode (Operational)	17.5	17.5	mW max	$V_{DD} = 5\text{ V}$; $f_{SAMPLE} = 1\text{ MSPS}$
Full Power-Down	4.8	4.8	mW max	$V_{DD} = 3\text{ V}$; $f_{SAMPLE} = 1\text{ MSPS}$
Full Power-Down	5	5	μW max	$V_{DD} = 5\text{ V}$; SCLK Off

NOTES

¹Temperature ranges as follows: A Version: -40°C to +85°C; S Version: -55°C to +125°C.

²Operational from $V_{DD} = 2.0\text{ V}$, with input high voltage, $V_{INH} = 1.8\text{ V}$ min.

³See Terminology section.

⁴Guaranteed by characterization.

⁵See Power vs. Throughput Rate section.

Specifications subject to change without notice.

AD7478—SPECIFICATIONS¹ ($V_{DD} = 2.7\text{ V to }5.25\text{ V}$, $f_{SCLK} = 20\text{ MHz}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

Parameter	A Version ^{1,2}	S Version ^{1,2}	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal-to-(Noise + Distortion) (SINAD)	49	49	dB min	$f_{IN} = 100\text{ kHz Sine Wave}$, $f_{SAMPLE} = 1\text{ MSPS}$ $f_a = 498.7\text{ kHz}$, $f_b = 508.7\text{ kHz}$ $f_a = 498.7\text{ kHz}$, $f_b = 508.7\text{ kHz}$ @ 3 dB
Total Harmonic Distortion (THD)	-65	-65	dB max	
Peak Harmonic or Spurious Noise (SFDR)	-65	-65	dB max	
Intermodulation Distortion (IMD)				
Second-Order Terms	-68	-68	dB typ	
Third-Order Terms	-68	-68	dB typ	
Aperture Delay	10	10	ns typ	
Aperture Jitter	30	30	ps typ	
Full Power Bandwidth	6.5	6.5	MHz typ	
DC ACCURACY				
Resolution	8	8	Bits	Guaranteed No Missed Codes to Eight Bits
Integral Nonlinearity	± 0.5	± 0.5	LSB max	
Differential Nonlinearity	± 0.5	± 0.5	LSB max	
Offset Error	± 0.5	± 0.5	LSB max	
Gain Error	± 0.5	± 0.5	LSB max	
Total Unadjusted Error (TUE)	± 0.5	± 0.5	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{DD}	0 to V_{DD}	V	
DC Leakage Current	± 1	± 1	$\mu\text{A max}$	
Input Capacitance	30	30	pF typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	$V_{DD} = 5\text{ V}$ $V_{DD} = 3\text{ V}$ Typically 10 nA, $V_{IN} = 0\text{ V or }V_{DD}$
Input Low Voltage, V_{INL}	0.8	0.8	V max	
	0.4	0.4	V max	
Input Current, I_{IN} , SCLK Pin	± 1	± 1	$\mu\text{A max}$	
Input Current, I_{IN} , \overline{CS} Pin	± 1	± 1	$\mu\text{A typ}$	
Input Capacitance, C_{IN}^4	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	$V_{DD} - 0.2$	$V_{DD} - 0.2$	V min	$I_{SOURCE} = 200\text{ }\mu\text{A}$; $V_{DD} = 2.7\text{ V to }5.25\text{ V}$ $I_{SINK} = 200\text{ }\mu\text{A}$
Output Low Voltage, V_{OL}	0.4	0.4	V max	
Floating-State Leakage Current	± 10	± 10	$\mu\text{A max}$	
Floating-State Output Capacitance ⁴	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	800	800	ns max	16 SCLK Cycles with SCLK at 20 MHz
Track-and-Hold Acquisition Time	400	400	ns max	
Throughput Rate	1	1	MSPS max	See Serial Interface Section
POWER REQUIREMENTS				
V_{DD}	2.7/5.25	2.7/5.25	V min/max	Digital I/Ps = 0 V or V_{DD} $V_{DD} = 4.75\text{ V to }5.25\text{ V}$; SCLK On or Off $V_{DD} = 2.7\text{ V to }3.6\text{ V}$; SCLK On or Off $V_{DD} = 4.75\text{ V to }5.25\text{ V}$; $f_{SAMPLE} = 1\text{ MSPS}$ $V_{DD} = 2.7\text{ V to }3.6\text{ V}$; $f_{SAMPLE} = 1\text{ MSPS}$ SCLK Off SCLK On
I_{DD}				
Normal Mode (Static)	2	2	mA typ	
	1	1	mA typ	
Normal Mode (Operational)	3.5	3.5	mA max	
	1.6	1.6	mA max	
Full Power-Down Mode	1	1	$\mu\text{A max}$	
	80	80	$\mu\text{A max}$	
Power Dissipation ⁵				
Normal Mode (Operational)	17.5	17.5	mW max	
	4.8	4.8	mW max	
Full Power-Down	5	5	$\mu\text{W max}$	

NOTES

¹Temperature ranges as follows: A Version: $-40^\circ\text{C to }+85^\circ\text{C}$; S Version: $-55^\circ\text{C to }+125^\circ\text{C}$.

²Operational from $V_{DD} = 2.0\text{ V}$, with input high voltage, $V_{INH} = 1.8\text{ V min}$.

³See Terminology section.

⁴Guaranteed by characterization.

⁵See Power vs. Throughput Rate section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS^{1, 2} ($V_{DD} = 2.35\text{ V to }5.25\text{ V}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

Parameter	Limit at T_{MIN} , T_{MAX} AD7476/AD7477/AD7478		Unit	Description
	3 V ³	5 V ³		
f_{SCLK} ⁴	10	10	kHz min	A Version B Version
	20	20	MHz max	
	12	12	MHz max	
$t_{CONVERT}$	$16 \times t_{SCLK}$	$16 \times t_{SCLK}$		
t_{QUIET}	50	50	ns min	Minimum Quiet Time Required between Bus Relinquish and Start of Next Conversion
t_1	10	10	ns min	Minimum \overline{CS} Pulsewidth
t_2	10	10	ns min	\overline{CS} to SCLK Setup Time
t_3 ⁵	20	20	ns max	Delay from \overline{CS} until SDATA Three-State Disabled
t_4 ⁵	40	20	ns max	Data Access Time after SCLK Falling Edge, A Version
	70	20	ns max	Data Access Time after SCLK Falling Edge, B Version
t_5	$0.4 \times t_{SCLK}$	$0.4 \times t_{SCLK}$	ns min	SCLK Low Pulsewidth
t_6	$0.4 \times t_{SCLK}$	$0.4 \times t_{SCLK}$	ns min	SCLK High Pulsewidth
t_7	10	10	ns min	SCLK to Data Valid Hold Time
t_8 ⁶	10	10	ns min	SCLK Falling Edge to SDATA High Impedance
	25	25	ns max	SCLK Falling Edge to SDATA High Impedance
$t_{POWER-UP}$ ⁷	1	1	$\mu\text{s typ}$	Power-Up Time from Full Power-Down

NOTES

¹Guaranteed by characterization. All input signals are specified with $t_r = t_f = 5\text{ ns}$ (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

²A Version timing specifications apply to the AD7477 S Version and AD7478 S Version; B Version timing specifications apply to the AD7476 S Version.

³3 V specifications apply from $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ for A Version; 3 V specifications apply from $V_{DD} = 2.35\text{ V to }3.6\text{ V}$ for B Version; 5 V specifications apply from $V_{DD} = 4.75\text{ V to }5.25\text{ V}$.

⁴Mark/Space ratio for the SCLK input is 40/60 to 60/40.

⁵Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.

⁶ t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8 , quoted in the Timing Specifications is the true bus relinquish time of the part and is independent of the bus loading.

⁷See Power-Up Time section.

Specifications subject to change without notice.

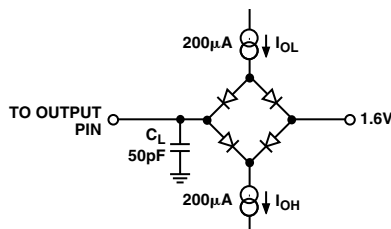


Figure 1. Load Circuit for Digital Output Timing Specifications

AD7476/AD7477/AD7478

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C, unless otherwise noted.)

V _{DD} to GND	-0.3 V to +7 V
Analog Input Voltage to GND	-0.3 V to V _{DD} + 0.3 V
Digital Input Voltage to GND	-0.3 V to +7 V
Digital Output Voltage to GND	-0.3 V to V _{DD} + 0.3 V
Input Current to Any Pin Except Supplies ²	±10 mA
Operating Temperature Range	
Commercial (A, B Versions)	-40°C to +85°C
Military (S Version)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

Junction Temperature	150°C
SOT-23 Package	
θ _{JA} Thermal Impedance	230°C/W
θ _{JC} Thermal Impedance	92°C/W
Lead Temperature, Soldering	
Reflow (10 sec to 30 sec)	235 (0/+5)°C
Pb-Free Temperature Soldering	
Reflow	255 (0/+5)°C
ESD	3.5 kV

NOTES

¹ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

² Transient currents of up to 100 mA will not cause SCR latch-up.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB) ¹	Package Option ²	Branding Information
AD7476ART-500RL7	-40°C to +85°C	±1 typ	RT-6	CEA
AD7476ART-REEL	-40°C to +85°C	±1 typ	RT-6	CEA
AD7476ART-REEL7	-40°C to +85°C	±1 typ	RT-6	CEA
AD7476ARTZ-500RL7 ³	-40°C to +85°C	±1 typ	RT-6	CEA
AD7476ARTZ-REEL ³	-40°C to +85°C	±1 typ	RT-6	CEA
AD7476ARTZ-REEL7 ³	-40°C to +85°C	±1 typ	RT-6	CEA
AD7476BRT-REEL	-40°C to +85°C	±1.5 max	RT-6	CEB
AD7476BRT-REEL7	-40°C to +85°C	±1.5 max	RT-6	CEB
AD7476BRTZ-REEL ³	-40°C to +85°C	±1.5 max	RT-6	CEB
AD7476BRTZ-REEL7 ³	-40°C to +85°C	±1.5 max	RT-6	CEB
AD7476SRT-500RL7	-55°C to +125°C	±1.5 max	RT-6	CES
AD7476SRT-R2	-55°C to +125°C	±1.5 max	RT-6	CES
AD7476SRT-REEL	-55°C to +125°C	±1.5 max	RT-6	CES
AD7476SRT-REEL7	-55°C to +125°C	±1.5 max	RT-6	CES
AD7476SRTZ-500RL7 ³	-55°C to +125°C	±1.5 max	RT-6	CES
AD7476SRTZ-R2 ³	-55°C to +125°C	±1.5 max	RT-6	CES
AD7476SRTZ-REEL ³	-55°C to +125°C	±1.5 max	RT-6	CES
AD7476SRTZ-REEL7 ³	-55°C to +125°C	±1.5 max	RT-6	CES
AD7477ART-500RL7	-40°C to +85°C	±1 max	RT-6	CFA
AD7477ART-REEL	-40°C to +85°C	±1 max	RT-6	CFA
AD7477ART-REEL7	-40°C to +85°C	±1 max	RT-6	CFA
AD7477SRT-500RL7	-55°C to +125°C	±1 max	RT-6	CFS
AD7477SRT-R2	-55°C to +125°C	±1 max	RT-6	CFS
AD7477SRT-REEL	-55°C to +125°C	±1 max	RT-6	CFS
AD7477SRT-REEL7	-55°C to +125°C	±1 max	RT-6	CFS
AD7478ART-500RL7	-40°C to +85°C	±0.5 max	RT-6	CJA
AD7478ART-REEL	-40°C to +85°C	±0.5 max	RT-6	CJA
AD7478ART-REEL7	-40°C to +85°C	±0.5 max	RT-6	CJA
AD7478SRT-500RL7	-55°C to +125°C	±0.5 max	RT-6	CJS
AD7478SRT-R2	-55°C to +125°C	±0.5 max	RT-6	CJS
AD7478SRT-REEL7	-55°C to +125°C	±0.5 max	RT-6	CJS
EVAL-AD7476CB ⁴			Evaluation Board	
EVAL-AD7477CB ⁴			Evaluation Board	
EVAL-CONTROL BRD ⁵			Control Board	

NOTES

¹Linearity Error here refers to integral linearity error.

²RT = SOT-23.

³Z = Pb free.

⁴This can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.

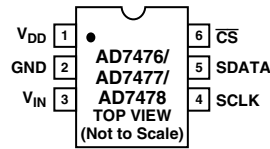
⁵This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. To order a complete evaluation kit, you need to order the particular ADC evaluation board, e.g., EVAL-AD7476CB, the EVAL-CONTROL BRD2, and a 12 V ac transformer. See relevant evaluation board application note for more information.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7476/AD7477/AD7478 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	V _{DD}	Power Supply Input. The V _{DD} range for the AD7476/AD7477/AD7478 is from 2.35 V to 5.25 V.
2	GND	Analog Ground. Ground reference point for all circuitry on the AD7476/AD7477/AD7478. All analog input signals should be referred to this GND voltage.
3	V _{IN}	Analog Input. Single-ended analog input channel. The input range is 0 V to V _{DD} .
4	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7476/AD7477/AD7478's conversion process.
5	SDATA	Data Out. Logic output. The conversion result from the AD7476/AD7477/AD7478 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7476 consists of four leading zeros followed by the 12 bits of conversion data, which is provided MSB first; the data stream from the AD7477 consists of four leading zeros followed by the 10 bits of conversion data, followed by two trailing zeros, which is also provided MSB first; the data stream from the AD7478 consists of four leading zeros followed by the eight bits of conversion data, followed by four trailing zeros, which is provided MSB first.
6	$\overline{\text{CS}}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7476/AD7477/AD7478 and framing the serial data transfer.

AD7476/AD7477/AD7478

TERMINOLOGY

Integral Nonlinearity

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. For the AD7476/AD7477, the endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition. For the AD7478, the endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal (i.e., AGND + 0.5 LSB). For the AD7478, this is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal (i.e., AGND + 1 LSB).

Gain Error

For the AD7476/AD7477, this is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., $V_{REF} - 1.5$ LSB) after the offset error has been adjusted out. For the AD7478, this is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., $V_{REF} - 1$ LSB) after the offset error has been adjusted.

Track-and-Hold Acquisition Time

The track-and-hold amplifier returns into track mode after the end of conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ± 0.5 LSB, after the end of conversion. See the Serial Interface Timing section for more detail.

Signal-to-(Noise + Distortion) Ratio

This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_s/2$), excluding dc.

The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$\text{Signal-to-(Noise + Distortion)} = (6.02N + 1.76) \text{ dB}$$

Thus for a 12-bit converter, this is 74 dB; for a 10-bit converter it is 62 dB; and for an 8-bit converter it is 50 dB.

Total Unadjusted Error

This is a comprehensive specification that includes gain error, linearity error, and offset error.

Total Harmonic Distortion (THD)

Total harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7476/AD7477/AD7478, it is defined as:

$$\text{THD (dB)} = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2 , V_3 , V_4 , V_5 , and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

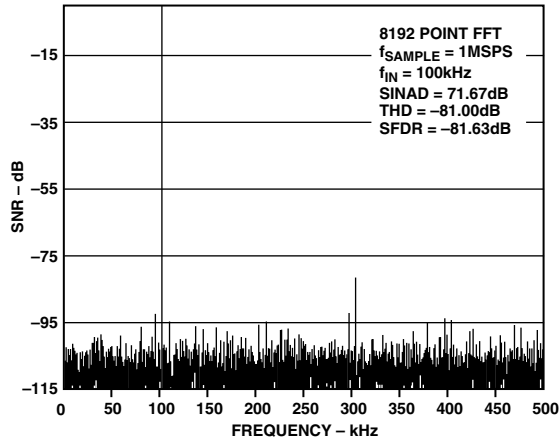
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_s/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

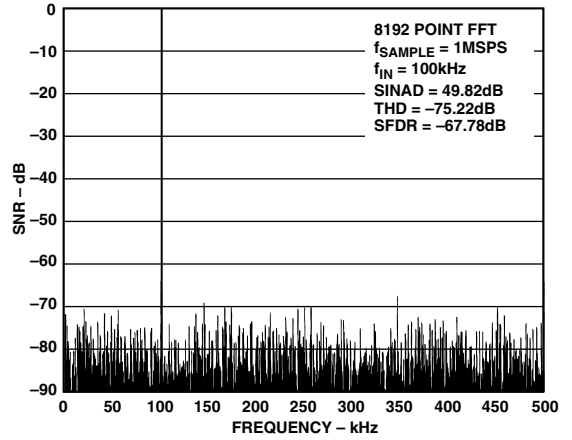
With inputs consisting of sine waves at two frequencies, f_a and f_b , any active device with nonlinearities will create distortion products at sum and difference frequencies of $m f_a \pm n f_b$ where $m, n = 0, 1, 2, 3$, and so on. Intermodulation distortion terms are those for which neither m nor n is equal to zero. For example, the second-order terms include $(f_a + f_b)$ and $(f_a - f_b)$, while the third-order terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$, and $(f_a - 2f_b)$.

The AD7476/AD7477/AD7478 are tested using the CCIF standard where two input frequencies are used, $f_a = 498.7$ kHz and $f_b = 508.7$ kHz. In this case, the second-order terms are usually distanced in frequency from the original sine waves while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals, expressed in dB.

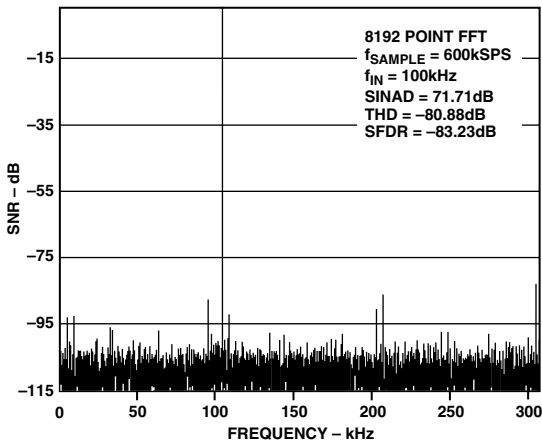
Typical Performance Characteristics—AD7476/AD7477/AD7478



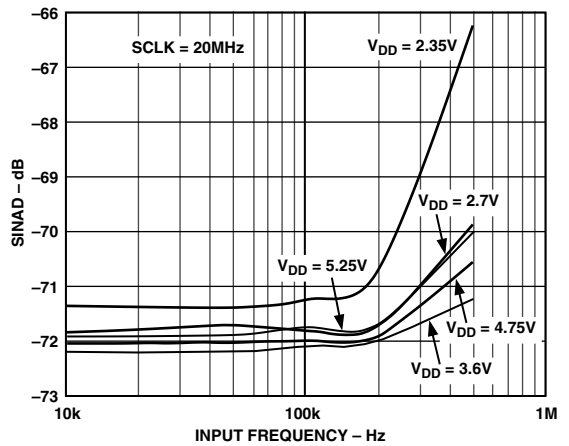
TPC 1. AD7476 Dynamic Performance at 1 MSPS



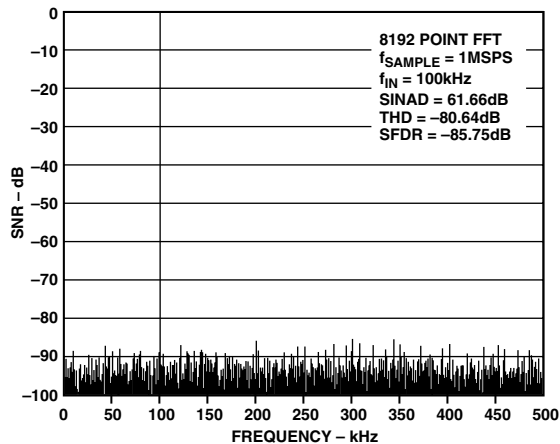
TPC 4. AD7478 Dynamic Performance at 1 MSPS



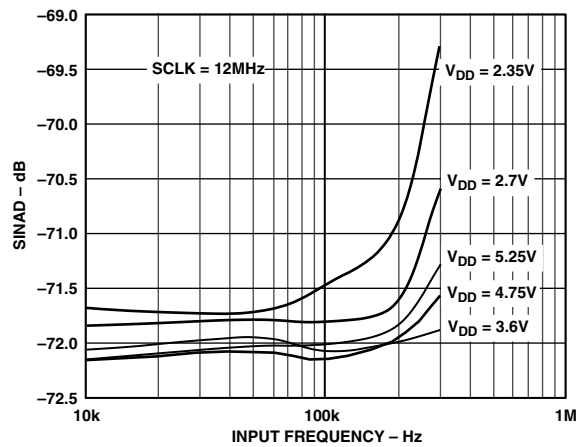
TPC 2. AD7476 Dynamic Performance at 600 kSPS



TPC 5. AD7476 SINAD vs. Input Frequency at 993 kSPS



TPC 3. AD7477 Dynamic Performance at 1 MSPS



TPC 6. AD7476 SINAD vs. Input Frequency at 605 kSPS

AD7476/AD7477/AD7478

CIRCUIT INFORMATION

The AD7476/AD7477/AD7478 are, respectively, 12-bit, 10-bit, and 8-bit, fast, micropower, single-supply ADCs. The parts can be operated from a 2.35 V to 5.25 V supply. When operated from either a 5 V supply or a 3 V supply, the AD7476/AD7477/AD7478 are capable of throughput rates of 1 MSPS when provided with a 20 MHz clock.

The AD7476/AD7477/AD7478 provide the user with an on-chip, track-and-hold ADC, and a serial interface housed in a tiny 6-lead SOT-23 package, which offers the user considerable space saving advantages over alternative solutions. The serial clock input accesses data from the part and also provides the clock source for the successive-approximation ADC. The analog input range is 0 V to V_{DD} . An external reference is not required for the ADC, nor is there a reference on-chip. The reference for the AD7476/AD7477/AD7478 is derived from the power supply and thus gives the widest dynamic input range.

The AD7476/AD7477/AD7478 also feature a power-down option to save power between conversions. The power-down feature is implemented across the standard serial interface as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7476/AD7477/AD7478 are successive-approximation analog-to-digital converters based around a charge redistribution DAC. Figures 2 and 3 show simplified schematics of the ADC. Figure 2 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on V_{IN} .

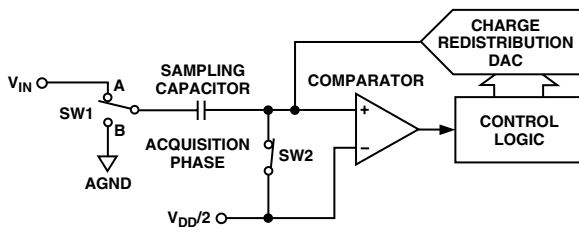


Figure 2. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 3), SW2 will open and SW1 will move to Position B, causing the comparator to become unbalanced. The Control Logic and the Charge Redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The Control Logic generates the ADC output code. Figures 4 and 5 show the ADC transfer function.

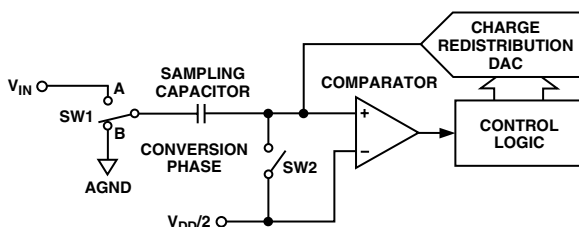


Figure 3. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7476/AD7477/AD7478 is straight binary. For the AD7476/AD7477, designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSB, and so on). The LSB size for the AD7476 is $V_{DD}/4096$ and the LSB size for the AD7477 is $V_{DD}/1024$. The ideal transfer characteristic for the AD7476/AD7477 is shown in Figure 4.

For the AD7478, designed code transitions occur midway between successive integer LSB values (i.e., 1 LSB, 2 LSB, and so on). The LSB size for the AD7478 is $V_{DD}/256$. The ideal transfer characteristic for the AD7478 is shown in Figure 5.

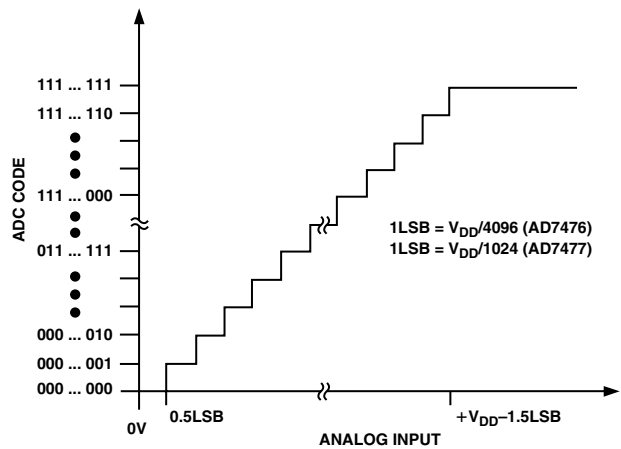


Figure 4. Transfer Characteristic for the AD7476/AD7477

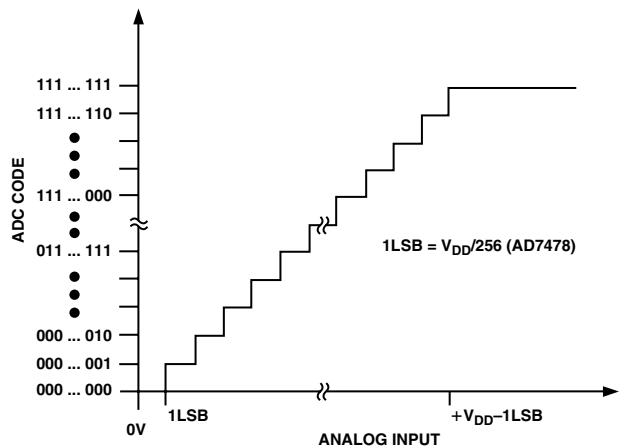


Figure 5. Transfer Characteristic for AD7478

TYPICAL CONNECTION DIAGRAM

Figure 6 shows a typical connection diagram for the AD7476/AD7477/AD7478. V_{REF} is taken internally from V_{DD} and as such, V_{DD} should be well decoupled. This provides an analog input range of 0 V to V_{DD} . The conversion result is output in a 16-bit word with four leading zeros followed by the MSB of the 12-bit, 10-bit, or 8-bit result. The 10-bit result from the AD7477 will be followed by two trailing zeros. The 8-bit result from the AD7478 will be followed by four trailing zeros.

Alternatively, because the supply current required by the AD7476/AD7477/AD7478 is so low, a precision reference can be used as the supply source to the AD7476/AD7477/AD7478. A REF19x voltage reference (REF195 for 5 V, or REF193 for 3 V) can be used to supply the required voltage to the ADC (see Figure 6). This configuration is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V or 3 V (e.g., 1.5 V). The REF19x will output a steady voltage to the AD7476/AD7477/AD7478. If the low dropout REF193 is used, the current it typically needs to supply to the AD7476/AD7477/AD7478 is 1 mA. When the ADC is converting at a rate of 1 MSPS, the REF193 will need to supply a maximum of 1.6 mA to the AD7476/AD7477/AD7478. The load regulation of the REF193 is typically 10 ppm/mA (REF193, $V_S = 5$ V), which results in an error of 16 ppm (48 μ V) for the 1.6 mA drawn from it. This corresponds to a 0.065 LSB error for the AD7476 with $V_{DD} = 3$ V from the REF193, a 0.016 LSB error for the AD7477, and a 0.004 LSB error for the AD7478. For applications where power consumption is of concern, the Power-Down mode of the ADC and the Sleep mode of the REF19x reference should be used to improve power performance. See the Modes of Operation section.

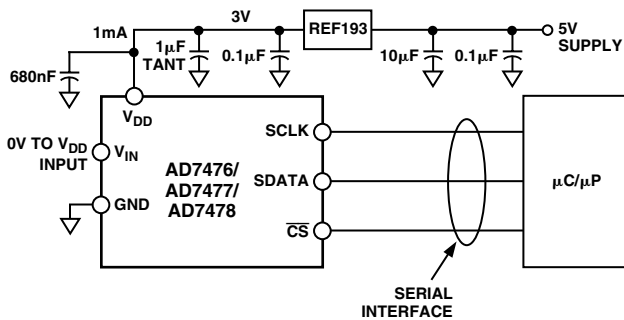


Figure 6. REF193 as Power Supply to AD7476/AD7477/AD7478

Table I provides some typical performance data with various references used as a V_{DD} source with a low frequency analog input. Under the same setup conditions, the references were compared and the AD780 proved the optimum reference.

Table I.

Reference Tied to V_{DD}	AD7476 SNR Performance 1 kHz Input (dB)
AD780 @ 3 V REF193	71.17 70.4
AD780 @ 2.5 V REF192 AD1582	71.35 70.93 70.05

Analog Input

Figure 7 shows an equivalent circuit of the analog input structure of the AD7476/AD7477/AD7478. The two diodes D1 and D2 provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 300 mV. This will cause these diodes to become forward-biased and start conducting current into

the substrate. These diodes can conduct a maximum of 10 mA without causing irreversible damage to the part. The capacitor C1 in Figure 7 is typically about 4 pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 100 Ω . The capacitor C2 is the ADC sampling capacitor and typically has a capacitance of 30 pF. For ac applications, removing high frequency components from the analog input signal is recommended by use of a band-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.

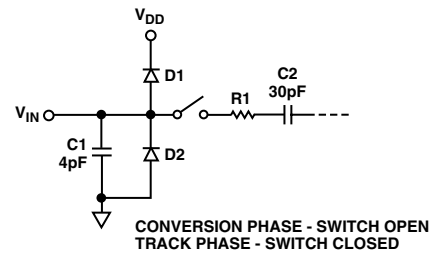


Figure 7. Equivalent Analog Input Circuit

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade. Figure 8 shows a graph of the total harmonic distortion versus source impedance for different analog input frequencies when using a supply voltage of 2.7 V and sampling at a rate of 605 kSPS. Figures 9 and 10 each show a graph of the total harmonic distortion versus analog input signal frequency for various supply voltages while sampling at 993 kSPS with an SCLK frequency of 20 MHz and 605 kSPS with an SCLK frequency of 12 MHz, respectively.

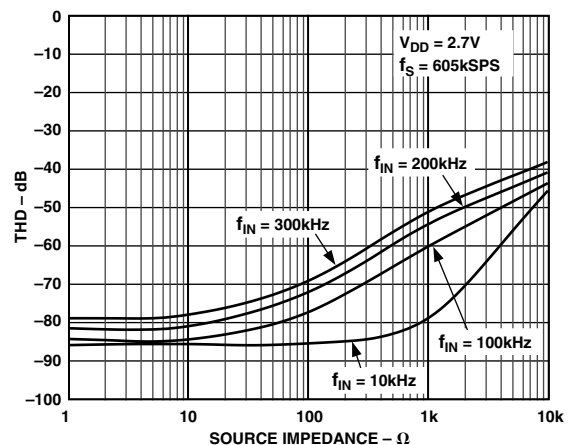


Figure 8. THD vs. Source Impedance for Various Analog Input Frequencies

AD7476/AD7477/AD7478

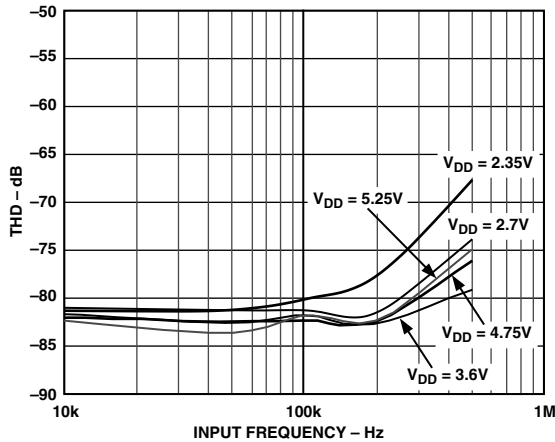


Figure 9. THD vs. Analog Input Frequency, $f_s = 993$ kSPS

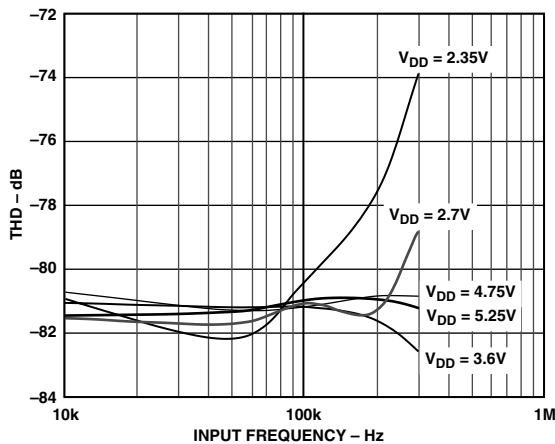


Figure 10. THD vs. Analog Input Frequency, $f_s = 605$ kSPS

Digital Inputs

The digital inputs applied to the AD7476/AD7477/AD7478 are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs applied can go to 7 V and are not

restricted by the $V_{DD} + 0.3$ V limit as on the analog inputs. For example, if the AD7476/AD7477/AD7478 were operated with a V_{DD} of 3 V, then 5 V logic levels could be used on the digital inputs. However, it is important to note that the data output on SDATA will still have 3 V logic levels when $V_{DD} = 3$ V. Another advantage of SCLK and \overline{CS} not being restricted by the $V_{DD} + 0.3$ V limit is the fact that power supply sequencing issues are avoided. If \overline{CS} or SCLK is applied before V_{DD} , there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V was applied prior to V_{DD} .

MODES OF OPERATION

The mode of operation of the AD7476/AD7477/AD7478 is selected by controlling the (logic) state of the \overline{CS} signal during a conversion. There are two possible modes of operation, Normal mode and Power-Down mode. The point at which \overline{CS} is pulled high after the conversion has been initiated will determine whether or not the AD7476/AD7477/AD7478 will enter Power-Down mode. Similarly, if already in power-down, \overline{CS} can control whether the device will return to normal operation or remain in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for different application requirements.

Normal Mode

This mode is intended for fastest throughput rate performance, as the user does not have to worry about any power-up times with the AD7476/AD7477/AD7478 remaining fully powered all the time. Figure 11 shows the general diagram of the operation of the AD7476/AD7477/AD7478 in this mode.

The conversion is initiated on the falling edge of \overline{CS} as described in the Serial Interface section. To ensure the part remains fully powered up at all times, \overline{CS} must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of \overline{CS} . If \overline{CS} is brought high any time after the tenth SCLK falling edge, but before the sixteenth SCLK falling edge, the part will remain powered up but the conversion will be terminated and SDATA will go back into three-state. Sixteen serial clock cycles are required to complete the conversion and access the complete

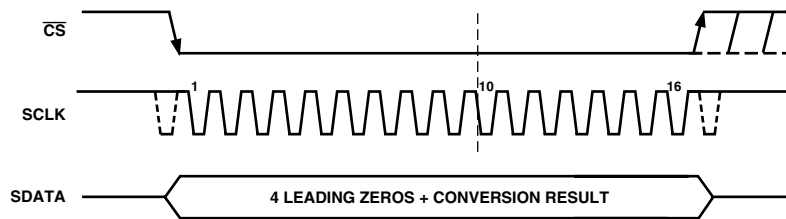


Figure 11. Normal Mode Operation

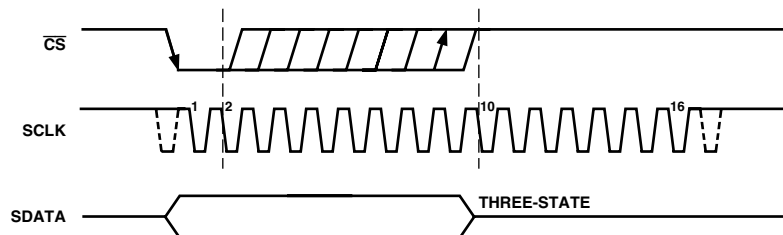


Figure 12. Entering Power-Down Mode

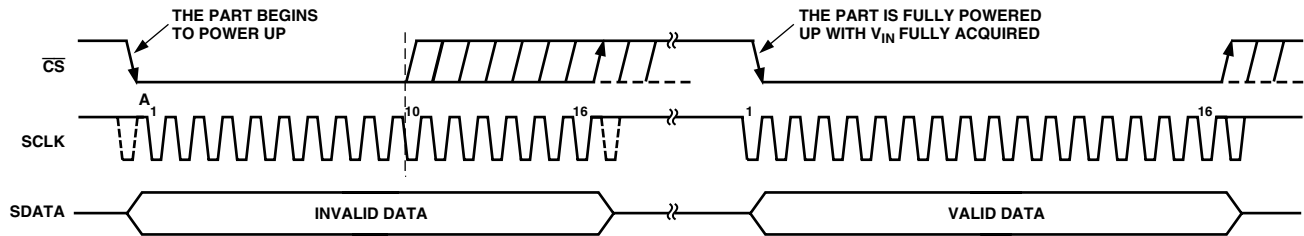


Figure 13. Exiting Power-Down Mode

conversion result. \overline{CS} may idle high until the next conversion or may idle low until \overline{CS} returns high sometime prior to the next conversion (effectively idling \overline{CS} low).

Once a data transfer is complete (SDATA has returned to three-state), another conversion can be initiated after the quiet time, t_{QUIET} , has elapsed by again bringing \overline{CS} low.

Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and the ADC is then powered down for a relatively long duration between these bursts of several conversions. When the AD7476/AD7477/AD7478 is in power-down, all analog circuitry is powered down.

To enter power-down, the conversion process must be interrupted by bringing \overline{CS} high any time after the second falling edge of SCLK and before the tenth falling edge of SCLK, as shown in Figure 12. Once \overline{CS} has been brought high in this window of SCLKs, the part will enter power-down and the conversion that was initiated by the falling edge of \overline{CS} will be terminated and SDATA will go back into three-state. If \overline{CS} is brought high before the second SCLK falling edge, the part will remain in Normal mode and will not power down. This will avoid accidental power-down due to glitches on the \overline{CS} line.

To exit this mode of operation and power up the AD7476/AD7477/AD7478 again, a dummy conversion is performed. On the falling edge of \overline{CS} , the device will begin to power up, and will continue to power up as long as \overline{CS} is held low until after the falling edge of the tenth SCLK. The device will be fully powered up once 16 SCLKs have elapsed and, as shown in Figure 13, valid data will result from the next conversion. If \overline{CS} is brought high before the tenth falling edge of SCLK, the AD7476/AD7477/AD7478 will again go back into power-down. This avoids accidental power-up due to glitches on the \overline{CS} line or an inadvertent burst of eight SCLK cycles while \overline{CS} is low. So although the device may begin to power up on the falling edge of \overline{CS} , it will again power down on the rising edge of \overline{CS} as long as it occurs before the tenth SCLK falling edge.

Power-Up Time

The power-up time of the AD7476/AD7477/AD7478 is typically 1 μs , which means that with any frequency of SCLK up to 20 MHz, one dummy cycle will always be sufficient to allow the device to power up. Once the dummy cycle is complete, the ADC will be fully powered up and the input signal will be acquired properly. The quiet time (t_{QUIET}) must still be allowed from the point at which the bus goes back into three-state after the dummy

conversion, to the next falling edge of \overline{CS} . When running at 1 MSPS throughput rate, the AD7476/AD7477/AD7478 will power up and acquire a signal within ± 0.5 LSB in one dummy cycle, i.e., 1 μs .

When powering up from the Power-Down mode with a dummy cycle, as in Figure 13, the track-and-hold that was in Hold mode while the part was powered down returns to Track mode after the first SCLK edge the part receives after the falling edge of \overline{CS} . This is shown as Point A in Figure 13. Although at any SCLK frequency one dummy cycle is sufficient to power up the device and acquire V_{IN} , it does not necessarily mean that a full dummy cycle of 16 SCLKs must always elapse to power up the device and fully acquire V_{IN} ; 1 μs will be sufficient to power up the device and acquire the input signal. If, for example, a 5 MHz SCLK frequency were applied to the ADC, the cycle time would be 3.2 μs . In one dummy cycle, 3.2 μs , the part would be powered up and V_{IN} fully acquired. However, after 1 μs with a 5 MHz SCLK, only five SCLK cycles would have elapsed. At this stage, the ADC would be fully powered up and the signal acquired. So, in this case, the \overline{CS} can be brought high after the tenth SCLK falling edge and brought low again after a time t_{QUIET} to initiate the conversion.

When power supplies are first applied to the AD7476/AD7477/AD7478, the ADC may power up in either Power-Down mode or Normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure the part is fully powered up before attempting a valid conversion. Likewise, if it is intended to keep the part in the Power-Down mode while not in use and the user wants the part to power up in Power-Down mode, the dummy cycle may be used to ensure the device is in power-down by executing a cycle such as that shown in Figure 12. Once supplies are applied to the AD7476/AD7477/AD7478, the power-up time is the same as that when powering up from the Power-Down mode. It takes approximately 1 μs to fully power up if the part powers up in Normal mode. It is not necessary to wait 1 μs before executing a dummy cycle to ensure the desired mode of operation. Instead, the dummy cycle can occur directly after power is supplied to the ADC. If the first valid conversion is then performed directly after the dummy conversion, care must be taken to ensure that adequate acquisition time has been allowed. As mentioned earlier, when powering up from the Power-Down mode, the part will return to track upon the first SCLK edge applied after the falling edge of \overline{CS} . However, when the ADC powers up initially after supplies are applied, the track-and-hold will already be in track. This means that if the ADC powers up in the desired mode of operation, and a dummy cycle is not required to change mode, then a dummy cycle is not required to place the track-and-hold into track.

AD7476/AD7477/AD7478

POWER VS. THROUGHPUT RATE

By using the Power-Down mode on the AD7476/AD7477/AD7478 when not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 14 shows how as the throughput rate is reduced, the device remains in its power-down state longer, and the average power consumption over time drops accordingly.

For example, if the AD7476/AD7477/AD7478 is operated in a continuous sampling mode with a throughput rate of 100 kSPS and a SCLK of 20 MHz ($V_{DD} = 5\text{ V}$), and the device is placed in the Power-Down mode between conversions, then the power consumption is calculated as follows. The power dissipation during normal operation is 17.5 mW ($V_{DD} = 5\text{ V}$). If the power-up time is one dummy cycle, i.e., 1 μs , and the remaining conversion time is another cycle, i.e., 1 μs , then the AD7476/AD7477/AD7478 can be said to dissipate 17.5 mW for 2 μs during each conversion cycle. If the throughput rate is 100 kSPS, the cycle time is 10 μs and the average power dissipated during each cycle is $(2/10) \times (17.5\text{ mW}) = 3.5\text{ mW}$. If $V_{DD} = 3\text{ V}$, SCLK = 20 MHz, and the device is again in Power-Down mode between conversions, the power dissipation during normal operation is 4.8 mW. The AD7476/AD7477/AD7478 can now be said to dissipate 4.8 mW for 2 μs during each conversion cycle. With a throughput rate of 100 kSPS, the average power dissipated during each cycle is $(2/10) \times (4.8\text{ mW}) = 0.96\text{ mW}$. Figure 14 shows the power versus throughput rate when using the Power-Down mode between conversions with both 5 V and 3 V supplies.

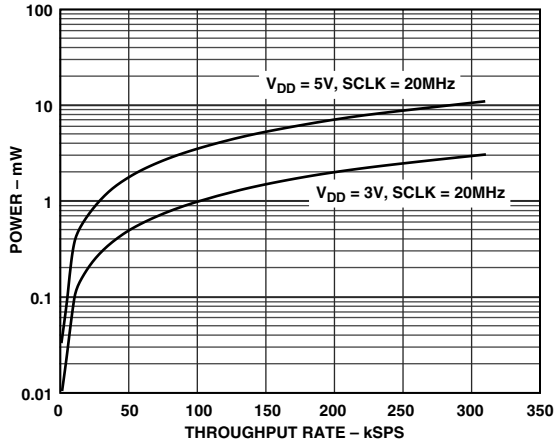


Figure 14. Power vs. Throughput Rate

The Power-Down mode is intended for use with throughput rates of approximately 333 kSPS and under, because at higher sampling rates power is not saved by using the Power-Down mode.

SERIAL INTERFACE

Figures 15, 16, and 17 show the detailed timing diagrams for serial interfacing to the AD7476, AD7477, and AD7478, respectively. The serial clock provides the conversion clock and also controls the transfer of information from the AD7476/AD7477/AD7478 during conversion.

The $\overline{\text{CS}}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{\text{CS}}$ puts the track-and-hold into Hold mode, takes the bus out of three-state, and the analog input is sampled at this point. The conversion is also initiated at this point and will require sixteenth SCLK cycles to complete. Once 13 SCLK falling edges have elapsed, the track-and-hold will go back into track on the next SCLK rising edge as shown in Figures 15, 16, and 17 at Point B. On the sixteenth SCLK falling edge, the SDATA line will go back into three-state. If the rising edge of $\overline{\text{CS}}$ occurs before 16 SCLKs have elapsed, the conversion will be terminated and the SDATA line will go back into three-state; otherwise, SDATA returns to three-state on the sixteenth SCLK falling edge as shown in Figures 15, 16, and 17. Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7476/AD7477/AD7478. $\overline{\text{CS}}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with the second leading zero. Thus the first falling clock edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. The final bit in the data transfer is valid on the sixteenth falling edge, having been clocked out on the previous (fifteenth) falling edge. In applications with a slower SCLK, it is possible to read in data on each SCLK rising edge, i.e., although the first leading zero will have to be read on the first SCLK falling edge after the $\overline{\text{CS}}$ falling edge. Therefore, the first rising edge of SCLK after the $\overline{\text{CS}}$ falling edge will provide the second leading zero and the fifteenth rising SCLK edge will have DB0 provided or the final zero for the AD7477 and AD7478. This may not work with most microcontrollers/DSPs, but could possibly be used with FPGAs and ASICs.

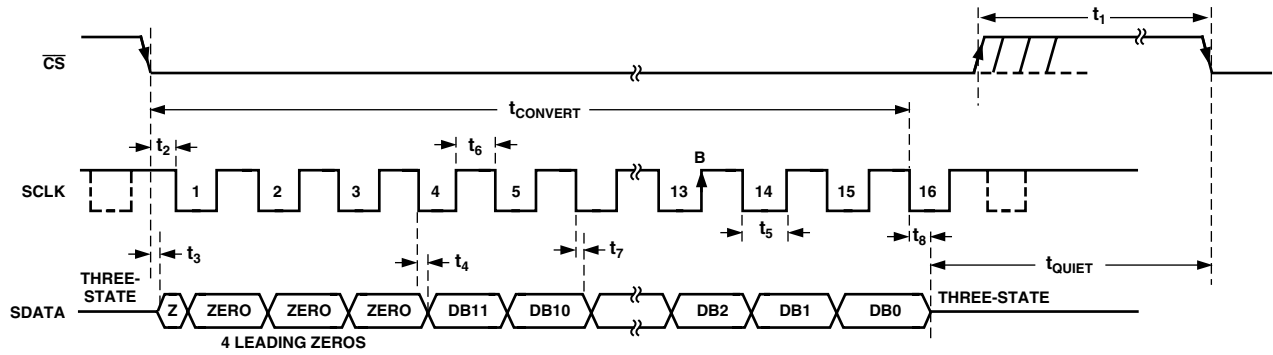


Figure 15. AD7476 Serial Interface Timing Diagram

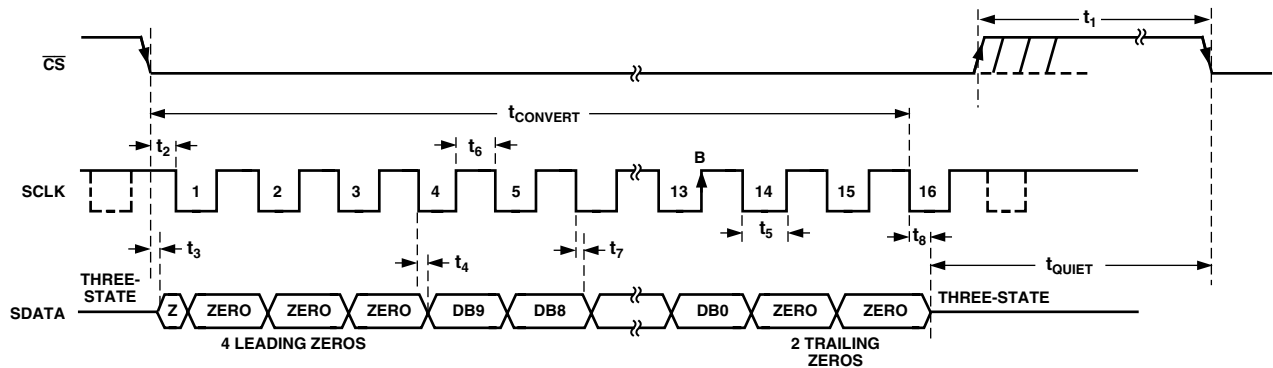


Figure 16. AD7477 Serial Interface Timing Diagram

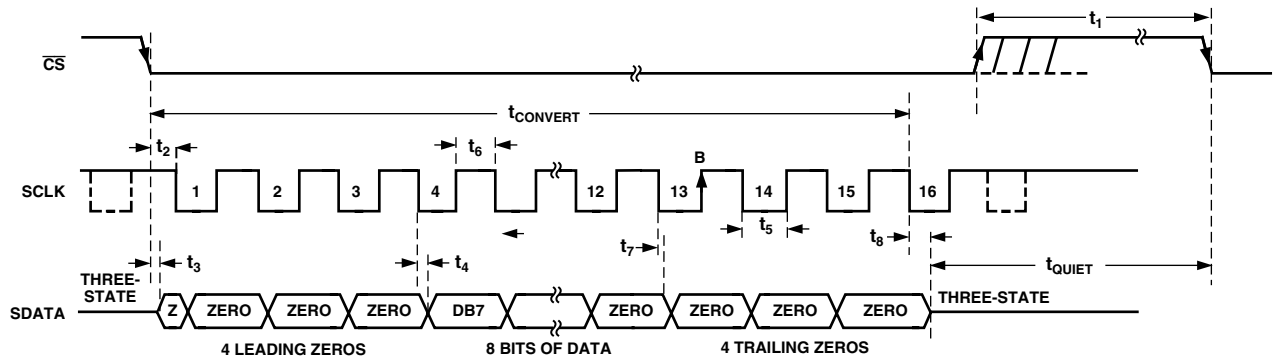


Figure 17. AD7478 Serial Interface Timing Diagram

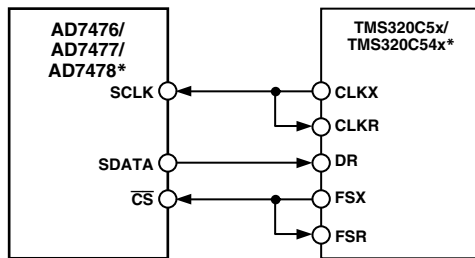
AD7476/AD7477/AD7478

MICROPROCESSOR INTERFACING

The serial interface on the AD7476/AD7477/AD7478 allows the part to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7476/AD7477/AD7478 with some of the more common microcontroller and DSP serial interface protocols.

AD7476/AD7477/AD7478 to TMS320C5x/C54x Interface

The serial interface on the TMS320C5x uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7476/AD7477/AD7478. The CS input allows easy interfacing between the TMS320C5x/C54x and the AD7476/AD7477/AD7478 without any glue logic required. The serial port of the TMS320C5x/C54x is set up to operate in burst mode with internal CLKX (Tx serial clock) and FSX (Tx frame sync). The serial port control register (SPC) must have the following setup: FO = 0, FSM = 1, MCM = 1, and TXM = 1. The format bit, FO, may be set to 1 to set the word length to eight bits, in order to implement the Power-Down mode on the AD7476/AD7477/AD7478. The connection diagram is shown in Figure 18. It should be noted that for signal processing applications, it is imperative that the frame synchronization signal from the TMS320C5x/C54x provides equidistant sampling.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 18. Interfacing to the TMS320C5x/C54x

AD7476/AD7477/AD7478 to ADSP-21xx Interface

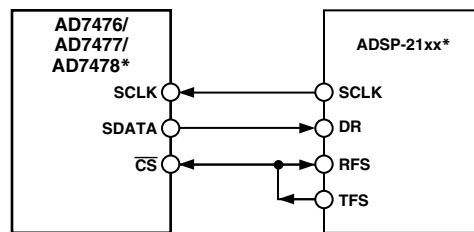
The ADSP-21xx family of DSPs are interfaced directly to the AD7476/AD7477/AD7478 without any glue logic required. The SPORT control register should be set up as follows:

- TFSW = RFSW = 1, Alternate Framing
- INVRFS = INVTFS = 1, Active Low Frame Signal
- DTYPE = 00, Right Justify Data
- SLEN = 1111, 16-Bit Data-Words
- ISCLK = 1, Internal Serial Clock
- TFSR = RFSR = 1, Frame Every Word
- IRFS = 0
- ITFS = 1

To implement the Power-Down mode, SLEN should be set to 0111 to issue an 8-bit SCLK burst. The connection diagram is shown in Figure 19. The ADSP-21xx has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in Alternate Framing mode and the SPORT control register is set up as described. The frame synchronization signal generated on the TFS is tied to CS and as with all signal processing applications, equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and, under certain conditions, equidistant sampling may not be achieved.

The timer registers, for example, are loaded with a value that will provide an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and therefore the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given (i.e., TX0 = AX0), the state of the SCLK is checked. The DSP will wait until the SCLK has gone high, low, and high before transmission will start. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, the data may be transmitted, or it may wait until the next clock edge.

For example, the ADSP-2111 has a master clock frequency of 16 MHz. If the SCLKDIV register is loaded with the value 3, a SCLK of 2 MHz is obtained, and eight master clock periods will elapse for every one SCLK period. If the timer registers are loaded with the value 803, 100.5 SCLKs will occur between interrupts and subsequently between transmit instructions. This situation will result in nonequidistant sampling as the transmit instruction is occurring on an SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N, equidistant sampling will be implemented by the DSP.

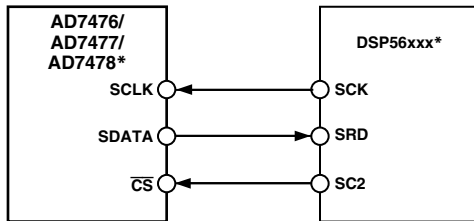


*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 19. Interfacing to the ADSP-21xx

AD7476/AD7477/AD7478 to DSP56xxx Interface

The connection diagram in Figure 20 shows how the AD7476/AD7477/AD7478 can be connected to the SSI (Synchronous Serial Interface) of the DSP56xxx family of DSPs from Motorola. The SSI is operated in Synchronous Mode (SYN bit in CRB = 1) with internally generated word frame sync for both Tx and Rx (Bits FSL1 = 0 and FSL0 = 0 in CRB). Set the word length to 16 by setting bits WL1 = 1 and WL0 = 0 in CRA. To implement the Power-Down mode on the AD7476/AD7477/AD7478, the word length can be changed to eight bits by setting bits WL1 = 0 and WL0 = 0 in CRA. It should be noted that for signal processing applications, it is imperative that the frame synchronization signal from the DSP56xxx provides equidistant sampling.

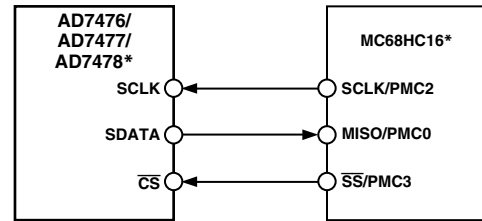


*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 20. Interfacing to the DSP56xxx

AD7476/AD7477/AD7478 to MC68HC16 Interface

The Serial Peripheral Interface (SPI) on the MC68HC16 is configured for Master Mode (MSTR = 1), the Clock Polarity Bit (CPOL) = 1, and the Clock Phase Bit (CPHA) = 0. The SPI is configured by writing to the SPI Control Register (SPCR)—see the *68HC16 User Manual*. The serial transfer will take place as a 16-bit operation when the SIZE bit in the SPCR register is set to SIZE = 1. To implement the Power-Down mode with an 8-bit transfer, set SIZE = 0. A connection diagram is shown in Figure 21.



*ADDITIONAL PINS OMITTED FOR CLARITY

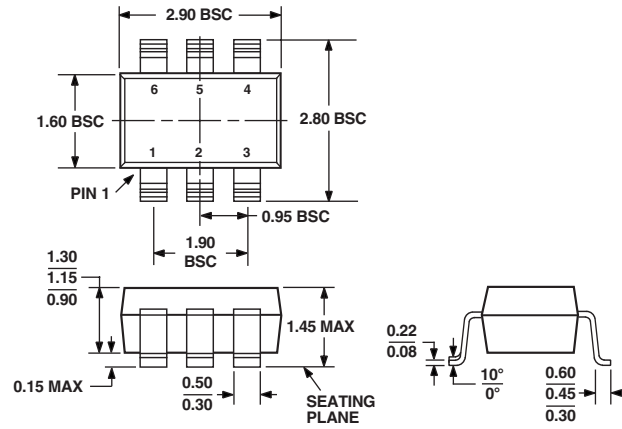
Figure 21. Interfacing to the MC68HC16

AD7476/AD7477/AD7478

OUTLINE DIMENSIONS

6-Lead Plastic Surface-Mount Package [SOT-23] (RT-6)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178AB

Revision History

Location	Page
3/04—Data Sheet changed from REV. C to REV. D.	
Added U.S. Patent number	1
Changes to SPECIFICATIONS	2
Changes to ABSOLUTE MAXIMUM RATINGS	6
Changes to AD7476/AD7477/AD7478 to ADSP-21xx Interface section	16
2/03—Data Sheet changed from REV. B to REV. C.	
Change to GENERAL DESCRIPTION	1
Changes to SPECIFICATIONS	2
Changes to ABSOLUTE MAXIMUM RATINGS	6
Change to ORDERING GUIDE	6
Change to TYPICAL CONNECTION DIAGRAM SECTION	10
Change to Figure 8 caption	11
Change to Figure 19	16
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