TLE 6710

Airbag
Combined Power-Supply and Firing Circuit

Datasheet

Version B **May 04, 2001**

Table of Content:

Combined Power-Supply and Firing Circuit for Airbag Applications

A. Features

- Step up converter 30V (Boost Converter) with a maximum duty cycle of 90% and a 700mA minimum current limitation of the power transistor
- Step down converter 5V (Buck Converter)
  Improvement of the efficiency of the buck converter by external supply (EVZ2)
- Four independent firing squib drivers
- Highside and lowside switch for each firing circuit
  Firing current limitation to maximum 3.25A for each firing circuit
- Digital output for firing current detection of minimum 1.75A for two squib drivers
- Squib resistance measurement with analogue outputs
- Switchable gain factor (10 or 30) for an improved accuracy of the squib resistance measurement
- Programmable squib leakage measurement to ground or to battery supply with digital outputs
- Several supply voltage measurements on external pins
- Digital output for detection of safing sensor closure
- Watch dog circuit
- Precise 100kHz oscillator
- Power on/off reset generator
- Serial interface line driver (ISO 9141 and TTL-level)
- Four voltage/current sources for diagnostic purposes
- Diagnostic lamp driver
- Diagnostic driver for inductive loads or lamps
- Serial peripheral interface (SPI) for direct driving from a micro controller
- Logic and analogue output signals for direct sensing and diagnostics by a µC
- Package P-MQFP-64-1

Type	Ordering Code	Package
TLE 6710	on request	P-MQFP-64-1

B. Circuit Description

A description of each section of the IC is given below with the representative block diagram and the application circuit.

Supply and Reference:

Internal supply and biasing of the sections is provided by a supply module which is driven by voltage EVZ of the boost converter (30V) . During start up, EVZ is charged by the battery voltage UBATT via external inductance and diode. The voltage reference is based on a temperature-compensated bandgap circuit and has an accuracy of ± 1% at room temperature.

Low Battery Detection on pin UBATT:

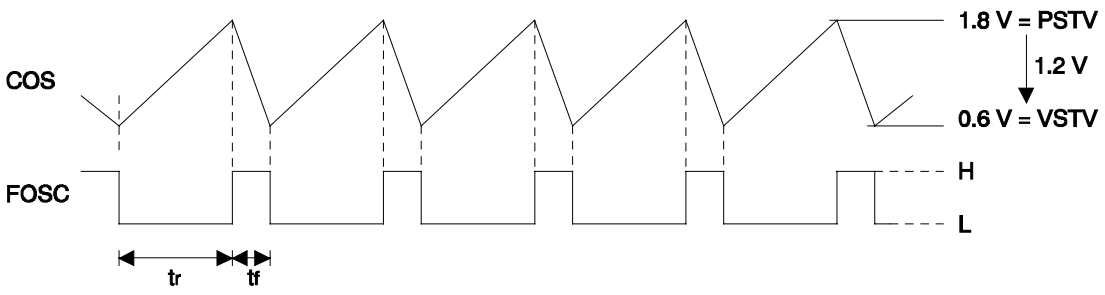
A comparator has been incorporated to guarantee that the modules i.e. reference voltage, internal supply and 100kHz-oscillator, are fully functional before the boost converter (30V) and the logic output AUSP are enabled. It prevents the possibility of start up glitches. The internal reference voltage is monitored by a comparator which disables the output stage AUSP when the voltage on input pin UBATT drops below 5V. To prevent erratic output switching as the threshold is crossed, 200mV of hysteresis is provided.

Oscillator for Boost (30V)-, Buck (5V)-Converter and Watchdog:

The oscillator frequency is externally programmed to 100kHz by the capacitor COS = 1nF on pin COS and a current source determined by the fixed resistor ROS = 5 kΩ on the pin ROS. The nominal voltage value on pin ROS is 1.2V.

Current calculation: $$I_{ROS} = \frac{1.2\ V}{5\ k\Omega} = 240\ \mu A$$

The charge to discharge ratio is controlled to yield a 90 % maximum duty cycle at the switch output of the boost converter (30V). During the discharge of COS, the oscillator generates an internal blanking pulse (FOSC) to disable the switch output of the boost converter (30V) and to enable the switch output of the buck converter (5V) as well as to provide a clock signal to the watchdog function. The nominal peak and valley saw tooth thresholds of the oscillator are VSTV = 0.6V and PSTV = 1.8V respectively.



Calculation formulas:

Capacitor charge current: $$I_{COSc} = \frac{7}{12} \times I_{ROS} = \frac{7}{12} \times \frac{V_{ROS}}{R_{ROS}} = 140\,\mu A$$

Capacitor discharge current: $$I_{COSd} = -\frac{7}{2} \times I_{ROS} = -\frac{7}{2} \times \frac{V_{ROS}}{R_{ROS}} = 840\,\mu A$$

Peak to peak voltage on pin COS: $$V_{COSpp} = V_{ROS} = 1.2\ V$$

Saw tooth rise time: $$t_r = \frac{V_{COSpp} \times C_{COS}}{I_{COSc}} = \frac{12}{7} \times R_{ROS} \times C_{COS}$$

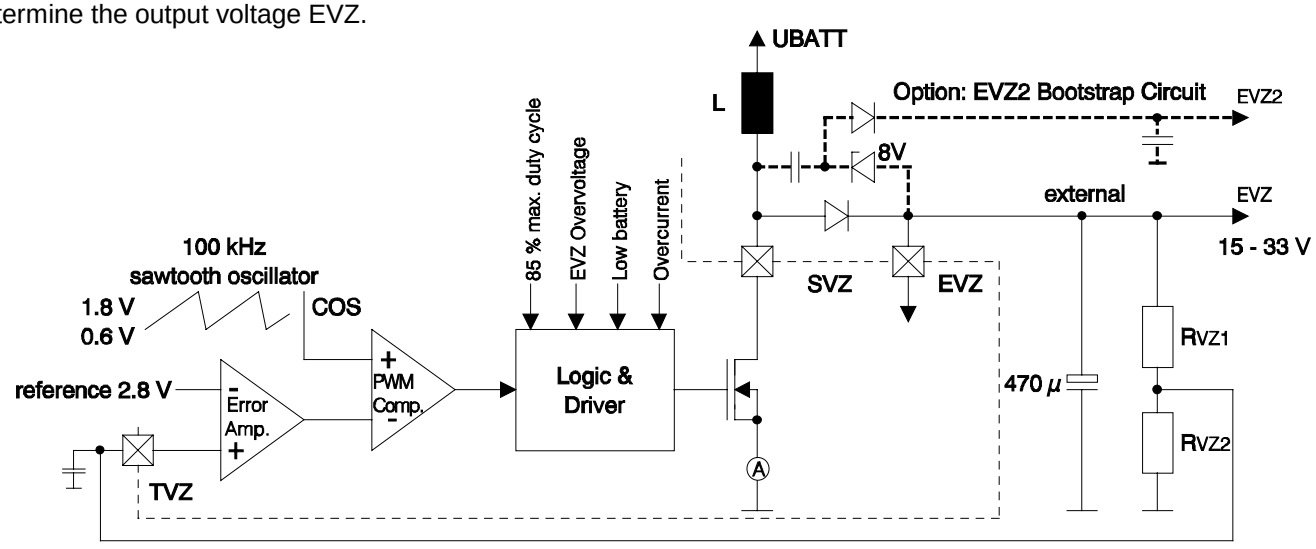
Saw tooth fall time: $$t_f = \frac{V_{COSpp} \times C_{COS}}{I_{COSd}} = \frac{2}{7} \times R_{ROS} \times C_{COS}$$

Oscillator frequency calculation: $$f_{OS} = \frac{1}{t_r + t_f} + f_{offset} \pm 5\% = \frac{1}{2 \times C_{COS} \times R_{ROS}} + f_{offset} \pm 5\%$$

f_{offset} ...Frequency offset of the PCB depending on the layout of each application.

Boost Converter (30V):

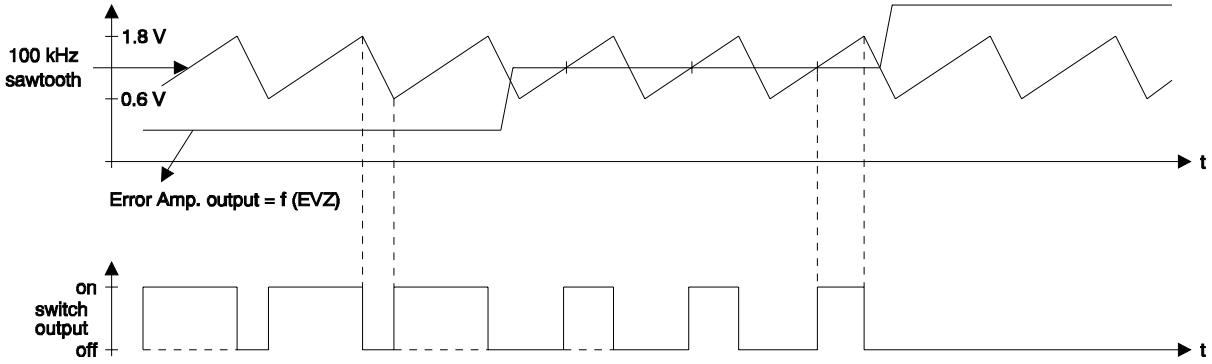
A boost converter generates a supply voltage for the airbag firing system, adjustable via external resistors between 15V and 33V. An inductance L is PWM-switched by an integrated current limited DMOS-power-transistor with a frequency of 100kHz. The reference section provides a 2.8V voltage for the regulation loop. An error amplifier compares the reference voltage with the feedback signal TVZ, which comes from an external divider network used to determine the output voltage EVZ.



Application note for programming the output voltage on pin EVZ:

$$V_{EVZ} = 2.8V \times \frac{R_{VZ1} + R_{VZ2}}{R_{VZ2}}$$

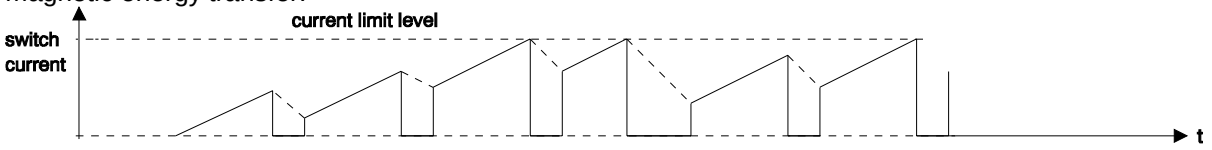
With a PWM comparator, the output of the error amplifier is then compared with a periodic linear ramp provided by the saw tooth signal of the oscillator. A logic signal with variable pulse width is generated, which passes through logic and driver circuits to the power switching FET. A duty cycle of typ. 86 % is determined by the duration of the falling ramp of the saw tooth oscillator.



The output transistor conduction is suppressed immediately if the current through the power FET exceeds typ. 800mA, low battery voltage or overvoltage on pin EVZ is detected. In case of short spikes, the logic circuit inhibits multiple pulses during one oscillating period.

Warning: A short from EVZ to ground can damage the external diode or the inductance, due to non existing overcurrent limitation in that path. The output transistor is designed to switch a maximum of 40V, with a drain current limitation of typically 800mA.

During start up, EVZ is charged by the battery voltage UBATT via external inductance and diode, so the voltage on pin EVZ is too low and the PWM-comparator requires a duty cycle of more than 85 %. Due to an increasing inductance current after several periods, the overcurrent sensor becomes active and reduces the maximum duty cycle to improve magnetic energy transfer.



NOTE: The pin GNDC chip internally is separated from the analog ground GNDB. On PCB these pins need to be connected for standard applications. If a boost converter application with higher power capability is needed, the pin GNDC can drive the gate of an external logic level power FET. The maximum output voltage on pin GNDC will be 7.5V (0mA) and minimum 5.5V driving 10mA. An external overcurrent detection circuit should switch off the external power FET and lead to a current spike on pin GNDC (900mA) to shut down the boost converter output driver stage of the TLE 6710.

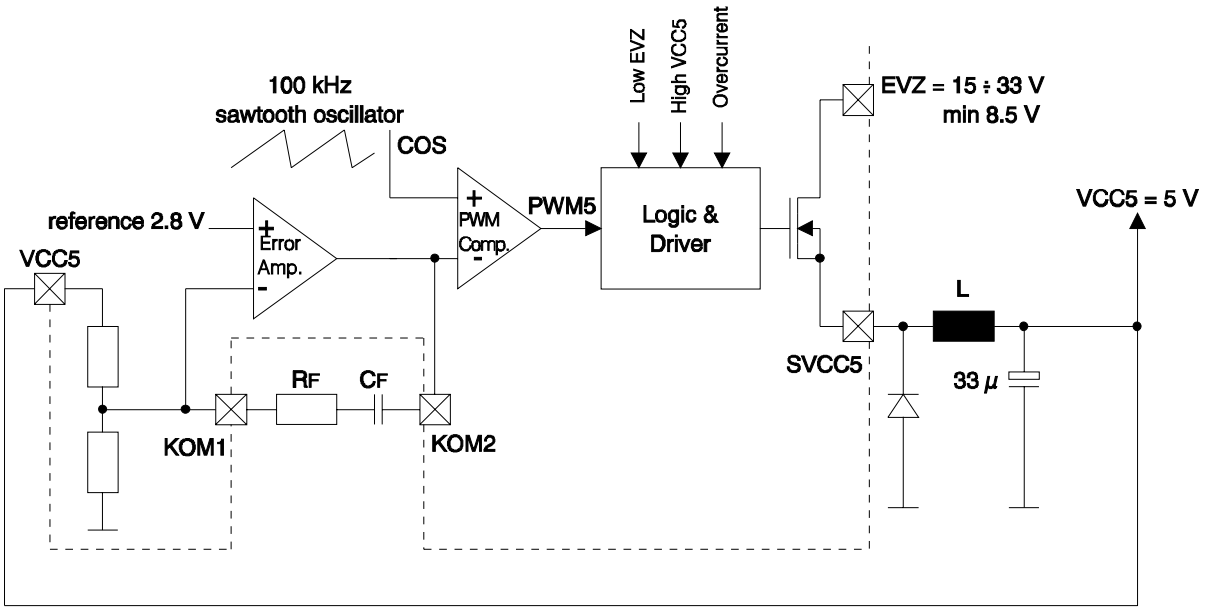
Buck Converter (5 V):

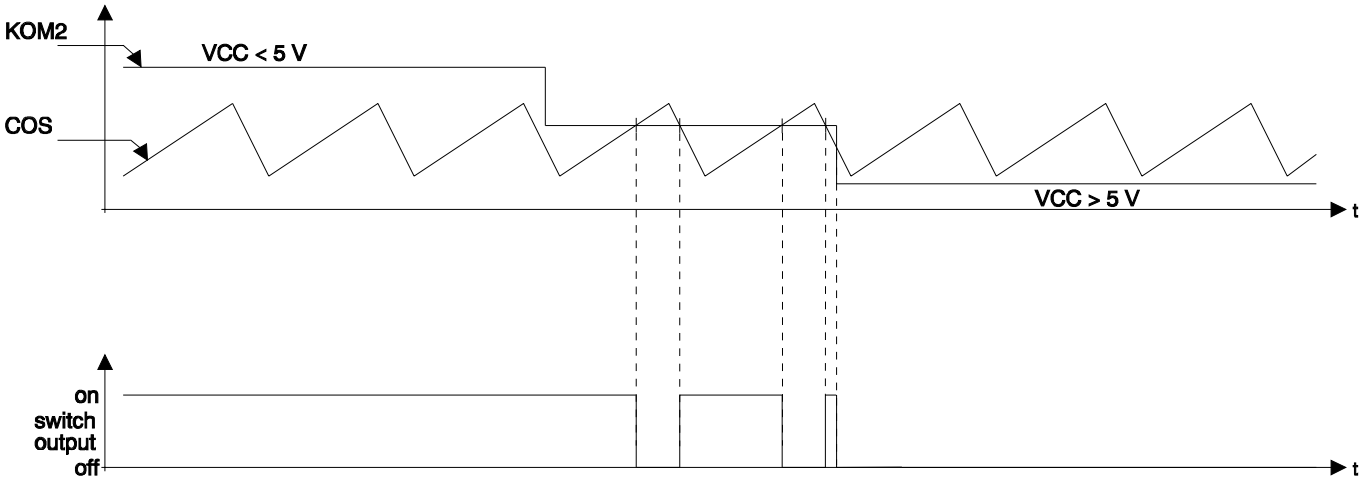
A stabilised 5V-supply for general purpose in the airbag system is realised by a buck converter. An external inductance L is PWM switched with a frequency of 100kHz via a high side DMOS-power transistor. The regulator module is supplied by the boost converter output (15-33V), and uses the stored energy of the boost converter capacitor if battery power-down occurs.

The basis for the regulation loop is a temperature compensated 2.8V bandgap reference voltage, generated in the reference section and linked to the non inverting input of the ‘Error Amplifier’ with a high voltage gain (> 60dB). The reference voltage is compared with the internally divided output voltage VCC5.

External loop compensation is required for converter stability, and is formed by connecting a series resistor-capacitor (R_F, C_F) between pins KOM1 and KOM2. The simplest way to optimise the compensation network is to observe the response of the output voltage VCC5 to a step load change, while adjusting R_F and C_F for critical damping. The final circuit should be verified for stability under four boundary conditions. These conditions are minimum input voltages, with minimum and maximum loads.

The error amplifier output is applied to the inverting input of the 'Pulse Width Modulator' (PWM) and is compared with the oscillator ramp voltage COS. Output switch conduction is initiated when the error amplifier output voltage exceeds the sawtooth peak voltage, due to less VCC5 voltage.

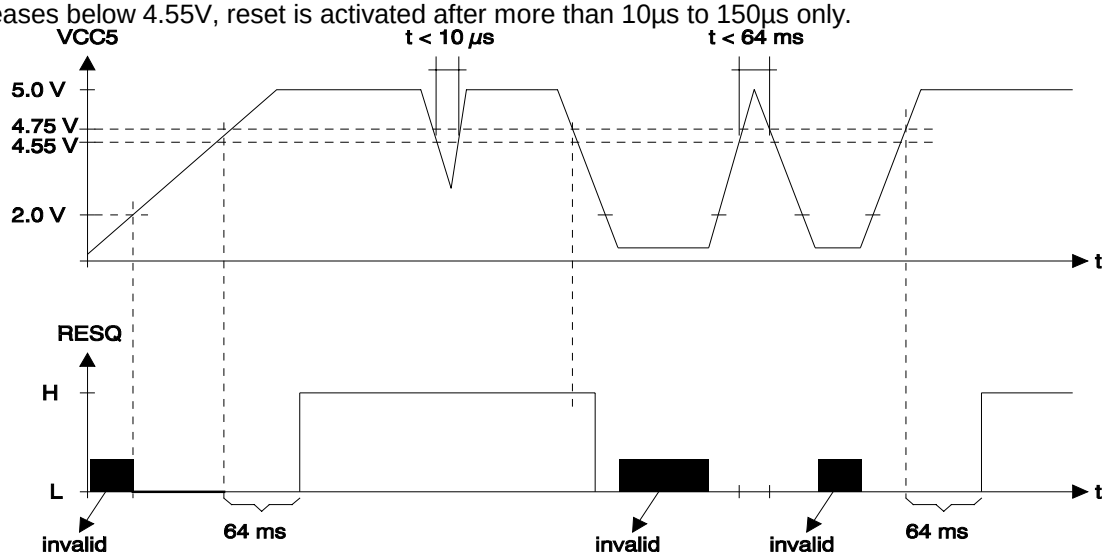




The duration of the output transistor conduction depends on VCC5 level and conduction is suppressed immediately if the current through the power FET exceeds typically 400mA or the voltage on pin VCC5 reaches typically 6V. The logic circuit inhibits in the case of short spikes, multiple pulse operation in one oscillating period.
During start up procedure the buck converter will be enabled, if the voltage on pin TVZ is greater than 1.85V.
So the EVZ voltage of the boost converter has to reach 60 % of its final value to enable the buck converter (5V). The buck converter will be disabled, only when a power down of EVZ occurs to less than about 7 % of the nominal voltage value on pin EVZ.
The output power FET works as a source follower and is designed to switch a maximum of 40V with a drain current limitation of typ. 400mA. To make the power dissipation of the output FET smaller, the voltage drop across the device can be reduced by increasing the gate voltage. This improvement can be executed by adding an external supply voltage to the pin EVZ2, which should be approximately 8V greater than the voltage on pin EVZ and realized by a bootstrap circuit.

Power On Reset of VCC5:

In order to avoid any system malfunction, a sequence of several conditions has to be passed. In case of VCC5 (5V)-power down a logic LOW output signal on pin RESQ is generated to disable an external microcontroller. When a voltage of VCC5 ≥ 4.75V is reached, the RESQ signal remains LOW for another 64ms before switching to HIGH. If VCC5 decreases below 4.55V, reset is activated after more than 10µs to 150µs only.



Watchdog Operation and Generation of the Squib Driver Enable Signal ZKEN:

The watchdog is driven by the oscillator frequency divided by 100 (= 1kHz). After power on, the LOW-signal on output RESQ for µC-reset is extended by 64 cycles. 32 clock cycles after the rising edge of RESQ, a chip internal trigger window (WDWI) begins. It ends after 32 cycles at the latest. If a trigger pulse (TRI) - coming via the serial peripheral interface (SPI) - occurs within the trigger window (or if a power-down occurs) the watchdog window signal is reset. The TRI pulse must be active for at least two rising clock edges and must return to zero for two clock edges. If no TRI pulse occurs in the trigger window, or if TRI pulse is outside of the trigger window, a reset (LOW) is generated on pin RESQ after 64 cycles and lasts for a further 64 cycles.

Correct triggering also will be executed, if after the falling edge of the TRI pulse signal only the sampling of the second 'low' occurs inside of the watchdog window. The beginning of the TRI pulse starts outside of the trigger window.

The TRI trigger pulse is set and latched by the SPI command WDTRH and reset by WDTRL. So the microcontroller is allowed to do measurements with the TLE 6710 during the TRI pulse is active.

In addition to the µC-reset signal RESQ, there exists an enable signal ZKEN for the internal squib drivers and for external firing circuits. If RESQ is high, the signal ZKEN goes to active high with the first valid trigger pulse TRI. It returns to low immediately if pretriggering, missing triggering or an incorrect trigger duration, as well as power down reset occurs. ZKEN is designed as an open drain output. If ZKEN is used as an input and held to 'low' by an external device, firing of the squibs can not be activated.

Accelerated testing via pin RTP and AW1CT:

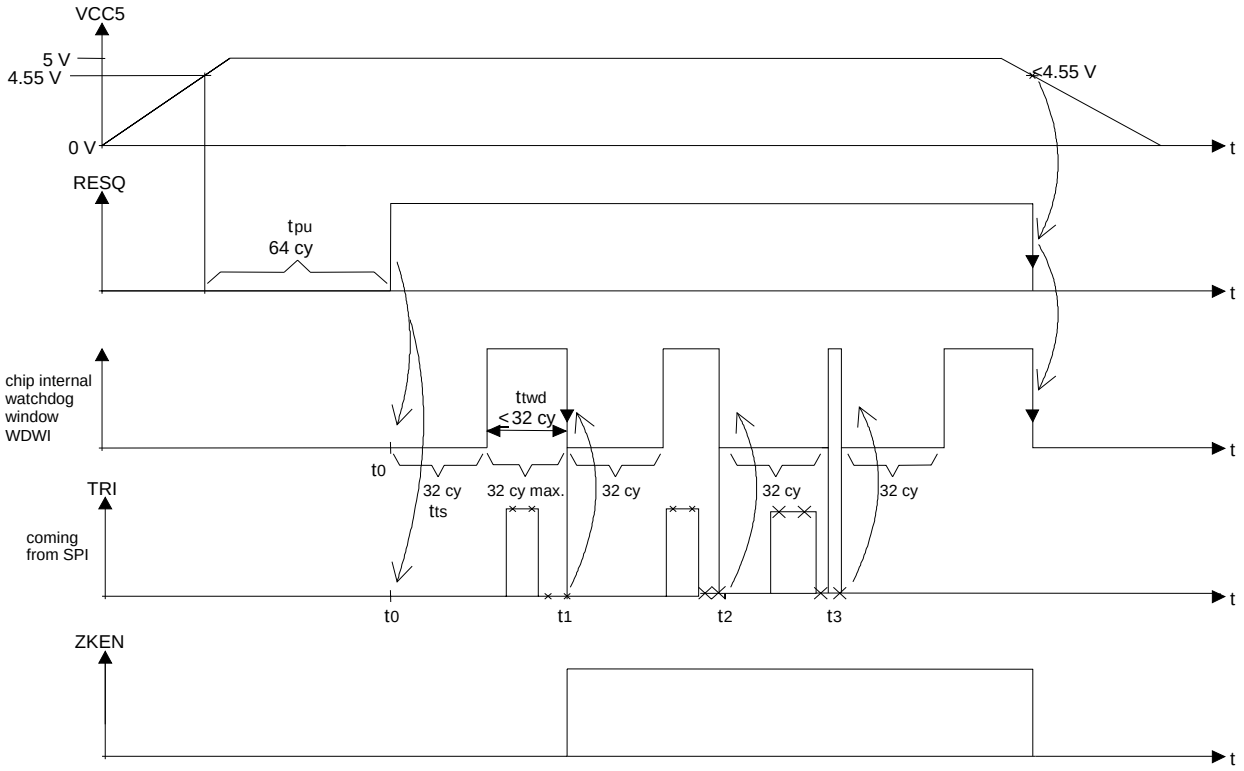
V_{VCC5}	V_{RTP}	AW1CT	RESQ	ZKEN	f_{WD} [kHz]	T_{WD} [ms]	Remarks
< 4.55 V	x	x	0	0	0	-	-
>4.75V	-0.3V ≤ V_{RTP} ≤ 0.8V	x	normal operating mode	Normal operating mode	1	1	
>4.75V	2.4V ≤ V_{RTP} ≤ V_{VCC5+} + 0.3V	1	1	1	1	1	test mode A
>4.75V	2.4V ≤ V_{RTP} ≤ V_{VCC5+} + 0.3V	0	normal operating mode	normal operating mode	25	0.04	test mode B
>4.75V	V_{VCC5} + 1.7V ≤ V_{RTP} ≤ 7.1V	1	1	1	25	0.04	test mode C

f_{WD} Frequency of the internal used 'Watchdog' - clock (f_{WD} = fos / 100; fos = 100kHz typ.)
For test mode B and C: f_{WD} = fos / 4

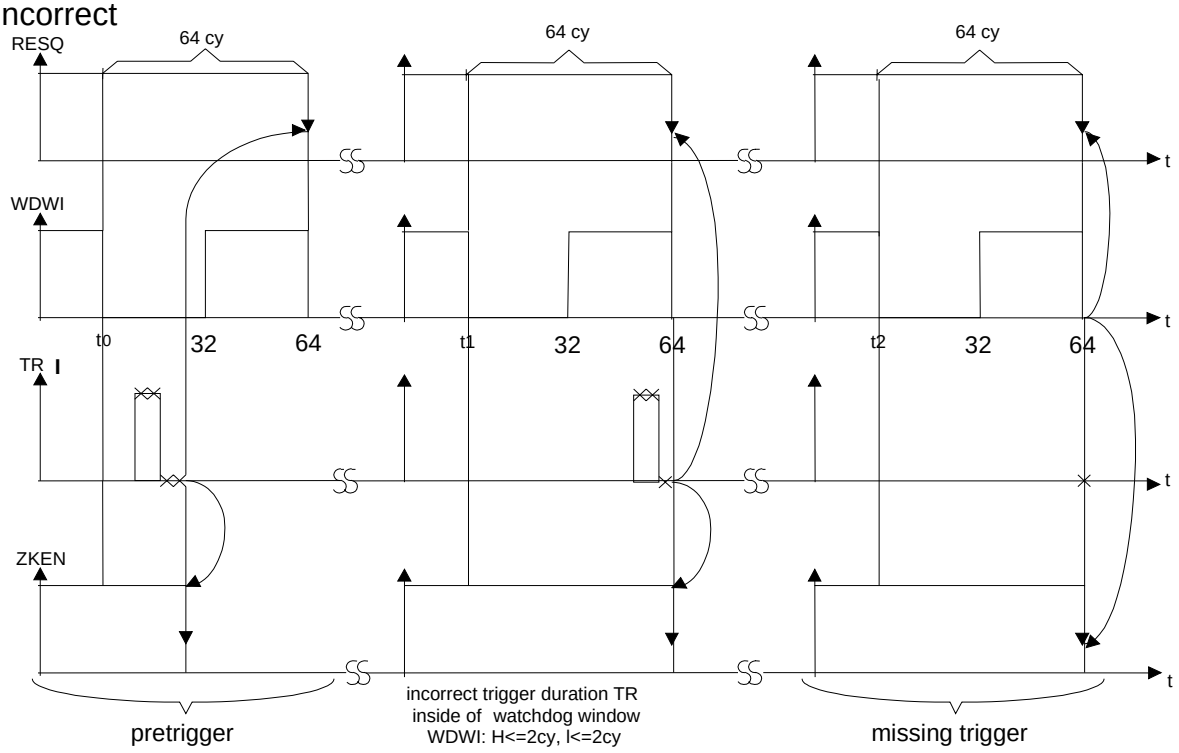
T_{WD} Period of the internal used 'Watchdog' - clock (= 1 / f_{WD})

Watchdog

A. Perfect triggering after power on



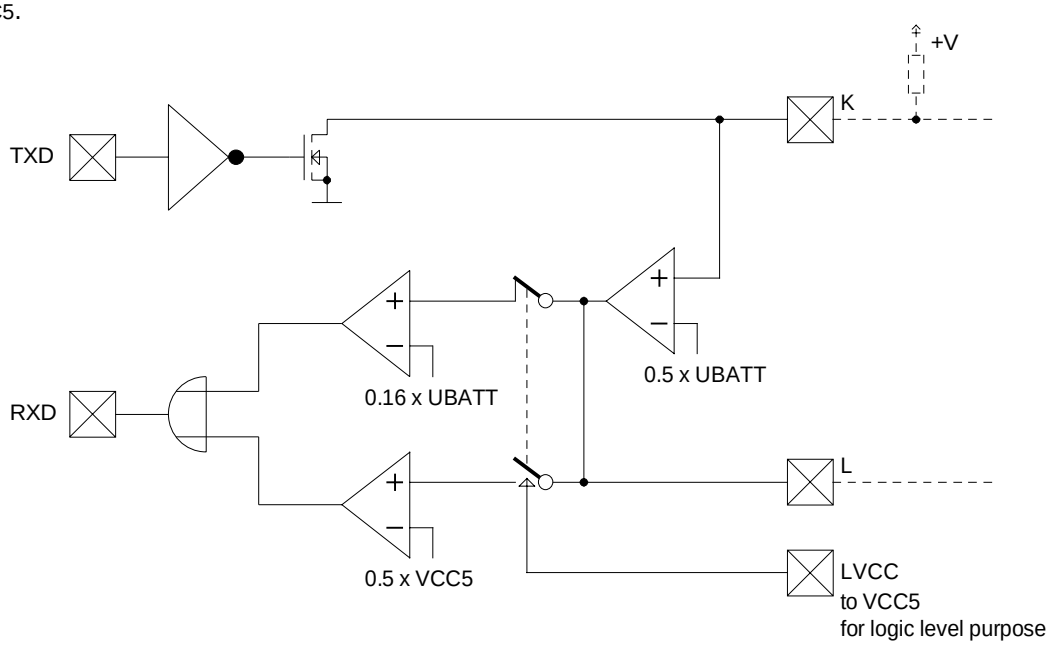
B. Incorrect



Note: After 'key ON' and sending the first correct SPI trigger command the output signal ZKEN is expected to transit to 'high' immediately. However it may stay 'low' longer depending on the voltage on pin ISS (Input Safing Sensor). This one time event happens only after a RESQ 'low' to 'high' transition in case of V_{ISS} = 0V to V_{VCC5}/2 (Spec. 20.4A), pin ISS = open or $V_{ISS} \geq V_{VCC5}$ + 1.2V (Spec.20.1). The time prolongation to achieve the rising edge on ZKEN will be 9800/f_{OS} (98ms typ.) starting from the rising edge of RESQ, if a SPI trigger command was successful at that time.

ISO 9141 - Serial Interface:

Serial data communication from external to the µC of the airbag board is provided by a 12V/5V-level-interface. The transmission signal TXD is transferred via an open drain output buffer to pin K. The external line signal K is linked to the receiving pin RXD. If the input pin L is not connected, the typ. threshold voltage on pin K is 0.5 x V_{UBATT}. If the input pin L is connected, the typical threshold voltage on pin L is 0.16 x V_{UBATT}. If it is necessary to handle a logic level input signal on pin L, the input pin LVCC has to be connected to VCC5. In this case the threshold voltage on pin L is 0.5 x V_{VCC5}.



Serial Peripheral Interface (SPI) and Decoder Logic:

The slave select pin SSQ allows the individual selection of different slave SPI devices. Slave devices that are not selected do not interfere with SPI bus activities. The SPI logic is selected by the slave select signal SSQ for the transmission of instructions like control and diagnostic commands.

(See chapter: 'J. Serial Peripheral Interface SPI')

The master-out slave-in pin MOSI is the input signal for the serial data from the µC, synchronously clocked by clock input CL, which operates at a maximum transmission rate of **4** Mbits/sec.

All commands, no matter which function, consist of 16 bits, so the TLE 6710 SPI includes a 16 bit input shift register, a 16 bit latch and a decoder logic block for the generation of the SPI command signals.

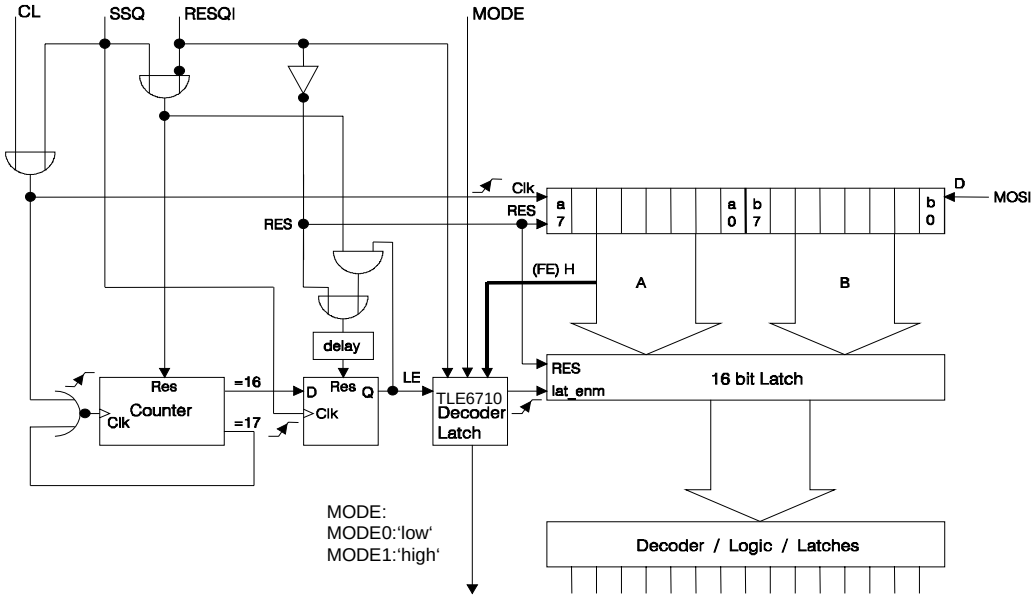
With the rising edge of CL the data via MOSI is shifted into the first bit of the shift register.

To suppress data transfer errors in the event that the clock signal includes spikes or glitches, a counter for 16 clock cycles is provided. Only after occurring of 16 clock cycles, the rising edge of SSQ causes an internal signal 'lat_enm' (latch enable) to transfer the data from the shift register to the 16 bit latch. A CMOS logic block decodes the 16 bit word of the latch to address the desired functional block.

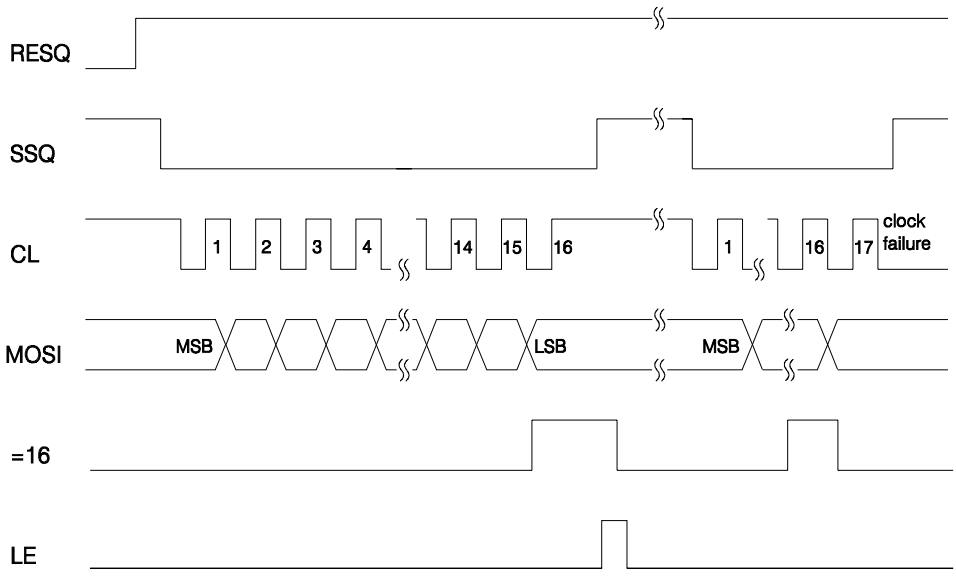
Mode definition: The TLE 6710 can be configured in two modes. The difference between the two modes are the definitions of the hardware pins HSEN_EN12, LSEN_EN34 and MODE for the functions of firing and squib measurements (see chapter J.2). A Mode1 operation requires an initializing SPI 'Mode command' (FExx)H and a 'high' on pin MODE before starting with SPI instructions. Otherwise the control and diagnostic commands will not be decoded. A MODE0 operation requires no SPI 'Mode command' however a 'low' or 'open' on pin MODE (due to a pull down resistor). With a hardware reset RESQ=0 the ASIC will return to its default state of the MODE0.

The following table shows the principle:

Mode	pin: MODE	SPI: Mode command
MODE0	0 or open	
MODE1	1	(FExx)H



Serial Peripheral Interface (SPI) and Decoder Logic:



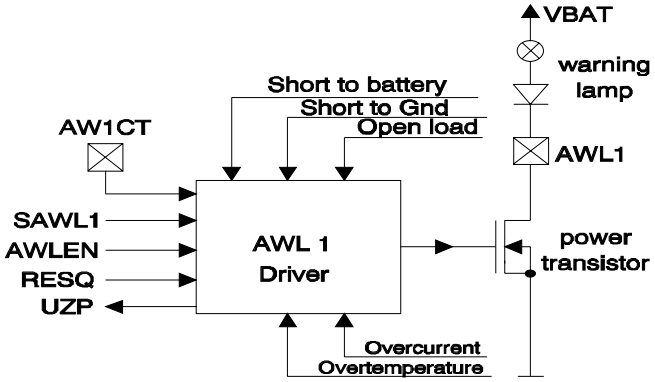
Timing of the Serial Peripheral Interface (SPI):

Alarm Warning Lamp Driver (AWL1):

The driver AWL1 is designed as a low side switch. Its logical behavior can be programmed via the control pin AW1CT. If AW1CT is not connected, the lamp driver AWL1 is ON as default. If AW1CT is connected to ground (0V), the lamp driver AWL1 is off as default. In case of missing EVZ or VCC5 the warning lamp is supplied via pin AWL1 with a typical saturation voltage of 2V, independent of the IC-supply voltage.

The following table defines all possible conditions:

AW1CT	EVZ	VCC5	RESQ	AWLEN	SPI-bit	Driver AWL1
open	ok	ok	0	X	X	ON
gnd	ok	ok	0	X	X	OFF
open	ok	ok	X	0	X	ON
gnd	ok	ok	X	0	X	OFF
open	ok	ok	1	1	SAWL1B	ON
open	ok	ok	1	1	SAWL1D	OFF
gnd	ok	ok	1	1	SAWL1B	OFF
gnd	ok	ok	1	1	SAWL1D	ON
open	ok	missing	X	X	X	ON
gnd	ok	missing	X	X	X	OFF
open	missing	ok	X	X	X	ON
gnd	missing	ok	X	X	X	OFF
open	missing	missing	X	X	X	ON
gnd	missing	missing	X	X	X	OFF



If AWL1 is on and the voltage on pin AWL1 is greater than typically 2V, the lamp current is limited. To protect the integrated power switch against overtemperature, a thermal limitation circuit is provided. This feature prevents catastrophic failures from accidental device overheating. The temperature limitation circuit starts to work, if the voltage drop across the power transistor is greater than typically 2V. The lamp status is reported as an information of the voltage or of the current on pin AWL1 to the general analogue measurement output pin UZP.

1. Voltage measurement on pin AWL1:

Via SPI command UAWL1 the voltage on pin AWL1 is measured and linked to the measurement pin UZP with a voltage ratio of 5 to 1.

Following detections are possible:

- Short to battery if lamp is switched on
- Over temperature if lamp is switched on
- Short to ground if lamp is switched off
- Open load if lamp is switched off

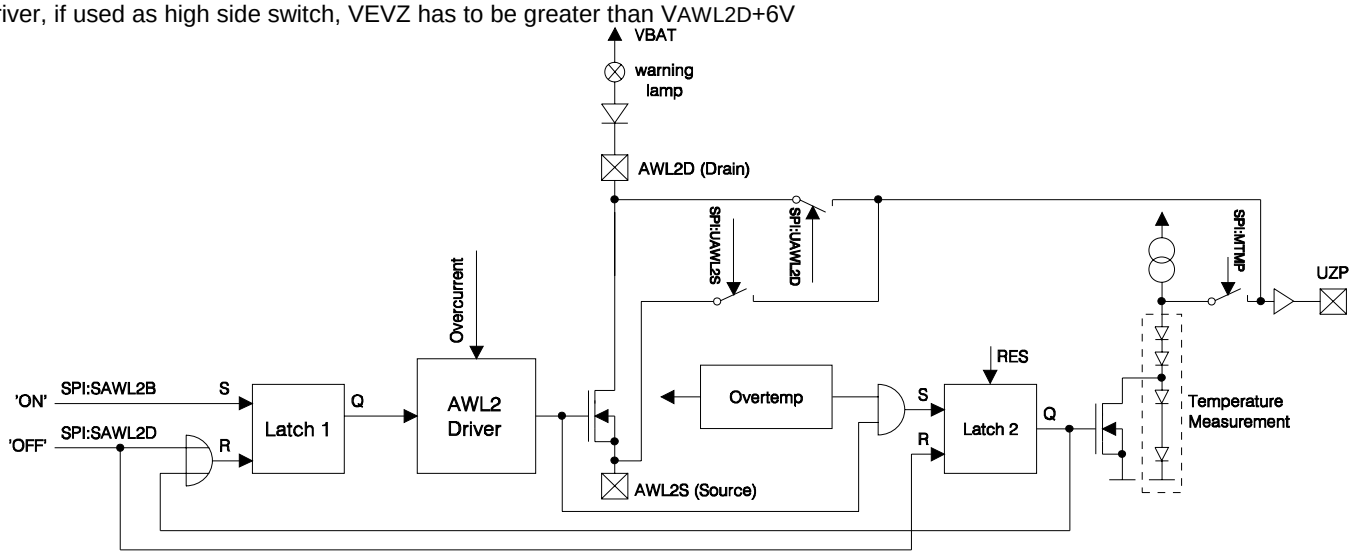
2. Current measurement on pin AWL1:

Via SPI command IAWL1 a current level on pin AWL1 is detected and reported to the measurement pin UZP as a digital information for 'open load if lamp is switched on'.

Lamp switched to	Lamp current	V_{UZP}
on	≤10 mA	0 to 0.4 V
on	≥30 mA	1.5 V to V_{VCC5}

Alarm Warning Lamp and Multifunction Driver 2 (AWL2):

A second warning lamp block (AWL2) is provided to drive high side or low side loads.
The default state of the driver is "off". The driver can be switched on via SPI control bits. To obtain minimum on resistance of the driver, if used as high side switch, VEVZ has to be greater than V_{AWL2D}+6V



In case of missing the voltage EVZ or VCC5 the driver is switched off. The pin AW1CT has no influence to the status of the AWL2-driver.

EVZ	VCC5	RESQ	SPI	driver awl2
ok	ok	0	X	OFF
ok	ok	1	on	ON
ok	ok	1	off	OFF
missing	ok	X	X	OFF
ok	missing	X	X	OFF
missing	missing	X	X	OFF

The load current is limited to 250 to 600 mA.
The load status is reported as an information for the voltage on pins AWL2S and AWL2D to the general analogue measurement output pin UZP. This information can be selected by the corresponding SPI commands.

1. Voltage measurement on pin AWL2D:

Via SPI command UAWLD the voltage on pin AWL2D is measured and linked to the measurement pin UZP with a voltage ratio of 5 to 1.
Following detections are possible:

- Short to battery if driver is switched on
- Overtemperature if driver is switched on
- Short to ground if driver is switched off
- Open load if driver is switched off

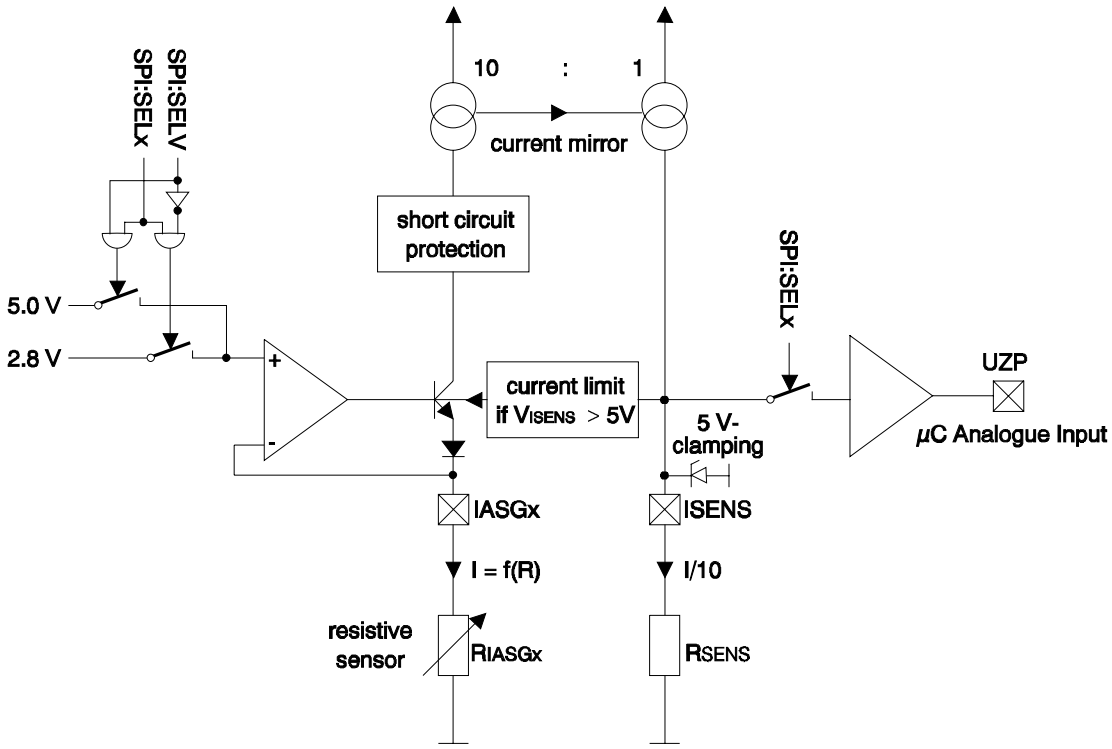
2. Voltage measurement on pin AWL2S:

Via SPI command UAWLS the voltage on pin AWL2S is measured and linked to the measurement pin UZP with a voltage ratio of 5 to 1.
Following detections are possible:

- Short to ground if driver is switched on
- Overtemperature if driver is switched on
- Short to battery if driver is switched off
- Open load if driver is switched off

Current can be measured by connecting a resistor from drain pin to battery supply or source pin to ground corresponding to the application. The voltage drop across the resistor indicates the current through the load.
To protect the integrated power switch against overtemperature, a thermal shut down circuit is included. This feature prevents catastrophic failures from accidental device overheating. The attached schematic shows the principal function in case of overtemperature. If the lamp driver is on and an overtemperature signal of the AWL2 driver occurs, latch 2 is set and latch 1 is reset to switch off the driver. Activating an 'Average Chip Temperature'-measurement reports to pin UZP a reduced voltage of less than approx. 1.4V, which can be interpreted as a digital information of over temperature of lamp driver 2. Returning to the specified 'Average Chip Temperature' measurement only can be done by a SPI command SAWL2D (to switch off the lamp).

Voltage-/ Current Sources:



The functional block 'V/I-Sources' is provided to measure the value of four different external resistors and can be addressed by a special SPI command SELx (x=1,2,3,4) $(2XXX)_H$. After being addressed a constant voltage source of 2.8V on pin IASGx is activated and a current flows through one addressed external resistor. The resistance dependent sensor current is reflected by a 10 to 1 current mirror to an analysis path ISENS. The voltage drop of R_{SENS} on pin ISENS is proportional to the actual external resistive sensor value and is reported 1:1 to pin UZP. This signal is connected with an analogue port of the µC and stored as first measurement value. Due to the possibility of an external ground shift a second measurement occurs to use a difference measurement principle to eliminate a constant ground voltage shift. Therefor the SPI command SELx (x=1,2,3,4) AND SELV $(BXXX)_H$ has to be addressed to activate the constant voltage source to the second value of 5.0V on pin IASGx. This voltage determines a second voltage value on pin UZP.
Calculation of the external resistance value on pin IASGx (done by the µC):

$$R_{IASGx} = \frac{R_{SENS}}{10} \times \frac{5.0V - 2.8V}{V_{ISENS2} - V_{ISENS1}}$$

The current through pin IASGx is limited to |25|...|80| mA, if pin IASGx is shorted to ground and the voltage on pin ISENS does not reach V_{VCC5} due to a low resistor on pin ISENS. However the value of the IASGx current limitation can be reduced by increasing the value of the resistor on pin ISENS. Then the maximum current through pin IASGx can be calculated as:

$$I_{IASGx\,lim} = 10 \times \frac{V_{VCC5}}{R_{SENS}}$$

For high accuracy the IASGx current needs to be between 1 and 20mA and the maximum ISENS voltage is less than V_{VCC5}-0.3V. Under clamping condition the voltage on pin ISENS is clamped to V_{VCC5} + 0.3V.
Calculation of the value of the resistor on pin ISENS:

$$R_{SENS} = 10 \times \frac{V_{VCC5} - 0.3V}{I_{IASGmax}}$$

Squib Drivers:

The TLE 6710 includes four independent driver circuits to fire one squib each. The deployment of a squib is only initiated, if two independent switches of the firing squib loop are closed. These two serial switches are realised by one highside DMOS[1)]-switch from squib supply pin VZx (x=1,2,3,4) to the first terminator of the squib ZPx1 (x=1,2,3,4) and one lowside DMOS-switch from the second terminator of the squib ZPx2 (x=1,2,3,4) to ground Mx (x=1,2,3,4).

The squib will fire only if all following signals are present: RESQ = 1,

Mode	MODE	ZKEN	ZKEN_int	HSEN_EN12	LSEN_EN34	Function
MODE0	0	1	1	1	0	(8xxx)H: firing of HSx and / or LSx
MODE1	1	1	1	1	0	(8xxx)H: firing of squib 1 and 2
MODE1	1	1	1	0	1	(8xxx)H: firing of squib 3 and 4
MODE1	1	1	1	1	1	(8xxx)H: firing of squibs 1 to 4

For MODE1 operation an initializing SPI 'Mode command' needs to be sent once after start up. If RESQ = 0 is generated, then the measurement will be interrupted and the ASIC will return to its default state of the MODE0. A soft reset (FFFF)H does not change the mode. ZKEN must be generated internally (ZKEN_int) to high. Used as an input the ZKEN signal is not allowed to hold it to GND by an external device.

In case of activating the lowside switching transistor the firing current will be sensed (squib driver 1 and squib driver 2 only). If the current exceeds 1.75A, a digital firing current signal can be detected on pins LL and LH as described in the following table:

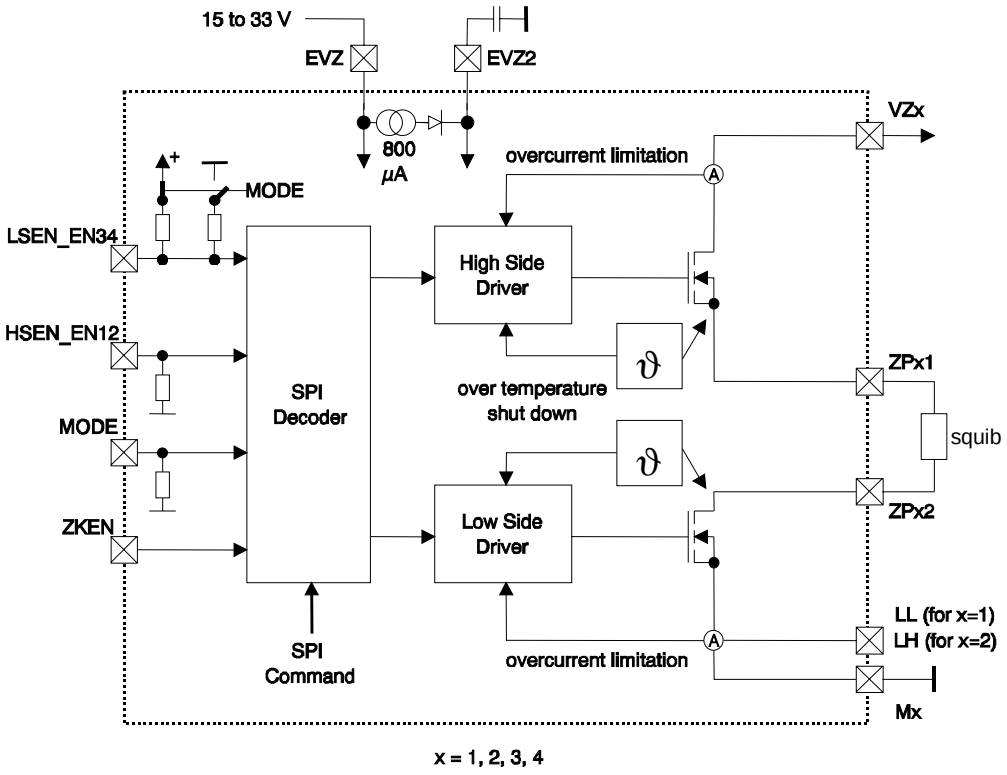
Firing current of squib 1	Firing current of squib 2	V_{LL}	V_{LH}
0A	0A	high	high
>1.75A	0A	low	high
0A	>1.75A	high	low
>1.75A	>1.75A	low	low

The maximum firing current of the squib loop is limited to 3.0 A by reducing the gate to source voltage of the low side DMOS transistors.

For a drain to source voltage drop less than approximately 2V of each switching transistor, no reduction of gate to source voltage of the squib transistor is demanded. So the sum of voltage drops across the high side and low side transistors does not exceed 3.0 V at 1.75 A of squib current. The gate driver of the high side transistor is supplied via pin EVZ2. A current source from EVZ to an external capacitor on pin EVZ2, de-coupled by a diode provides a sufficient gate to source voltage for the DMOS.

To protect each individual squib driver transistor in the event that the peak junction temperature of the transistor exceeds 280^{O}C a thermal toggling circuit is provided to avoid a further increasing of the DMOS temperature. This feature prevents catastrophic failures from accidental device overheating. Due to too long switch on times and high power consumption the thermal toggling leads to a general increasing of the average chip temperature. If the average chip temperature exceeds 100°C, a driver will be deactivated under thermal toggling and stays in off-state by a latch. Repeating on-commands do not activate the affected transistor, however to resume firing it will be necessary to send a NO OP-, 0000-, driver-off- or any measurement-command to reset the latch, before sending a new firing command, once the average temperature falls below its critical level.

1).....DMOS: Double Diffused Metal Oxide Transistor



Truth table for the squib drivers:

Mode	MODE	ZKEN	ZKEN_int	HSEN_EN12	LSEN_EN34	SPI command / Function
MODE0	0	1	1	1	0	(8xxx)H: firing of HSx and / or LSx
MODE0	0	x	1	1	1	(7xxx)H: reference + HSx main current
MODE0	0	x	1	1	x	(Cxxx)H: measurement with HSx on
MODE0	0	x	1	x	0	(Cxxx)H: measurement with LSx on
MODE1	1	1	1	1	0	(8xxx)H: firing of squib 1 and 2
MODE1	1	1	1	0	1	(8xxx)H: firing of squib 3 and 4
MODE1	1	1	1	1	1	(8xxx)H: firing of squibs 1 to 4
MODE1	1	x	1	0	0	(7xxx)H: reference + HSx main current
MODE1	1	x	1	0	0	(Cxxx)H: measurement with HSx on
MODE1	1	x	1	0	0	(Cxxx)H: measurement with LSx on

LSx low side switch of the squib driver (x = 1,2,3,4)
HSx high side switch of the squib driver (x = 1,2,3,4)

For MODE1 operation an initializing SPI ‘Mode command’ needs to be sent once after start up. If RESQ = 0 is generated, then the measurement will be interrupted and the ASIC will return to its default state of the MODE0. A soft reset (FFFF)H does not change the mode. ZKEN must be generated internally (ZKEN_int) to high. Used as an input the ZKEN signal is not allowed to hold it to GND by an external device.

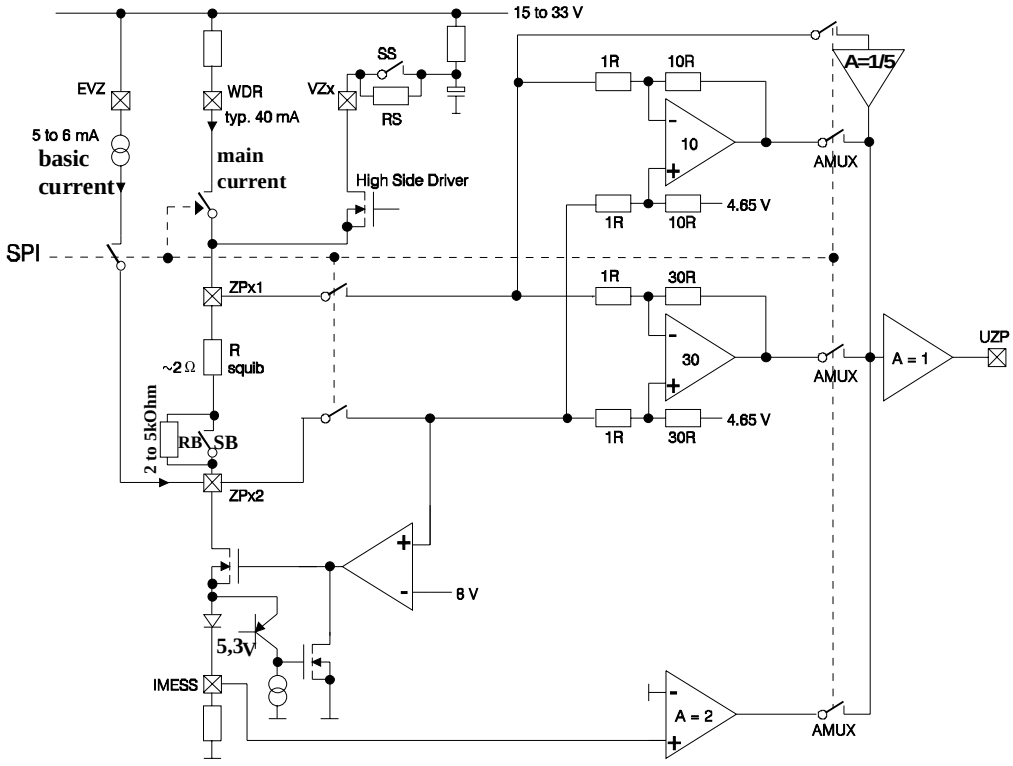
Squib Resistance Measurement:

The squib resistance measurement module consists of several circuit parts and can be addressed by a SPI command (4XXX)H. After being addressed a current source of approximately 5.5mA is activated and this current flows as a reference measurement current through ZPx2. The appropriate voltage drop across the squib is amplified by a precise amplifier with a fixed gain of either 10 or 30 and monitored on the external analogue output pin UZP. The measurement current is also reported by the voltage drop across the external resistor on pin IMESS. The value of this basic current through pin IMESS is determined by the external resistor on pin ROS and can be calculated by the following formula:

$I_{IMESS} = I_{ROS} \times 55 \times 5/12$ $I_{ROS} = 1.2V / R_{ROS}$ (I_{ROS}=240µA @ 5kΩ)

One of the recommended values for R_{ROS} in the application circuits is 4.99kΩ.

After the first reference measurement has been performed with the current of typ. 5.5mA, a second measurement with a programmable current source of typically 40mA is started by an additional SPI command (6XXX)H. This current is determined by an external resistor from pin EVZ to pin WDR. The voltage on pin WDR is regulated to approximately 9 V.



Squib resistance measurement: Functional schematic

Application note for calculation of the external resistor R_{WDR}:

$$R_{WDR} = \frac{V_{EVZ} - (7.5 \text{ to } 8.5V)}{I_{WDR}} - (10 \text{ to } 50\Omega) \qquad I_{WDR} < 60mA,$$

Rsquib = 2Ω approx.

Also for the second measurement the voltage drop across the squib (x10 or x30) via pin UZP and the measurement current via the pin IMESS are reported to the microcontroller. This feature enables the µC to calculate the external squib resistance with a high accuracy by eliminating DC-offsets.

Calculation of the squib resistance R_{squib}:

$$R_{squib} = \frac{V_{UZP1} - V_{UZP2}}{(V_{IMESS2} - V_{IMESS1})} \times R_{IMESS} \; / \; \text{gain factor (10 or 30)} \qquad V_{UZP1} = 0.9 \times V_{VCC5} \text{ typ.}$$

$$R_{IMESS} = 50\Omega \text{ approx.}$$

There is another way to measure R_{squib}, if a mechanical safing sensor (SS) with a resistor (RS) is used in parallel. Instead of activating the higher measurement current the highside switch of a squib driver can be switched on via SPI: $(7XXX)_H$. Now a current determined by the resistor RS flows through the squib and is reported to UZP and IMESS.
For buckle switch measurement purposes an amplifier with gain 2 was provided. In applications a buckle switch (SB) with a 2kΩ to 5kΩ resistor (RB) in parallel is connected in series to the squib. For the distinction between a broken and an open seat belt switch the result of the gain 10/30 amplifier gives us no information, so the voltage drop across pin IMESS multiplied by two can be reported to pin UZP to increase the sensitivity of the current measurement through the pin IMESS. If this principle does not give information enough a squib voltage measurement with activated 'main current' can be performed to multiplex V_{ZPx1} / 5 to pin UZP. So the SPI commands for the squib resistance measurement select between a measurement of the voltage drop across the squib (gain 10/30 amplifier), a measurement of the voltage drop across pin IMESS (gain 2 amplifier) or a measurement of the voltage on pin Zpx1 (divided by 5) reported to pin UZP each.
The measurement for each squib is activated separately, but the analogue output signals on pins UZP and IMESS are common.
Note 1: The high measurement current through the squib requires a force and sense measurement principle to guarantee the high resistance measurement accuracy. So the precise gain-10-amplifier sense inputs and the gain-30-amplifier sense inputs are bonded separately to the pins ZPx1 and ZPx2. (x=1,2,3,4).
Note 2: The analogue output pin UZP can be connected in parallel with other ASICs on one PCB.
Note 3: The current output pin IMESS can be connected in parallel with other ASICs on one PCB. So the external resistor on pin IMESS is only used once and is common for all IC's.

Squib Leakage Measurement:

The leakage resistance measurement module can be addressed only for one squib at one time by a SPI command $(1XXX)_H$. The current for the leakage measurement I_{RLM} is determined by the reference resistor R_{RLM} from pin RLM to ground, which is supplied by a voltage of V_{UBRL} / 3 .

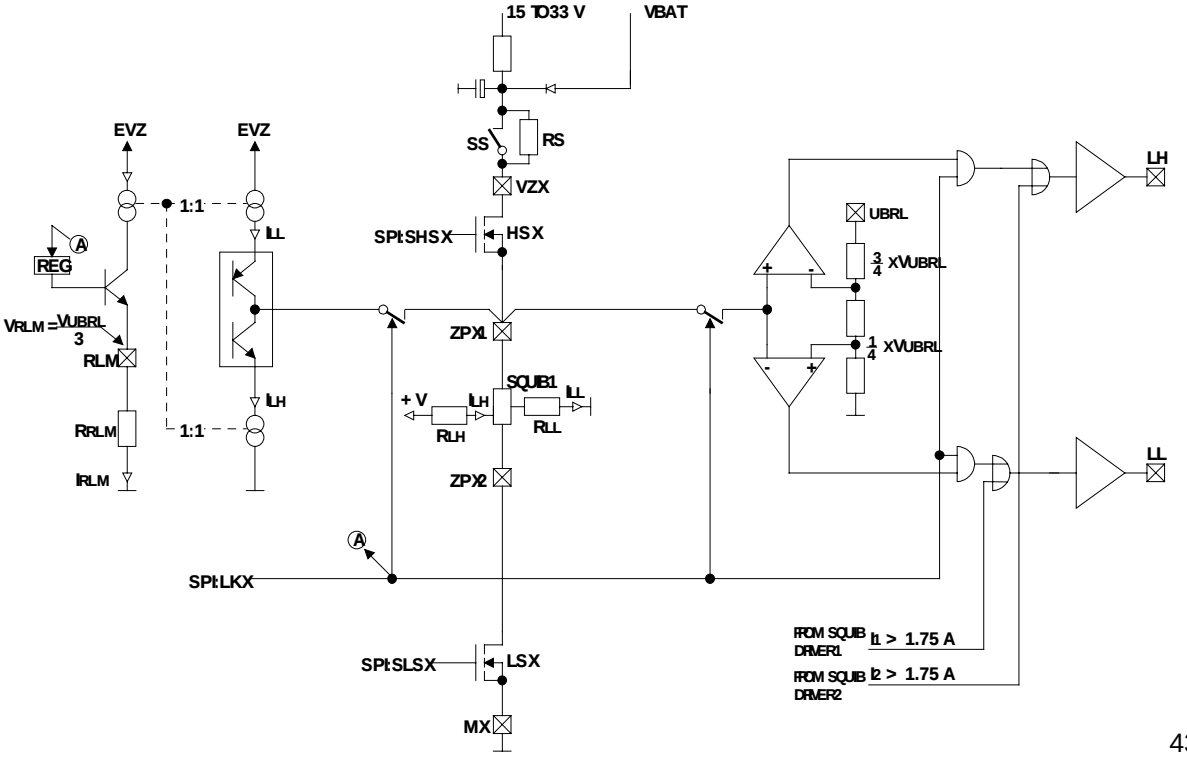
$$I_{RLM} = \frac{V_{UBRL}}{3 \times R_{RLM}} = I_{LL} = I_{LH}$$

Due to a leakage the programmed leakage current I_{RLM} can flow either from the squib system via the leakage resistor R_{LL} to ground (I_{LL}) or from a positive voltage +V via the leakage resistor R_{LH} into the squib system (I_{LH}). See schematic.

Across the leakage resistors R_{LL} and R_{LH} the following leakage voltage drops can be monitored:

$$V_{ZPx1\,to\,GND} = I_{LL} \times R_{LL} = \frac{V_{UBRL}}{3 \times R_{RLM}} \times R_{LL}$$

$$V_{UBRL\,to\,ZPx1} = I_{LH} \times R_{LH} = \frac{V_{UBRL}}{3 \times R_{RLM}} \times R_{LH} \qquad x = 1,2,3,4$$



43

Leakage resistance measurement: Functional schematic

For the TLE 6710 the leakage resistance threshold is defined by:

$$R_{Leak} = R_{LL} = R_{LH} = R_{RLM} \times 3/4$$

and so the leakage voltage drops become:

$$V_{ZPx1\,to\,GNDB} = V_{UBRL} / 4$$

and

$$V_{+V\,to\,ZPx1} = V_{UBRL} / 4$$

Two comparators, which are referenced to 1/4 x V_{UBRL} and 3/4 x V_{UBRL}, determine a leakage to V_{UBRL} or a higher voltage by setting pin LH to 'low' and a leakage to ground by setting pin LL to 'low'. If no leakage is detected the pins LL and LH report 'high'.
To prevent jitters on the output pins a hysteresis of 1/48 x V_{UBRL} is provided in both comparators.

Leakage resistance malfunction can be simulated in a testmode by switching on only the squib driver highside transistor for a leakage to battery, as well as by switching on only the lowside transistor for a leakage to ground by SPI: (CXXX)H. (see chapter 'SPI Commands').

Supply Voltage Measurements:

By SPI commands (1XXX)H (see chapter J.2.8) different voltage measurements are activated and reported to the analogue output pin UZP with a defined voltage ratio. The pin names of the voltage sources which can be selected are:

UBATT, UBRL, ZPx1	voltage ratio to pin UZP: 5,
EVZ, EVZ2, VZ1, VZ2, VZ3, VZ4	voltage ratio to pin UZP: 8.

For test purposes the internal used reference voltage can be measured by addressing the SPI command UREF: (AA AA)H.

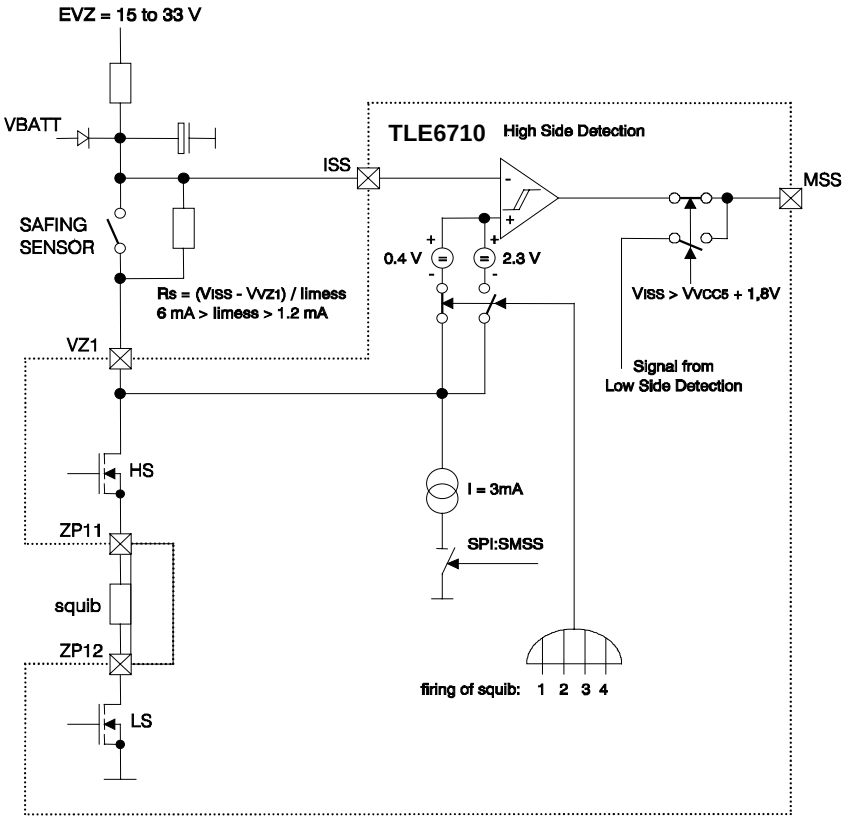
UREF	voltage ratio to pin UZP: 1 (+/-7%).

Detection of Safing Sensor Closure:

Depending on the voltage on pin ISS either the high side - or the low side detection circuit is activated.

High Side Detection:

For $V_{ISS} \geq V_{VCC5}$+1.8V the 'Safing Sensor' high side - detection is turned on.
This comparator circuit detects a closure of an external 'Safing Sensor' of the system between the pins VZ1 and ISS. A closure Safing sensor switch reports a 'high' to pin MSS. If under firing condition the differential voltage between VZ1 and ISS exceeds typ.2.3 V output MSS changes to 'low'.
For testing purposes a current source (typ. 3 mA) from pin VZ1 to ground can be addressed by the SPI command: SMSSH. In this case a testing current flows through a resistor in parallel with the Safing Sensor. The voltage drop across VZ1 and ISS is high enough to exceed the MSS comparator threshold voltage of typ. 0.4 V to get 'low' on pin MSS.

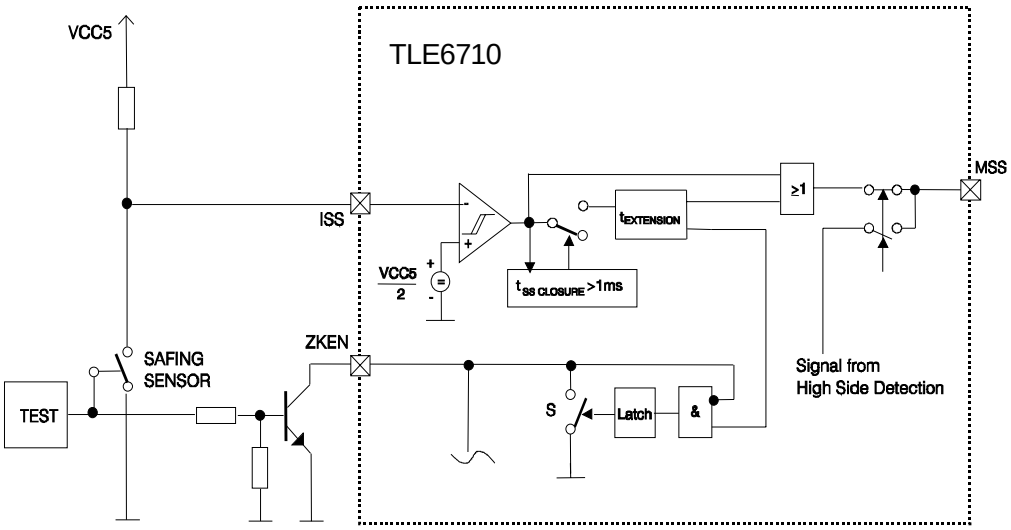


Functional description ($V_{ISS} \geq V_{VCC5}+1.8$ V)	$V_{ISS} - V_{VZ1}$	V_{MSS}
Safing sensor closed	0V	'high'
Safing sensor open and squib driver inactive (off)	0V	'high'
Safing sensor open and squib driver active (on)	10 to 30V	'low'
Safing sensor open and squib driver inactive (off) and 3mA current source activated by SPI	≥0.3V	'low'
Safing sensor closed and one to four squib drivers active (on)	≥2.1V	'low'

Low Side Detection:

A voltage on pin ISS of $V_{ISS} \leq V_{VCC5}+0.6V$ activates the 'Safing Sensor' low side - detection.
This comparator circuit detects a closure of an external 'Safing Sensor' from pin ISS to ground, which is reported to pin MSS and indicated by a 'high' state at this output ('Closure' means that $V_{ISS} \leq V_{VCC5}/2$ typ.). To describe the behavior of the pin MSS depending on ISS and ZKEN, following cases need to be considered together with the time diagrams on the following page:

Case 1: If the closure time of the safing sensor $t_{closure}$ is less than 0.5 ms, then the output MSS will follow the inverted input signal ISS.
Case 2: In case of a duration of the safing sensor closure $t_{closure} \geq 1$ms a time extension of $t_{add} = 96.5$ms is triggered. The input signal ISS will be sampled by a clock with the period of $T_S=50/f_{OS}$. The MSS time prolongation will be started only, if the internal clock ($1/T_S$) samples a transition of H==>L==>L (see x in the timing diagrams). The output MSS remains 'high' for the total period of time $t_{sum} = t_{detect} + t_{add} = (0.5 \div 1)$ms + 96.5ms. To describe the behavior of the MSS - output after this period of time, following cases must be considered.
The state on pin MSS will return to 'low', if the voltage on pin ISS has returned to 'high' and has been 'high' continuously within this period of time plus 0.5ms.
Case 3: If the closure still exists after this period t_{add} plus 1ms, the output MSS will be triggered again and will remain in 'high' state for another t_{add} period .
Case 4: After an interruption of the safing sensor closure of at least 0.5ms within the extension period t_{add} a retrigger will occur, if the following closure time is longer than 1ms. An interrupt less than 1ms does not have any effect on the origin time extension.
Case 5: For testing purposes of the external safing sensor the squib drivers can be disabled externally via the pin ZKEN. Whenever this happens, and the time extension is activated ($t_{closure} \geq 1$ms), the voltage on pin ZKEN is kept 'low' internally by the ASIC within this period (t_{add}) of time (see switch S in the following schematic).

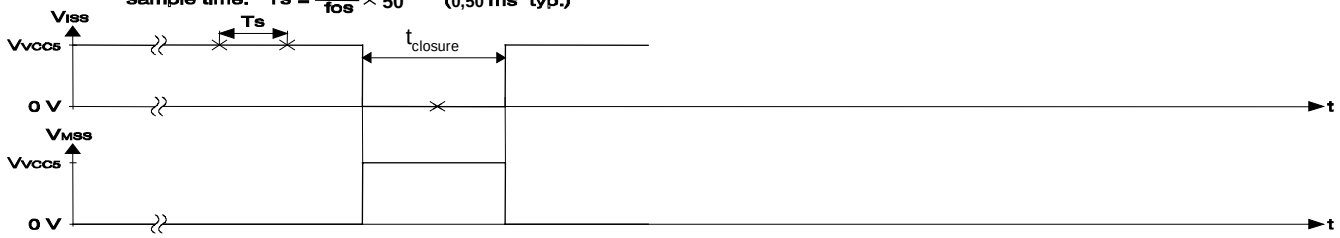


Function description ($V_{ISS} \leq V_{VCC5}+0.6$ V)	V_{ISS} [V]	V_{MSS}	t_{sum} [100/f_{OS}]
Safing sensor open	$V_{VCC5} \geq V_{ISS} \geq (V_{VCC5}/2)+0.1$	'low'	----
Safing sensor closed ($t_{closure} \leq 0.5 \cdot 100/f_{OS}$)	$V_{ISS} \leq (V_{VCC5}/2)-0.1$	'high'	$t_{closure}$
Safing sensor closed ($t_{closure} \geq 1 \cdot 100/f_{OS}$)	$V_{ISS} \leq (V_{VCC5}/2)-0.1$	'high'	$(0.5+96.5) \leq t_{sum} \leq (1+96.5)$
Safing sensor retrigger ($t_{interrupt} \geq 0.5 \cdot 100/f_{OS}$)	$V_{ISS} \leq (V_{VCC5}/2)-0.1$	'high'	$(0.5+96.5) \leq t_{sum} \leq (1+96.5)$

Detection without Time Extension

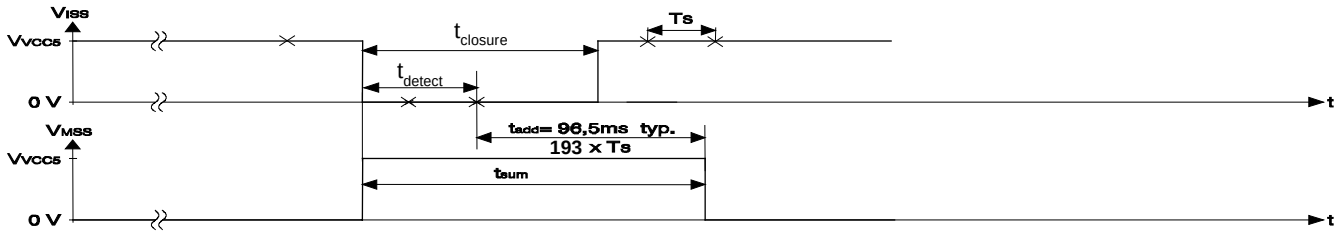
Case 1:

sample time: $Ts = \frac{1}{fos} \times 50$ (0,50 ms typ.)

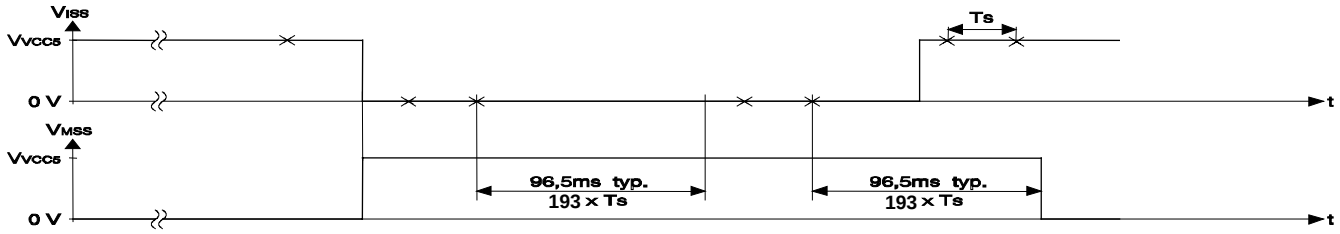


Detection with Time Extension

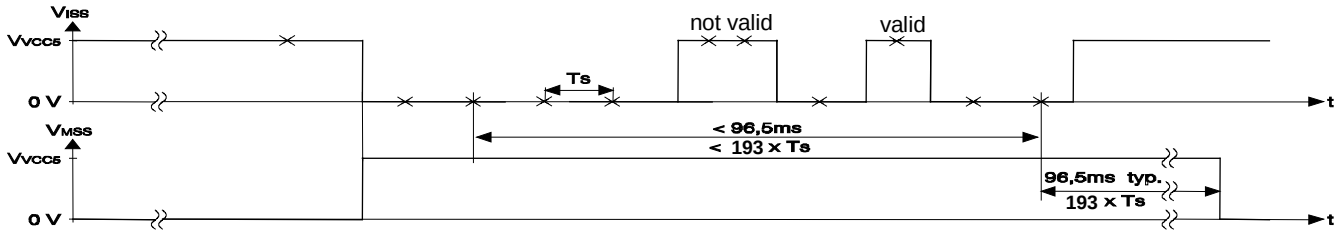
Case 2: Triggering Mode



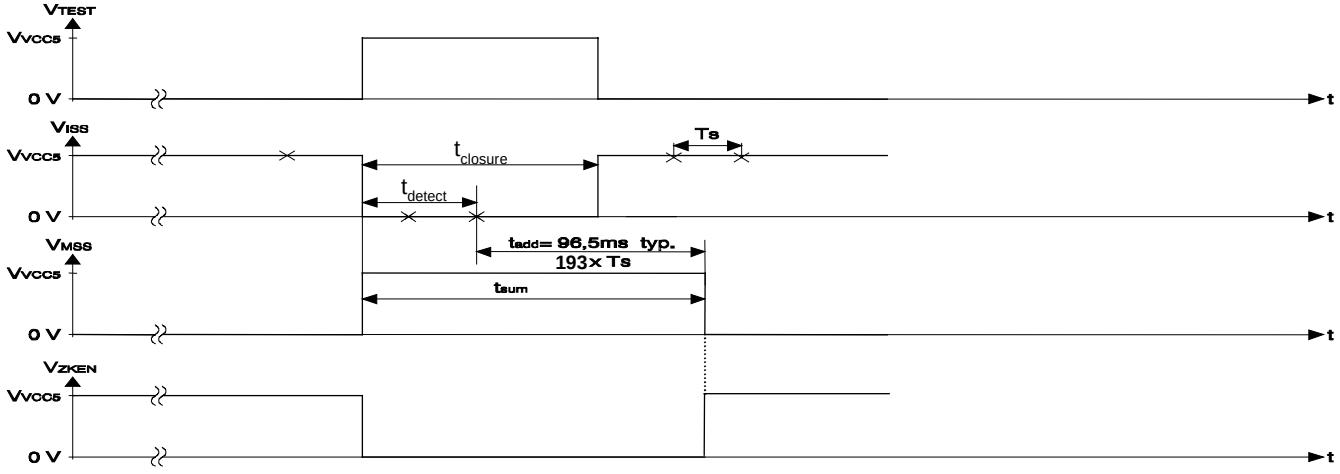
Case 3: Retriggering Mode



Case 4: Retriggering Mode with Interruptions



Case 5: Testmode



Average Chip Temperature Measurement:

A SPI command (9XXX)H (MTEMP) allows to measure the temperature dependent voltage of 4 diodes connected in series via the pin UZP. The diodes are supplied by a temperature constant current source which is generated in the oscillator circuit. The current depends on the resistor on pin ROS.

$$I_{DIODES} = I_{ROS} / 6 = 0.2V / R_{ROS}$$

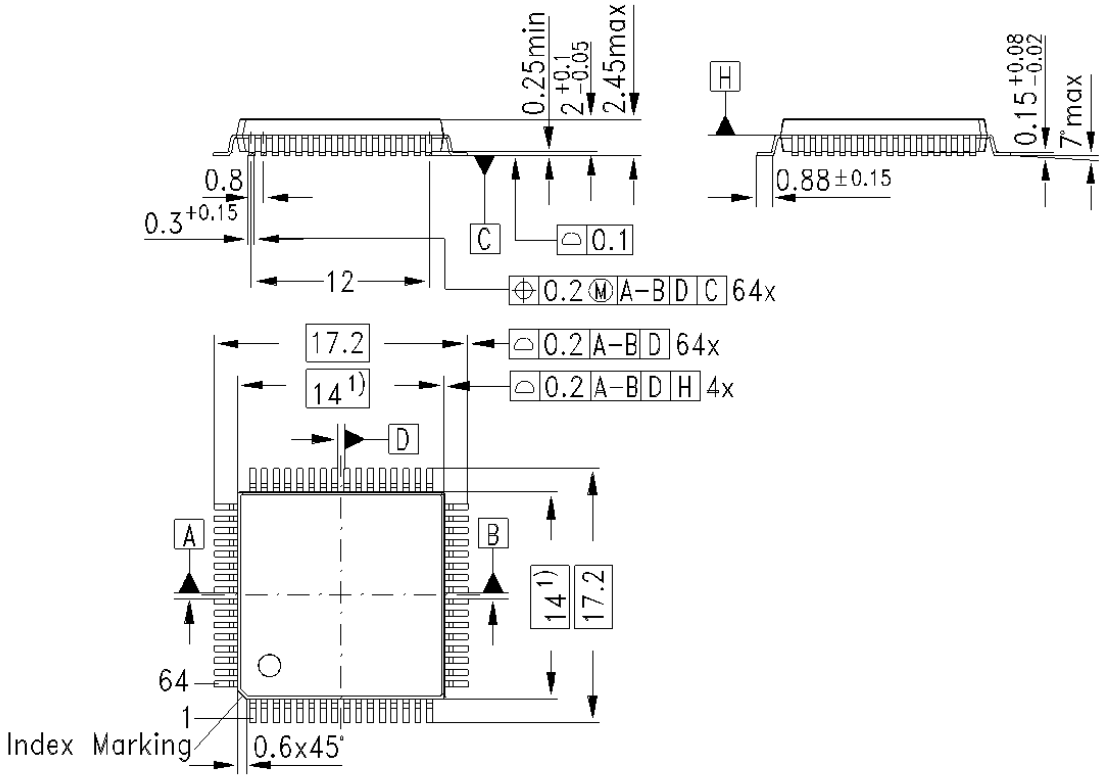
With ROS = 5kΩ the current will be 40µA. The temperature dependence of the voltage across the four diodes is approximately - 7 mV/K. The nominal value at room temperature (25°C) will be 2.9 V.
The value will be divided by two after an overtemperature shut down of the lamp driver AWL2 (see chapter AWL2).

Grounding Requirements for External Components on PCB:

The external components from the following pins to ground are necessary to be grounded to pin GNDB. The connections have to be low resistive and without any voltage shift to the ground pin GNDB.
Critical pins: ROS, TVZ, UZP, IMESS, RLM, ISENS

C. Package Outline

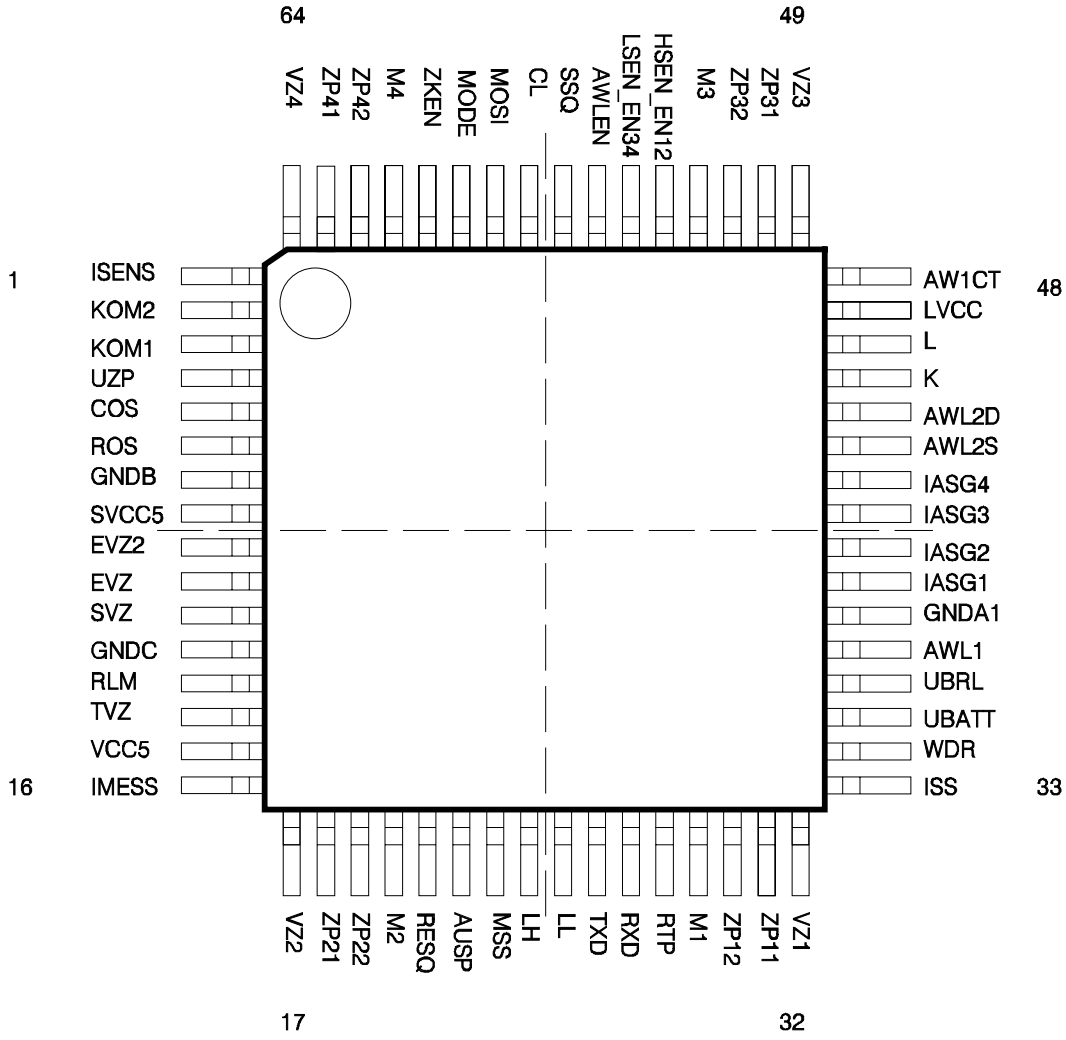
P-MQFP-64-1



1) Does not include plastic or metal protrusions of 0.25 max per side

D. Pin Configuration

(top view)



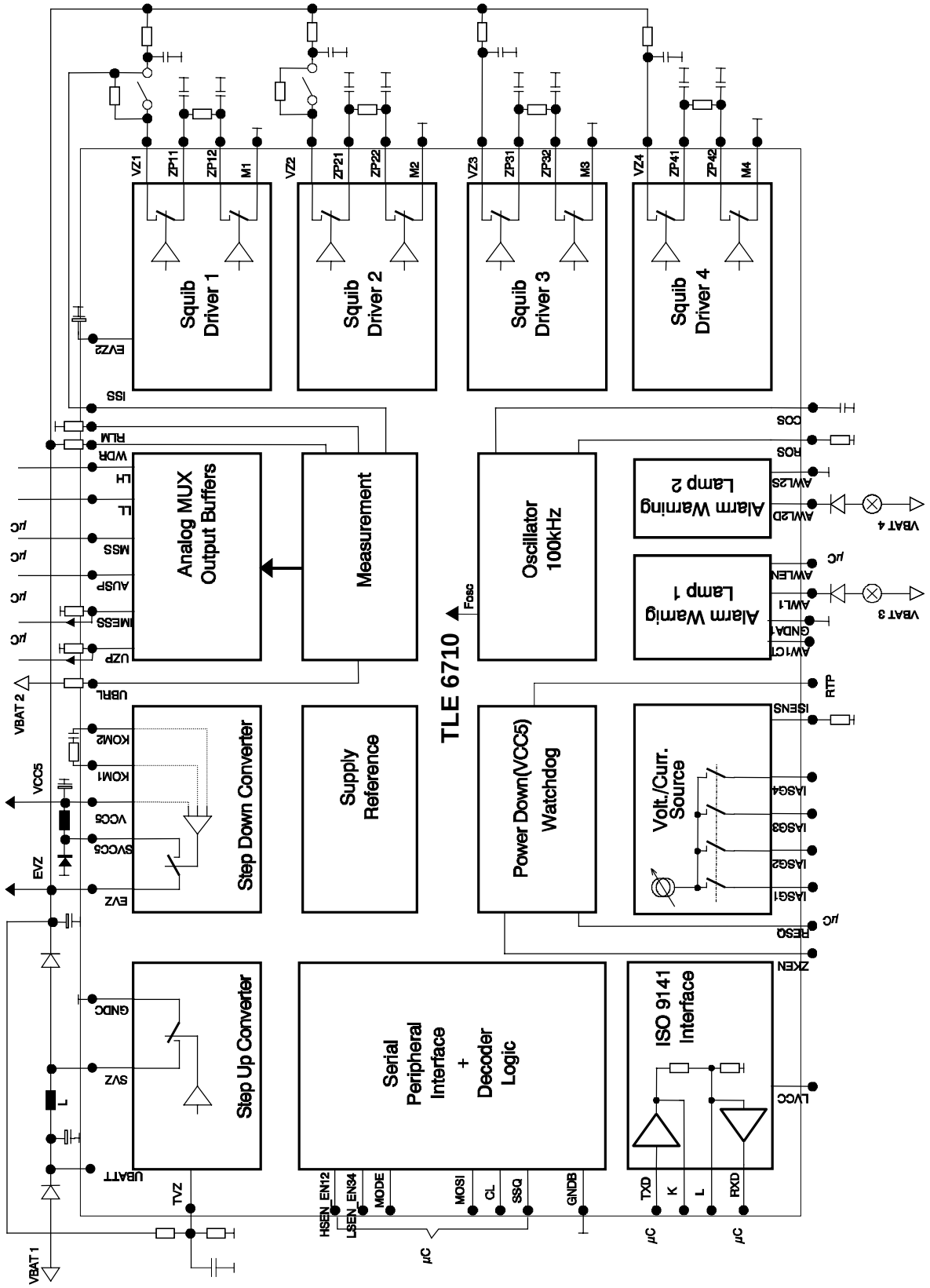
E. Pin Definitions and Functions

Pin No.	Symbol	Function
1	ISENS	Current measurement output of V/I-source for connection of an external resistor
2	KOM2	Frequency compensation capacitor terminal 2 for 5 V-buck converter
3	KOM1	Frequency compensation capacitor terminal 1 for 5 V-buck converter
4	UZP	Analogue measurement and diagnostic output 0...5V
5	COS	External capacitor (COS=1nF) for oscillator
6	ROS	External resistor (ROS=5kΩ) for oscillator
7	GNDB	Ground terminal for analogue functions and digital logic
8	SVCC5	The output of the buck converter (5V) is connected to an external inductance
9	EVZ2	Connection for external stabilization capacitor
10	EVZ	Boost Converter Output
11	SVZ	The input of the boost converter is connected to an external inductance (100 µH)
12	GNDC	Ground terminal for step-up and step-down-converter
13	RLM	Connection of external reference resistor for leakage current detection
14	TVZ	Feedback terminal of the boost converter regulation loop via an external resistive divider between EVZ and GNDC
15	VCC5	5V-supply terminal for feedback of the buck converter regulation loop and supply-input for all 5V-modules
16	IMESS	Connection of external reference resistor for firing circuit resistance measurement
17	VZ2	Buffered supply input voltage firing circuit 2
18	ZP21	Connection high-side-switch firing circuit 2
19	ZP22	Connection low-side-switch firing circuit 2
20	M2	Ground terminal for firing circuit2
21	RESQ	Open drain output for reset or power fail signal
22	AUSP	CMOS/TTL-level output of low supply voltage detection, low active
23	MSS	CMOS/TTL-output for detection of short of safing sensor
24	LH	CMOS-level output for squib leakage to battery or firing current 2 >1.75A
25	LL	CMOS-level output for squib leakage to ground or firing current 1 >1.75A
26	TXD	CMOS-level input for the Serial ISO 9141 Interface
27	RXD	CMOS-level output signal of the Serial ISO 9141 Interface
28	RTP	CMOS-level input for testing purposes (Watchdog functions)
29	M1	Ground terminal for firing circuit 1
30	ZP12	Connection low-side-switch firing circuit 1
31	ZP11	Connection high-side-switch firing circuit 1
32	VZ1	Buffered supply input voltage firing circuit 1

Pin Definitions and Functions (continued)

Pin No.	Symbol	Function
33	ISS	Detection input for short of safing sensor
34	WDR	Connection of external reference resistor to EVZ for resistance measurement
35	UBATT	Unregulated high voltage supply input
36	UBRL	UBATT supply voltage connection
37	AWL1	Output of the warning lamp
38	GNDA1	Ground terminal for AWL1
39	IASG1	Output of V/I-source 1
40	IASG2	Output of V/I-source 2
41	IASG3	Output of V/I-source 3
42	IASG4	Output of V/I-source 4
43	AWL2S	Source terminal for AWL2
44	AWL2D	Drain of AWL2 driver for general purpose
45	K	High-voltage open drain output of the serial interface
46	L	High-voltage input for the serial interface
47	LVCC	Input to program the L input to TTL-level, if connected to VCC5
48	AW1CT	Input, control pin for warning lamp 1, must be left open for self conductance
49	VZ3	Buffered supply input voltage firing circuit 3
50	ZP31	Connection high-side-switch firing circuit 3
51	ZP32	Connection low-side-switch firing circuit 3
52	M3	Ground terminal for firing circuit 3
53	**HSEN_EN12**	Logic-level input to enable the high-side switches (MODE0) or squibs 1 & 2 (MODE1)
54	**LSEN_EN34**	Logic-level input to enable the low-side switches (MODE0) or squibs 3 & 4 (MODE1)
55	AWLEN	Logic-level input to switch on the warning lamp
56	SSQ	Logic-level input to select SPI slave
57	CL	Logic-level clock input of SPI
58	MOSI	Logic-level master-out slave in input
59	**MODE**	Logic-level input for the mode definition (MODE0 or MODE1)
60	ZKEN	Logic-input/output open drain signal, enable firing HS- and LS-switch
61	M4	Ground terminal for firing circuit 4
62	ZP42	Connection low-side-switch firing circuit 4
63	ZP41	Connection high-side-switch firing circuit 4
64	VZ4	Buffered supply input voltage firing circuit 4

F. Block Diagram and Application Circuit



G. Absolute Maximum Ratings

Maximum ratings are absolute ratings; exceeding just one of these values may cause irreversible damage to the integrated circuit.
Maximum Ratings for junction temperature T_j from -40 to 150°C

No.	Parameter	Symbol	Limit Values			Unit
			min.	typ.	max.	
	Supply Pins					
1.1	Voltage	V_{UBATT}, V_{UBRL}, V_{SVZ}, V_{EVZ}, V_{VZ1},V_{VZ2},V_{VZ3}, V_{VZ4}, V_{AWL1}, V_{AWL2D}, V_{AWL2S}, V_{ISS}, V_{TVZ}	-0.3		40.0	V
		V_{SVCC5}	-1.2		40.0	V
		V_{EVZ2}	-0.3		44.0	V
		V_{VCC5}	-0.3		6.8	V
1.2	Current	I_{UBRL}	-30		3.0	mA
	Squib Driver Pins					
1.3	Voltage	V_{ZP11},V_{ZP12}, V_{ZP21}, V_{ZP22}, V_{ZP31},V_{ZP32}, V_{ZP41},V_{ZP42}	-0.3		40.0	V
1.4	Current (see diagram A for timing characteristics)	I_{ZP11}, I_{ZP12}, I_{ZP21}, I_{ZP22}, I_{ZP31}, I_{ZP32}, I_{ZP41}, I_{ZP42}			|4.0|	A
	Input-/ Output-Signal Pins					
1.5	Digital input voltages	V_{RTP}	-0.3		7.1	**V**
		V_{HSEN_EN12}, V_{LSEN_EN34}, V_{TXD}, V_{AWLEN}, V_{MOSI}, V_{CL}, V_{AW1CT}, V_{SSQ}, V_{MODE}	-0.3		V_{VCC5} +0.3	V
1.6	Digital input currents	I_{HSEN_EN12}, I_{LSEN_EN34}, I_{TXD}, I_{AWLEN},I_{MOSI}, I_{CL}, I_{RTP}, I_{AW1CT}, I_{SSQ}, I_{MODE}			|10.0|	mA
1.7	Digital output voltages	V_{RXD}, V_{AUSP},V_{RESQ}, V_{MSS}, V_{LL}, V_{LH}, V_{ZKEN}	-0.3		V_{VCC5} +0.3	V
1.8	Digital output currents	I_{RXD}, I_{AUSP}, I_{RESQ}, I_{MSS}, I_{LL}, I_{LH}, I_{ZKEN}			|10.0|	mA

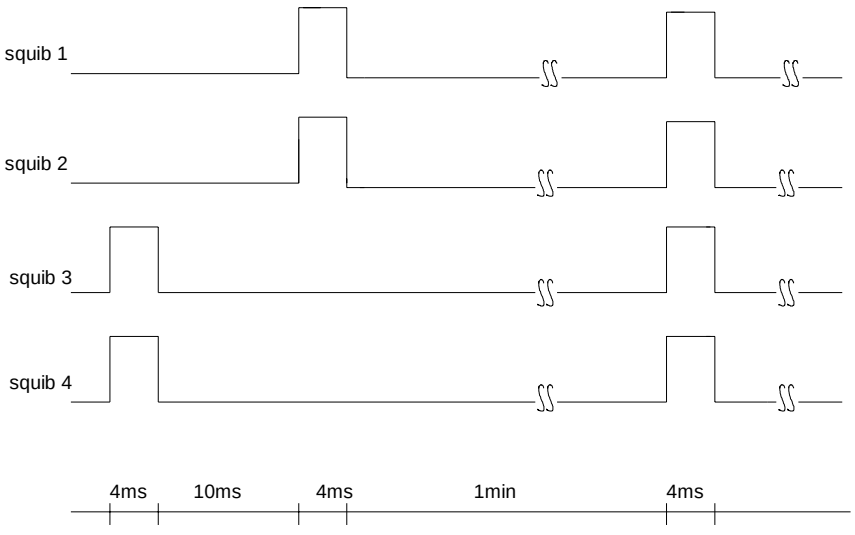
Absolute Maximum Ratings (continued)

No.	Parameter	Symbol	Limit Values			Unit
			min.	typ.	max.	
	Resistance Measurement Pins					
1.9	Current output for squib resistance	V_{IMESS}	-0.3		6.8	V
1.10	measurement	I_{IMESS}	-100.0		100.0	mA
1.10A	For On-time ton< 5ms	I_{IMESS}	-220.0		100.0	mA
1.11	Voltage output for squib resistance	V_{UZP}	-0.3		6.8	V
1.12	measurement	I_{UZP}	-10.0		10.0	mA
1.13	Reference input for squib resistance	V_{WDR}	-0.3		40.0	V
1.14	measurement	I_{WDR}	-100.0		100.0	mA
	Leakage Measurement Pins					
1.15	Input differential voltage	V_{ZPx1}-V_{ZPx2}	-40.0		40.0	V
1.16	Reference output for leakage resistance	V_{RLM}	-0.3		25.0	V
1.17	measurement	I_{RLM}	-10.0		10.0	mA
	ISO 9141 Interface Pins					
1.18	L input	V_L	-1.0		15	V
1.19		I_L	-2		2	mA
1.20	K output / input	V_K	-1		40	V
1.21		I_K	-100		100	mA
1.21.A	LVCC input voltage	V_{LVCC}	-0.3		6.8	V
	V/I-Source Pins					
1.22	IASGx voltage (x=1 to 4)	$V_{IASG1\ to\ 4}$	-0.6		40	V
1.23	ISENS output voltage	V_{ISENS}	-0,3		6.8	V
1.24	ISENS output current	I_{ISENS}	-6.0		6.0	mA
	Oscillator Pins					
1.25	ROS voltage	V_{ROS}	-0,3		6.8	V
1.26	ROS current	I_{ROS}	-300		300	µA
1.27	COS voltage	V_{COS}	-0.3		6.8	V
1.28	COS current	I_{COS}	-2		2	mA
	Compensation Pins					
1.29	KOM1, KOM2 voltage	V_{KOM1}, V_{KOM2}	-0,3		6.8	V

Absolute Maximum Ratings (continued)

No.	Parameter	Symbol	Limit Values			Unit
			min.	typ.	max.	
1.31	Squib Deployments Number of firings per squib driver and lifetime of the IC. Squib firing on / off timing characteristics see the following enclosed 'diagram A + B' cooling delay time between two cycles 1min.; load=2Ω	N_{max}			100	
	Temperatures					
1.32	Ambient temperature	ϑ_a	-40		90	°C
1.33	Storage temperature	ϑ_s	-55		150	°C
1.34	Junction temperature	ϑ_j	-40		150	°C
	Thermal Resistance					
1.35	Junction to ambient	R_{thja}			50 [1]	K/W
1.36	Junction to case	R_{thjc}			15	K/W
	ESD Classification					
1.37	Human Body Model (100pF/1.5kΩ)	$\pm V_{HBM}$	2000			V
1.38	Machine Model (200pF/0Ω)	$\pm V_{MM}$	200			V

1) Condition: Printed circuit board (epoxi), t = 1.5mm
Top side: copper connections to the pins (W_{CU} = 0.35mm, L_{CU} > 10mm)
Bottom side: Copper lattice (W_L = 5mm, W_{CU} = 1mm)



Squib firing on/off-timing characteristics

H. Functional Range

In the functional range the functions given in the circuit are fulfilled.
Deviations from the characteristics are possible.

T_j = -40 to + 125°C

No.	Parameter	Symbol	Limit Values			Unit	Condition
			min.	typ.	max.		
2.1	Voltage on pins UBATT, AWL1, AWL2D, AWL2S	V_{UBATT} V_{AWL1} V_{AWL2S} V_{AWL2D}	-0.3 -0.3		20 18	V V	
2.2	Voltage on pins UBATT, AWL1, AWL2D, AWL2S during jump start	V_{UBATT} V_{AWL1} V_{AWL2S} V_{AWL2D}			25	V	t ≤ 15 min lamps off
2.3	Voltage on pins UBATT, AWL1, AWL2D, AWL2S during load dump	V_{UBATT} V_{AWL1} V_{AWL2S} V_{AWL2D}			40	V	t ≤ 400ms lamps off
2.4	Rate of supply voltage rise	dV_{UBATT}/dt dV_{UBRL}/dt, dV_{EVZ}/dt, dV_{EVZ2}/dt, dV_{VZx}/dt, dV_{ZPxx}/dt, dV_{IASGx}/dt			30	V/µs	
2.5	Supply voltage EVZ	V_{EVZ}	4,5		33.0	V	
2.5.A	Supply voltage EVZ	V_{EVZ}			40.0	V	t ≤ 48 hours
2.6	Supply voltage EVZ2	V_{EVZ2}	10.0		44.0	V	
2.7	Supply voltage of squib drivers	V_{VZ1}, V_{VZ2}, V_{VZ3}, V_{VZ4}	6.0		40.0	V	
2.8	Supply voltage on pin VCC5	V_{VCC5}	4.8	5.0	6.2	V	
2.8 A	Voltage on digital I/O pins	$V_{digital\ I/O}$	-0.3		V_{VCC5}	V	
2.9	Reference input on pin UBRL for leakage measurement	V_{UBRL}	-0.3		40.0	V	t ≤ 400ms; ≤25V: t ≤ 15 min; ≤18V: continuous
2.10	Voltage on pin SVCC5	V_{SVCC5}	-0.6		40	V	I_{SVCC5} ≤ 600mA
2.10A	Voltage on pin SVZ	V_{SVZ}	-0.3		40	V	
2.11	Voltage on pin L	V_L	-0.3		6.8	V	
2.12	Voltage on pin K	V_K	-1.0		18	V	V_{UBATT} = V_{EVZ} = 8V
2.13	Voltage on pin ZPx1 (x=1,2,3,4)	V_{ZPx1}	-1.0		40	V	
2.14	Voltage on pin IASGx	V_{IASGx}	-0.6		18	V	
2.15	Voltage on pin IASGx	V_{IASGx}			25	V	t ≤ 15 min
2.16	Voltage on pin IASGx	V_{IASGx}			40	V	t ≤ 400ms
2.17	Lifetime	t_{lt}			15	years	
2.18	Operating time on battey Conditions: Tj = 90 °C Tj = 110 °C Tj = 125 °C Tj = 150 °C	t_{op}			10000 7000 4500 3000	h	

General Conditions for operating range:

1 Increasing or decreasing the supply voltages V_{VZ1}, V_{VZ2}, V_{VZ3}, V_{VZ4}, V_{EVZ}, V_{EVZ2},V_{UBATT}, V_{UBRL}, V_{WDR}, V_{VCC5} causes no incorrect firing of the squibs.

2 Loosing the connection to pin WDR or one of the squib driver supply voltages V_{VZ1}, V_{VZ2}, V_{VZ3}, or V_{VZ4}, has no influence to the other squib driver function.

3 During jump start and load dump conditions the IC must be able to fire the squibs

4 Squib failures like shorts to ground or battery must not have an influence to other chip functions

5 Maximum difference voltage of the squib connections: +/- (VZPx1 - VZPx2) = 40V

I. AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified supply voltage range and ambient temperature range.
Typical characteristics specify mean values expected over the production spread.
Currents into pins have positive values and vice-versa.
ATE tests will be performed with V_{EVZ}=33V, V_{VZx}=33V, unless otherwise specified under Test Condition.

Supply currents:

T_j = -40 to + 125°C, V_{UBATT}=**0** to 18V, V_{UBRL}=**0** to 18V

$V_{VZ1,2,3,4}$=6 to 33V, V_{EVZ}=15 to 33V, V_{EVZ2}=$V_{VZ1,2,3,4}$; V_{VCC5}=4.8 to 5.2V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
3.1	Supply current on pin UBATT	I_{UBATT}			1.5	mA	EVZ, VCC5 open
3.2	Quiescent current on pin VCC5	I_{VCC5}			1	mA	Regulators inactive
3.3	Current on pin VCC5	I_{VCC5}			1	mA	Regulators active, no diagnostic
3.3A	Current on pin VCC5	I_{VCC5}			2	mA	Regulators active, diagnostic ON [1)]
3.4	Operating current on pin EVZ	I_{EVZ}			6	mA	drivers off 30V regulator off, 5V regulator off, no diagnostic, V_{EVZ2}=open
3.4A	Operating current on pin EVZ	I_{EVZ}			6.5	mA	drivers on, oscill. on 30V regulator on, 5V regulator on, no diagnostic, V_{EVZ2}= V_{EVZ}=30V [1)]
3.5	Current on pin EVZ during squib leakage measurement	I_{EVZ}			15	mA	V_{EVZ2}=30V, V_{EVZ}=30V V_{UBATT}=18V, V_{VCC5}=4.8V, V_{TVZ}=2.2V; oscill. on I_{RLM}=1.5mA
3.6	Current on pin EVZ2	I_{EVZ2}	-3		-0.8	mA	V_{EVZ2}=0V, V_{EVZ}=30V drivers off
3.7	Current on pin EVZ2	I_{EVZ2}			850	µA	V_{EVZ2}=30V, V_{EVZ}≥8V V_{VCC5}=4.8V,drivers off
3.8	Current on pin EVZ2	I_{EVZ2}			500	µA	V_{EVZ2}=30V,V_{EVZ}≥20V all drivers on
3.8A	Current on pin EVZ2	I_{EVZ2}			350	µA	V_{EVZ2}=30V,V_{EVZ}≥20V squib drivers OFF [1)]
3.9	Quiescent currents on squib driver supply pins VZ2 to 4	I_{VZ2}, I_{VZ3}, I_{VZ4}	0		20	µA	drivers off, measurement off
3.10	Quiescent current on squib driver supply pin VZ1	I_{VZ1}	0		60	µA	driver off, measurement off
3.10 A	Additional current on pins EVZ2, VZx, UBATT, UBRL	I_{VZ1}	0		150	µA	pin voltage measurem. ON / OFF
3.11	Voltage difference between pins EVZ and EVZ2	V_{EVZ} - V_{EVZ2}	0.3		0.9	V	drivers off, squibs off, V_{EVZ}=30V, I_{EVZ2}=-500µA

1) Guaranteed by design

AC/DC Characteristics (continued)

Logic Inputs and Outputs:

Inputs: HSEN_EN12, LSEN_EN34, TXD, AWLEN, MOSI, CL, SSQ, ZKEN, RTP, MODE

Outputs: RXD, AUSP, RESQ, MSS, ZKEN, LL, LH

T_j = -40 to + 125°C, V_{VCC5}=4.8 to 5.2V, V_{EVZ}=15 to 33V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
4.1	Input voltage - high level	V_{IH}	2.4			V	
4.2	Input voltage - low level	V_{IL}			0.8	V	
4.3	Input hysteresis	ΔV_I	20		200	mV	
4.4	Input pull-up resistance internal to VCC5 on pins: SSQ, TXD LSEN_EN34	R_{IU}	16		48	kΩ	V_{VCC5} = 5 V, V_I = 0 V V_{MODE} = 0 V (MODE0)
4.4A	Input pull-up resistance internal to VCC5 on pin: MOSI	R_{IU_MOSI}	40	100	260	kΩ	V_{VCC5} = 5 V, V_I = 0 V
4.5	Input pull-down resistor internal to ground on pins: HSEN_EN12, AWLEN, RTP, MODE LSEN_EN34	R_{ID}	16		48	kΩ	V_I = 5 V V_{MODE} = 5 V (MODE1)
4.6	Output voltage - low level	V_{OL}	0		0.4		V_{VCC5} = 5 V, V_{EVZ} = 8 V, I_{OUT} = 1 mA
4.7	Output current - high level; only pin ZKEN	I_{OH}	-220		-50	µA	V_{VCC5} = 5 V, V_{EVZ} = 8 V, V_{OUT}= 0 V
4.7A	Output current - high level; only pin RESQ	I_{OH}	-440		-100	µA	V_{VCC5} = 5 V, V_{EVZ} = 8 V, V_{OUT}= 0 V
4.8	Output voltage - high level; except pins RESQ, ZKEN, LL, LH	V_{OH}	2.8		V_{VCC5}	V	V_{VCC5} = 5 V, I_{OUT} = -200 µA
4.8A	Output voltage - high level; only pins LL and LH	V_{OH}	2.8		V_{VCC5}	V	V_{VCC5} = 5 V, I_{OUT} = -100 µA
4.11	Input voltage - high level for pin AW1CT	V_{IH}	4.2			V	
4.12	Input voltage - low level for pin AW1CT	V_{IL}			0.8	V	

AC/DC Characteristics (continued)

Low Battery Detection on pin UBATT (EVZ):

T_j = -40 to + 125°C, V_{EVZ} = 4,5 to 33 V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
5.1	Threshold voltage on pin UBATT reported to pin AUSP	V_{UBATT}	4.10		4.60	V	V_{UBATT} decreases V_{VCC5} > 4.7 V 1)
5.2	Hysteresis	ΔV_{UBATT}	130		250	mV	2)
5.3	Threshold voltage on pin EVZ to start the boost converter	V_{EVZ}			4.5	V	V_{EVZ} increases $V_{UBATT} \geq$ 4.6 V

1) Output AUSP is low active and follows the input UBATT.
The internal signal of AUSP enables the boost converter, so the regulator will not work, if V_{UBATT} is less than the value of Spec 5.1.

2) Not tested. Guaranteed by design. If V_{EVZ} is less than the threshold value of Spec 5.3, the converters will stop to operate

Oscillator for Boost (30V)-, Buck (5V)-Converter and Watchdog

T_j = -40 to + 125°C, V_{EVZ} = 8 to 33 V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
6.1	Frequency	f_{OS}	89	1)	103	kHz	V_{UBATT} = 12 V; C_{COS} = 1 nF; R_{ROS} = 4.99 kΩ
6.2	Voltage on pin ROS	V_{ROS}	1.176	1.2	1.224	V	R_{ROS} = 5 kΩ
6.2A	Current on pin ROS	I_{ROS}		-240		µA	R_{ROS} = 5 kΩ 2)
6.3	Current on pin COS	I_{COS}		-140		µA	R_{ROS} = 5 kΩ $V_{COS} \leq$ 0.5 V
6.3A	Current ratio of pin COS to pin ROS	I_{COS} / I_{ROS}		-7/12			R_{ROS} = 5 kΩ $V_{COS} \leq$ 0.5 V
6.4	Current on pin COS	I_{COS}		+840		µA	R_{ROS} = 5 kΩ $V_{COS} \geq$ 1.9 V
6.4A	Current ratio of pin COS to pin ROS	I_{COS} / I_{ROS}		7/2			R_{ROS} = 5 kΩ $V_{COS} \geq$ 1.9 V
6.5	Difference of sawtooth thresholds (PSTV - VSTV)	ΔV_{COS}		1.2		V	C_{COS} = 1 nF, R_{ROS} = 5 kΩ

Application information: Oscillator starts running at $V_{EVZ} \geq$ 4.5 V

1) Application Note: Formula for fos: fos = [1/(2 x CCOS x RROS) +/-5%] + foffset
foffset depends on the layout of the application board. Correlation between reference Board and the real application boards need to be performed with 'golden devices TLE 6710'.
Recommendation for RROS: 4.87kΩ to 5.23kΩ nominal value+/- tolerance and +/- temperature depend.
Formula for fos Reference Board measurement: fos = fRESQ x 12800

2) IROS = VROS / RROS

AC/DC Characteristics (continued)

Boost Converter (30V):

T_j = -40 to + 125°C, V_{UBATT} = 4.75 to 20 V, V_{EVZ} = 5 to 33 V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
7.1	Switching current limiting	I_{SVZ}	650		950	mA	V_{UBATT} = 6 V; V_{TVZ} = 0 V; V_{SVCC5} open; V_{VCC5} open;
7.2	Switching saturation voltage	V_{SVZ}			1	V	I_{SVZ} = 450 mA; V_{UBATT} = 6 V; V_{TVZ} = 0 V; $V_{EVZ} \geq$ 18 V V_{SVCC5} open; V_{VCC5} open
7.2A	Switching on resistance	$Ron_{SVZ-GNDC}$			2.2	Ω	I_{SVZ} = 450 mA; V_{UBATT} = 6 V; V_{TVZ} = 0 V; $V_{EVZ} \geq$ 18 V V_{SVCC5} open; V_{VCC5} open
7.3	Max. switch duty cycle	D_{30max}	85		90	%	$I_{SVZ} \geq$ 10 mA; $V_{EVZ} \geq$ 18 V;
7.4	Min. switch duty cycle	D_{30min}			0	%	
7.5	Switch on time via pin COS	t_{on30}	0.2		0.8	µs	I_{SVZ} = 300 mA; V_{UBATT} = 6 V; V_{TVZ} = 0 V; $V_{EVZ} \geq$ 18 V V_{COS} = 2.0 to 0.5V; sample: 0.1xV_{SVZmax}
7.6	Switch on slope via pin COS	s_{on30}	-250		-50	V/µs	see: 7.5 1) sample: 0.1xV_{SVZmax} and 0.9xV_{SVZmax}
7.7	Switch off time via pin COS	t_{off30}	0.3		1.5	µs	I_{SVZ} = 300 mA; V_{UBATT} = 6 V; V_{TVZ} = 0 V; $V_{EVZ} \geq$ 18 V V_{COS} = 0.5 to 2.0V; sample: 0.9xV_{SVZmax}
7.8	Switch off slope via pin COS	s_{off30}	100		280	V/µs	see: 7.7 1) sample: 0.1xV_{SVZmax} and 0.9xV_{SVZmax}

1) Not tested. Guaranteed by design.

AC/DC Characteristics (continued)

Boost Converter (30V): (continued)

T_j = -40 to + 125°C, V_{UBATT} = 5.25 to 18 V, V_{EVZ} = 5 to 33 V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
7.9	Overcurrent switch off time	$t_{offCL30}$	0.08		0.5	µs	V_{UBATT} = 6 V; V_{TVZ} = 0 V; $V_{EVZ} \geq$ 18 V R_{load} = 1 Ω; V_{load} = 12V; sample: 0.9xV_{SVZmax}
7.10	Overvoltage on pin EVZ for switch off the regulator	V_{EVZ}	33.5		39.5	V	
	Error Amplifier						
7.11	Input offset voltage	ΔV_{EAVZ}	-40		40	mV	1)
7.12	DC open loop gain	A_{OLVZ}	34		70	dB	1)
7.12A	Unity-Gain bandwidth	f_U	1.3		2	MHz	1)
7.12B	Gain at f = 100 kHz	A_{100}	18			dB	1)
	Reference						
7.13	Reference voltage	V_{VR}	2.75	2.8	2.85	V	1), 2)
7.14	Reference voltage	V_{VR}	2.52	2.8	3.08	V	V_{EVZ}=33.5 to 40V 1), 2), 3)
7.15	Leakage current on pin TVZ	I_{TVZ}	-2		1.5	µA	V_{TVZ}=2.52 to 3.08V
	SVZ Output						
7.16	Switch **on** threshold via TVZ	V_{TVZ}	2.65	2.8		V	
7.17	Switch **off** threshold via TVZ	V_{TVZ}		2.8	2.95	V	6)

	Application characteristics (see: Application Circuit)						
7.A	Output voltage range (adjusted by an external divider)	V_{EVZ}	16		30	V	V_{TVZ} = 2.8 V
7.B	Output voltage accuracy for one determined V_{EVZ} via TVZ-divider resistors.	a_{EVZ}	0.95x V_{EVZ}		1.05x V_{EVZ}	V	regulator on at: VTVZ = 2.65 V; regulator off at: VTVZ = 2.95 V 5)
7.C	Output power	P_{EVZ}			0.6	W	V_{VCC5} = 5.5 V; SVCC5 open

1) Error Amplifier characteristics of the packaged device cannot be measured, but are guaranteed by design. The reference voltage is measured only on wafer.

2) Reference is supplied only via pin EVZ.

3) No uncontrolled reset on pin RESQ is allowed, due to higher supply voltage V_{EVZ}.

5) Accuracy of the external resistive TVZ-divider from EVZ to GNDB: 0%

6) If the voltage on pin TVZ reaches 33V for a max. duration of 10 sec and returns to 2.8V (typ. value), the regulator must operate as specified.

AC/DC Characteristics (continued)

Buck Converter (5V):

T_j = -40 to + 125°C, V_{EVZ} = 8 to 33 V, V_{UBATT} = 5.25 to 18 V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
8.1	Output current limit	I_{SVCC5}	-600		-250	mA	
8.2	Switch saturation voltage	V_{EVZ} - V_{SVCC5}			3.9	V	V_{EVZ} = 18 V ≤ V_{EVZ2}; V_{TVZ} = 3 V; I_{SVCC5}=-300mA; 47Ω to Gnd SVZ open, VCC5<4.6 V
8.3	Switch saturation voltage	V_{EVZ} - V_{SVCC5}			3.5	V	V_{EVZ} = 8.5 V ≤ V_{EVZ2}; V_{TVZ} = 3 V; I_{SVCC5} = -30 mA; SVZ open; VCC5<4.6 V
8.3A	Switch saturation voltage	V_{EVZ} - V_{SVCC5}			1.5	V	V_{EVZ} = 18 V; V_{EVZ2} = 26 V; V_{TVZ} = 3 V; I_{SVCC5}=-300mA; SVZ open, VCC5<4.6 V
8.4	Switch on time via pin COS	t_{on5}	0.2		0.8	µs	I_{SVCC5} = -300 mA; V_{TVZ} = 3 V; V_{EVZ} ≥ 18 V; V_{COS} = 0.5 to 2.0V; sample: 0.5x$V_{SWITCHmax}$
8.5	Switch on slope via pin COS	s_{on5}	40		100	V/µs	see: 8.4 1) sample: 0.75x$V_{SWITCHmax}$ and 0.5x$V_{SWITCHmax}$
8.6	Switch off time via pin KOM1	t_{off5}	0.8		2.5	µs	I_{SVCC5} = -300 mA; V_{TVZ} = 3 V; V_{EVZ} ≥ 18 V; V_{VCC5} = 4.7V V_{KOM1} = 0 to 3V; sample: 0.5x$V_{SWITCHmax}$
8.7	Switch off slope via pin KOM1	s_{off5}	-700		-100	V/µs	see: 8.6 1) sample: 0.75x$V_{SWITCHmax}$ and 0.5x$V_{SWITCHmax}$

1) Not tested. Guaranteed by design.

AC/DC Characteristics (continued)

Buck Converter (5V): (continued)

T_j = -40 to + 125°C, V_{EVZ} = 8 to 33 V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
8.8	Overcurrent switch off time	t_{offCL5}	**0.05**		0.8	µs	V_{VCC5} = 0V; V_{TVZ} = 3V; $V_{EVZ} \geq$ 18 V; R_{load} = 47Ω; sample: 0.5x$V_{SWITCHmax}$
8.9	Switch on time via pin TVZ	t_{onVZ5}	10		150	µs	I_{SVCC5} = -300 mA; $V_{EVZ} \geq$ 18 V; V_{TVZ} = 0 to 5 V; sample: 0.5x$V_{SWITCHmax}$
8.10	Switch off time via pin TVZ	t_{offVZ5}	0.2		1	µs	I_{SVCC5} = -300 mA; $V_{EVZ} \geq$ 18 V; V_{TVZ} = 5 to 0 V; sample: 0.5x$V_{SWITCHmax}$
8.10A	Switch off time due to an overvoltage on pin VCC5	$t_{offVCC5}$	0.2		1.5	µs	I_{SVCC5} = -300 mA; $V_{EVZ} \geq$ 18 V; V_{TVZ} = 3V; V_{KOM1} = 0V; V_{VCC5} = 4.8V to 6.1V; sample: 0.5x$V_{SWITCHmax}$
8.10B	Overvoltage switch off threshold on pin VCC5	$V_{offVCC5}$	5.3		6.1	V	$V_{KOM2} \geq$ 2 V; 1)
8.11	Switch on threshold voltage via pin TVZ	V_{TVZ}	1.51	1.70	1.85	V	(54..66%) 2)
8.12	Switch off threshold voltage via pin TVZ	V_{TVZ}	0.1	0.2	0.3	V	(4..11%)
	Error Amplifier						
8.13	Input offset voltage	ΔV_{EAVCC}	-10		+10	mV	1)
8.14	DC open loop gain	A_{OLVCC}	60			dB	1)
8.15	Unity-Gain bandwidth	f_U	2			MHz	1)
8.16	Gain at f = 100 kHz	A_{100}	26			dB	1)
8.17	Output voltage LOW on pin KOM2	V_{KOM2}			0.4	V	I_{KOM2} = 20 µA; V_{KOM1} = 3V
8.18	Output voltage HIGH on pin KOM2	V_{KOM2}	2.5			V	I_{KOM2} = -500 µA; V_{KOM1} = 0V
	Reference see No. 7.13: Reference of the 30 V Step-up Regulator						
	SVCC5 Output						
8.19	Switch **on** threshold via pin VCC5	V_{VCC5}	4.85	5.0		V	I_{SVCC5} = 30mA
8.20	Switch **off** threshold via pin VCC5	V_{VCC5}		5.0	5.15	V	I_{SVCC5} = 30mA

1) Not tested. Guaranteed by design.
2) The switching of the output transistor will ´be delayed by 10 to 150 us after reaching the threshold voltage.

AC/DC Characteristics (continued)

Buck Converter (5V): (continued)

T_j = -40 to + 125°C, V_{EVZ} = 8 to 33 V

	Application characteristics (see: Application Circuit)						
8.A	Output voltage	V_{VCC5}	4.85		5.15	V	$I_{VCC5\,L}$ = 30mA T_a = 25°C V_{EVZ} = 30 V
8.B	Output voltage	V_{VCC5}	4.8		5.2	V	I_{VCC5L} = 10 to 60 mA $V_{EVZ} \geq$ 18 V
8.C	Output voltage	V_{VCC5}	4.8		5.2	V	I_{VCC5L} = 10 to 33 mA $V_{EVZ} \geq$ 8.5 V
8.D	Output power	P_{VCC5L}			0.3	W	

I_{VCC5L} ..... is the symbol for the output current of the buck converter output.
P_{VCC5L}..... is the symbol for the output power of the buck converter output.

Power On Reset of VCC5 & EVZ and Watchdog:

T_j = -40 to + 125°C, V_{EVZ} = 8 to 33 V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
9.1	Power-on reset, RESQ = H	V_{VCC5}	4.75			V	V_{EVZ} = 8 to 40 V
9.2	Power-down reset, RESQ = L	V_{VCC5}	2.0		4.50	V	
9.2A	Power-down reset threshold level for RESQ high to low transition	V_{EVZ}	7		8.5	V	VEVZ decreasing; VVCC5 > 4.75V
9.3	Power down reset delay time	t_{rdel}	10		150	µs	V_{VCC5} decreases to 4 V
9.4	Watchdog period (determined by oscillator frequency divider)	T_{WD}	128		128	$\frac{100}{f_{OS}}$	$V_{VCC5} \geq$ 4.7 V
9.5	Start of reset (after watchdog time-out)	t_{sr}	64		64	$\frac{100}{f_{OS}}$	$V_{VCC5} \geq$ 4.7 V
9.6	Reset duration (after watchdog time-out)	t_{rd}	64		64	$\frac{100}{f_{OS}}$	$V_{VCC5} \geq$ 4.7 V
9.7	Trigger window duration	t_{twd}	1		32	$\frac{100}{f_{OS}}$	$V_{VCC5} \geq$ 4.7 V
9.7A	Trigger window duration without SPI triggering	t_{twdmax}	32		32	$\frac{100}{f_{OS}}$	$V_{VCC5} \geq$ 4.7 V
9.8	Start of trigger window	t_{ts}	32		32	$\frac{100}{f_{OS}}$	$V_{VCC5} \geq$ 4.7 V
9.9	Power-up reset extension	t_{pu}	64		65	$\frac{100}{f_{OS}}$	$V_{VCC5} \geq$ 4.7 V

Note: Reset threshold voltage is derivated from the reference for VCC5, so there is a linear function of the absolute value of VCC5. Power down reset: A hysteresis is included by design, but will not be tested. Logic functions and diagrams as defined in circuit description of chapter 'Watchdog'.
If the pin RTP is 'High' and pin AW1CT is grounded (test mode B), the units for tests No. 9.4 to 9.9 are 4/fos instead of 100/fos.

AC/DC Characteristics (continued)

ISO 9141 - Serial Interface:

T_j = -40 to + 125°C, V_{UBATT} = 8 to 18 V, V_{EVZ} = 8 to 33 V, $V_{VCC5} \geq 4.55V$

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
10.1	Output voltage on pin K	V_K			1.4	V	I_K = 30 mA
10.2	Output voltage on pin K	V_K			1	V	I_K = 30 mA at 25°C
10.3	L pin input threshold low	V_L			0.13x V_{UBATT}	V	V_K=0V, V_{LVCC}=open
10.4	L pin input threshold high	V_L	0.19x V_{UBATT}			V	V_K=0V, V_{LVCC}=open
10.5	L pin hysteresis	ΔV_L	30		150	mV	V_K=0V, V_{LVCC}=open 1)
10.6	L pin input threshold (logic level) 'low level'	V_L			2	V	V_K=0V, V_{LVCC}=V_{VCC5}
10.7	L pin input threshold (logic level) 'high level'	V_L	3			V	V_K=0V, V_{LVCC}=V_{VCC5}
10.8	K pin input treshold low (to pin RXD)	V_K			0.35x V_{UBATT}	*V*	L = open
10.9	K pin input treshold high (to pin RXD)	V_K	0.70x V_{UBATT}			*V*	L = open
10.10	K pin input current	I_K	-12		12	µA	V_{UBATT}=0V; V_K=18V; V_{EVZ}=0V; V_{VCC5}=0V
10.10A	K pin input current	I_K	-12		12	µA	V_K=18V; V_{EVZ}=0V; V_{VCC5}=0V
10.10B	K pin input current	I_K	-12		12	µA	V_K=18V; V_{TXD}=0V; $V_{VCC5} \leq 2V$
10.11	K pin input current	I_K	-12		12	µA	V_{UBATT}=18V; V_K=0V; VTXD=VVCC5 or open
10.12	K pin input current	I_K	-12		12	µA	V_K = V_{UBATT} - 1V; VTXD=VVCC5 or open
10.12A	K pin input current	I_K	-12		12	µA	V_{VCC5} = 0V or open; V_K=18V
10.12B	K pin input peak current	I_K			1	mA	$dV_K / dt \leq 10$ V/µs; VTXD=VVCC5 or open 1)
10.13	L pin input current	I_L	0		60	µA	V_L = 6 V; V_K=0V or open
10.14	Short-circuit current	I_K	35		100	mA	max. 5 ms
10.15	Rise time delay TXD to K	t_{Kr}	1		4	µs	Sample point: 0.5 x V_{Kmax} 2)
10.16	Fall time delay TXD to K	t_{Kf}	0.5		3	µs	Sample point: 0.5 x V_{Kmax} 2)
10.17	Rise time delay L to RXD	t_{RXDr}	0.2		2	µs	Sample point: 0.5 x V_{RXD}
10.18	Fall time delay L to RXD	t_{RXDf}	0.1		1	µs	Sample point: 0.5 x V_{RXD}
10.19	Rise time delay K to RXD	t_{K_RXDr}	0.2		2	µs	Sample point: 0.5 x V_{RXD} 3)
10.20	Fall time delay K to RXD	t_{K_RXDf}	0.1		2	µs	Sample point: 0.5 x V_{RXD} 3)

1) Not tested. Guaranteed by design.
2) With 500 R external pull-up to battery and 10 nF to GND for test purposes only.
3) Not tested. Guaranteed by design. Pin L is not connected.

If the pin K operates within the maximum ratings (-1V to +40V), all other circuit blocks must work as defined by the specification. This function is not tested, but it is guaranteed by design.

The allowed current into pin L is -0.3 to 2.0 mA. At I_L = 1mA the voltage $V_L \geq 7.0V$

AC/DC Characteristics (continued)

Alarm Warning Lamp Driver (AWL1):

T_j = -40 to + 125°C, V_{EVZ} = 8 to 33 V

No.	Parameter	Symbol	Limit Values min.	typ.	max	Unit	Test Condition
11.1	Output voltage	V_{AWL1}		2	3.2	V	I_{AWL1} = 300mA 1) V_{EVZ} = 0 V
11.2	Output voltage	V_{AWL1}			0.6	V	I_{AWL1} = 300mA 1), 4)
11.3	AWL1 leakage current	I_{AWL1}	0		150	µA	V_{AWL1} = 17.5 V, off; AWL1 measurement on
11.4	AWL1 leakage current	I_{AWL1}	0		50	µA	V_{AWL1} = 17.5 V, off; AWL1 measurement off
11.4 A	AWL1 reverse voltage	V_{AWL1}			-0.2	V	I_{AWL1} = -100 µA V_{GNDA1} = 0 V
11.5	Output current limit static	I_{AWL1}	400		650	mA	V_{AWL1} = 4 V
11.6	Temperature limitation (current will be reduced)	T_{AWL1}		150	170	°C	AWL1 switch is on; V_{AWL1} > 2 V 2)
11.7	Temperature limitation	T_{AWL1}	130			°C	V_{AWL1} > 2 V 2)
11.8	AWL1 Voltage to UZP output voltage ratio	V_{AWL1}/V_{UZP}	-5%	5	+5%	V/V	selection via SPI: UAWL1 $V_{AWL1} \leq V_{EVZ}$-6V
11.9	Current threshold for open load detection	I_{AWL1}	10		35	mA	selection via SPI: IAWL1 detection on pin UZP
11.10	Voltage on pin UZP for open load	V_{UZP}	0		0.4	V	selection via SPI for lamp on and current measurement I_{AAWL1} < 10 mA
11.11	Voltage on pin UZP for standard load	V_{UZP}	1.5		V_{VCC5}	V	selection via SPI for lamp on and current measurement I_{AWL1} > 30 mA
11.12	Current on pin AW1CT	I_{AW1CT}	-20		0	µA	V_{AW1CT}=0V and 5V, V_{AWL1}=12V 3)

1) If $V_{AAWL} \geq$ 25 V, the warning lamp driver can not be switched on. This feature prevents a reduction of warning lamp lifetime.

2) Limit values are guaranteed by design. The logic function is tested only on wafer.
In case of a short circuit from an external voltage source (=12V) to pin AWL1 and voltage on pin UBATT is 0V, the chip will be warmed up to a temperature limitation value of approximately 150 °C. Proposal: Continuous operation with temperature limitation is not recommended. If a start up of the voltage on pin UBATT (4.5 to 18V) occurs immediately, following functions have to operate:
a. Bandgap-Reference, Oscillator, Boost- and Buck-Converter;
b. Generation of signal RESQ to 'high';
c. SPI command transfer for 1. trigger; 2. measurement of chip temperature
3. measurement of AWL1 voltage; 4. switch OFF lamp 1

3) Pin AW1CT could be connected to VCC5 or be open for default ON operation. For default OFF operation pin AW1CT has to be shorted; the maximum value of the external short circuit resistor to ground is 10kΩ.

- No active clamping circuitry is included in the device.
- During start up the AWL1 lamp driver is **ON** if AW1CT is left open. It can be switched off if all three conditions are applied: 1. RESQ = 'HIGH'; 2. AWLEN = 'HIGH'; 3. SPI: SAWL1D
- During start up the AWL1 lamp driver is **OFF** if AW1CT is connected to ground. It can be switched on if all following conditions occur: 1. RESQ = 'HIGH'; 2. AWLEN = 'HIGH'; 3. SPI: SAWL1D
- AWL1 lamp driver can be switched on/off by the SPI-command SAWL1B/SAWL1D (lamp 'bright' /'dark') according to the state of AW1CT.

4) At the maximum voltage of 0.6V and a current of 300mA the maximum ON-resistance is Rds(on)max = 2Ω.

AC/DC Characteristics (continued)

Alarm Warning Lamp and Multifunction Driver 2 (AWL2):

T_j = -40 to + 125°C, V_{EVZ} = 8 to 33 V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max		
12.1	Output Voltage (used as low side switch)	V_{AWL2D}			0.6	V	V_{AWL2S} = 0 V 2) I_{AWL2} = 200mA
12.2	Drain Source Saturation Voltage (used as high side switch) $V_{DS} = V_{AWL2D} - V_{AWL2S}$	V_{DS}			1.0	V	$V_{EVZ} > V_{AWL2D}$ + 6 V I_{AWL2} = 200mA
12.3	AWL2 leakage current	I_{AWL2}	0		20	µA	V_{AWL2} = 17.5 V lamp off, AWL2 measurement off
12.4	AWL2 leakage current	I_{AWL2}	0		150	µA	V_{AWL2D} = 17.5 V V_{AWL2S} = 0 V lamp off, AWL2 measurement on
12.4 A	AWL2 reverse voltage	V_{AWL2}			-0.2	V	I_{AWL2D} = -100 µA V_{AWL2S} = 0 V
12.5	Output current limit static	I_{AWL2}	250	400	600	mA	$V_{DS} \geq$ 3V
12.6	Over-Temperature shut down	T_{AWL2}	150		190	°C	AWL2 power-switch turns off; 1)
12.7	Voltage on pin UZP after over-temperature shut down	V_{UZP}		1.45		V	SPI: MTEMP $(9XXX)_H$ T = 25°C 1)
12.8	AWL2D Voltage to UZP output voltage ratio	V_{AWL2D}/V_{UZP}	-5%	5	+5%	V/V	selection via SPI: UAWL2D $V_{AWL2D} \leq V_{EVZ}$-6V
12.9	AWL2S Voltage to UZP output voltage ratio	V_{AWL2S}/V_{UZP}	-5%	5	+5%	V/V	selection via SPI: UAWL2S $V_{AWL2S} \leq V_{EVZ}$-6V

1) Limit values are guaranteed by design. Logic function is tested only on wafer.
Activating 'Average Chip Temperature' measurement, the typical temperature coefficient of the voltage on pin UZP after over temperature shut down is -4mV/K

No active clamping circuitry is included in the device.
If the AWL2 lamp driver is used as a high side switch to drive an inductive load, an external free-wheeling diode in parallel with the load must be used.

AWL2 lamp driver only can be switched on by the SPI-command SAWL2B (lamp 'bright' or on)

AWL2 lamp driver only can be switched off by the SPI-command SAWL2D (lamp 'dark' or off)

2) At the maximum voltage of 0.6V and a current of 200mA the maximum ON-resistance is: Rds(on)max = 3Ω.

AC/DC Characteristics (continued)

Voltage-/ Current-Sources (V/I):

T_j = -40 to + 125°C, V_{VCC5} = 4.8 to 5.2 V, V_{EVZ} = 18 to 33 V; x=1,2,3,4

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
13.1	Operating current on pin IASGx	I_{IASGx}	-20		-1	mA	t_{on}≤5 ms
13.2	Current limitation on pin IASGx	I_{IASGx}	-80		-25	mA	t_{on}≤5 ms, V_{ISENS} = 0V, V_{IASGx} = 0V
13.2A	Current limitation on pin IASGx	I_{IASGx}	-32		-24	mA	t_{on}≤5 ms, R_{ISENS}=2kΩ V_{IASGx} = 0V
13.3	Output voltage 1 on pin IASGx	V_{IASGx}	-7%	2.8	+3%	V	R_{IASGx} ≤ 100kΩ I_{IASGx} = -1 to -20 mA I_{IASGx} = -0.5 mA 2) SPI: $(2XXX)_H$
13.4	Difference of output voltage 2 (5V) and output voltage 1 (2.8V) on pin IASGx	ΔV_{IASGx}	-5%	2.2	+5%	V	R_{IASGx} ≤ 100kΩ I_{IASGx} = -1 to -20 mA I_{IASGx} = -0.5 mA 2) SPI: $(BXXX)_H$
13.6	Current ratio accuracy I_{ISENS} / I_{IASG}	I_{IASGx}/ I_{ISENS}	-5% 0%	10	7% 15%		I_{IASG}= -1 mA to -20mA I_{IASG}= -0.5 mA to -1mA 1), 2)
13.7	Voltage on pin ISENS for IASG-current limit	V_{ISENS}	V_{VCC5}		V_{VCC5} +0.6	V	R_{ISENS}≤20 kΩ, V_{IASGx} = 0V
13.8	Voltage on pin ISENS	V_{ISENS}			V_{VCC5} +0.8	V	R_{ISENS} open, V_{IASGx}=0V
13.9	ISENS offset current	I_{ISENS}	-2		2	µA	V_{ISENS}=0V, 2) measurement inactive
13.9A	ISENS offset current	I_{ISENS}	-2		2	µA	V_{ISENS}=V_{VCC5} - 0.3V, 2) measurement inactive
13.9B	ISENS offset current	I_{ISENS}	-2		2	µA	pin IASGx open, 2) V_{ISENS}=0V, measurement active
13.10	Voltage ratio V_{UZP} / V_{ISENS}	V_{UZP} / V_{ISENS}	-5%	1.0	+5%		SPI: SELx V_{ISENS}=0.4V to V_{VCC5} - 0.3V
13.11	Settling time on pin UZP for one measurement	t_{UZP}			50	µs	Starting with SPI command, ending at 90% of the final value on pin UZP
13.12	IASGx leakage current	I_{IASGx}	-2		2	µA	V_{IASGx}=0V and 5V; 2) measurement inactive

1) Current ratio accuracy calculation: $a_{ISENS} = (10 \times \frac{I_{ISENS}}{I_{IASGx}} - 1) \times 100\%$

Current ratio calculation: $\frac{I_{IASGx}}{I_{ISENS}} = \frac{1000}{100 + a_{ISENS}}$

2) After characterization guaranteed by design.

If the pin IASGx is open or shorted to ground, no latch-up or oscillation may occur (R_{ISENS} ≤ 20kΩ).

AC/DC Characteristics (continued)

Squib Driver: Highside:A)

T_j = -40 to + 150°C, $V_{VZ1,2,3,4}$=6 to 33V, V_{EVZ}=8.5 to 33V, $V_{EVZ2} \geq V_{VZx}$ + 6V, V_{VCC5}=4.8 to 5.2V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
14.1	Saturation voltage of switch x=1,2,3,4	$V_{VZx-ZPx1}$		1.75	2.0	V	V_{EVZ} = V_{EVZ2} = 21V, 1) V_{VZx}=12V, -I_{ZPx1}=1.75A
14.2	Output current limitation of switch x=1,2,3,4	I_{ZPx1}	-3.5		-2.25	A	V_{EVZ} = V_{EVZ2} = 21V, $V_{VZx - ZPx1} \geq$4V
14.2 A	Clamping voltage on pin Zpx1 during firing (x=1,2,3,4)	V_{ZPx1}	24		27	V	I_{ZPx1}= value of Spec. 15.3 and 15.4 2)
14.3	Switch off time delay of switch x=1,2,3,4	t_{off}	0.1		5	µsec	R_{load}= 2.2Ω
14.4	Switch on time delay of switch x=1,2,3,4	t_{on}	1		20	µsec	V_{EVZ} = V_{EVZ2} = 33V, $R_{ZPx1\ to}$ +18V = 2.2Ω, V_{VZx} = 33V (I=0.23A) Trigger V_{ZPx1}=18.5V
14.5	Switch on time delay of switch x=1,2,3,4	t_{on}	1		35	µsec	V_{EVZ} = V_{EVZ2} = 33V, $R_{ZPx1\ to}$ +18V = 2.2Ω, V_{VZx} = 33V (I=2A) Trigger V_{ZPx1}=22.4V
14.6	Over temperature limitation	T	180		300	°C	not tested 2)

A) The limits are valid for a switch on duration of 4ms and a firing on- / off- timing characteristics as descript in chapter 'Absolute Maximum Ratings'.
From one squib output ZPx1 a short to ground or a connection to the automotive supply voltage VBAT has no influence to other squib drivers, and vice versa.

1) The maximum saturation voltage V_{VZx} - V_{ZPx1} = 2.6 V is guaranteed by design.
The test conditions are V_{EVZ} = V_{EVZ2} = 15 V, V_{VZx} = 12V, -I_{ZPx1} = 1.75 A

2) Guaranteed by design

Squib Driver: Lowside:A)

T_j = -40 to + 150°C, $V_{VZ1,2,3,4}$=6 to 33V, V_{EVZ}=8.5 to 33V, $V_{EVZ2} \geq V_{VZx}$ + 6V, V_{VCC5}=4.8 to 5.2V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
15.1	Saturation voltage of switch x=1,2,3,4	V_{ZPx2}		1.65	1.85	V	V_{EVZ} = V_{EVZ2} = 21V, I_{ZPx2} = 1.75A
15.2	Driver current detection of switch x (x=1 to LL, x=2 to LH)	$I_{ZPx2det}$	1.75	2.0	2.25	A	$V_{ZPx2} \geq$4V 2)
15.3	Output current limitation of switch x=1,2	$I_{ZPx2lim}$	$I_{ZPx2det}$ +0.25		I_{ZPx2de} +0.75	A	$V_{ZPx2} \geq$4V 3)
15.4	Output current limitation of switch x= 3,4	$I_{ZPx2lim}$	$I_{ZPx2det}$ +0.25		I_{ZPx2de} +0.75	A	$V_{ZPx2} \geq$4V

A) The limits are valid for a switch on duration of 4ms and a firing on- / off- timing characteristics as descript in chapter 'Absolute Maximum Ratings'. From one squib output ZPx1 a short to ground or a connection to the automotive supply voltage VBAT has no influence to other squib drivers, and vice versa.

2) The hysteresis of the driver current detection is typically 50 mA.

3) The value of the current limitation is always greater than the value of the current detection.

AC/DC Characteristics (continued)

Squib Driver: Lowside (continued):

T_j = -40 to + 150°C, $V_{VZ1,2,3,4}$=6 to 33V, V_{EVZ}=**8.5** to 33V, V_{VCC5}=4.8 to 5.2V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
15.4 A	Switch off time delay of switch x=1,2,3,4	t_{off}	0.1		5	µsec	R_{load}= 2.2Ω
15.5	Switch on time delay of switch x=1,2,3,4	t_{on}	3		20	µsec	R_{load} = 2.2Ω, V_{load} = 12V (I=0.23A) Trigger V_{ZPx2}=11.5V
15.6	Switch on time delay of switch x=1,2,3,4	t_{on}	5		35	µsec	R_{load}= 2.2Ω, V_{load}= 12V (I=2A) Trigger V_{ZPx2}=7.6V
15.7	Over temperature limitation	T	180		300	°C	not tested, guaranteed by design
	Outputs LL and LH for Firing Current Detection:						
15.8	Voltage on pin LL	V_{LL}			0.8	V	I_{ZP12}>1.75A
15.9	Voltage on pin LH	V_{LH}			0.8	V	I_{ZP22}>1.75A
15.10	Response time to LL or LH if the squib current will be interrupted	t_{LL}, t_{LH}	1		3	1/f_{OS}	I_{ZP12}>1.75A to pin LL I_{ZP22}>1.75A to pin LH f_{OS} = frequency of the oscillator
15.11	Delay time to LL or LH if the firing current exceeds the value of Spec.No. 15.2	t_{LLon}, t_{LHoff}	10		40	µs	R_{squib} = 2.2Ω V_{load} = 8V t_o = signal SSQ from low to high

Note: The timing measurements of No. 14.3, 14.4, 14.5, 15.4A, 15.5 and 15.6 will be started either with the rising edge of SSQ or a transition of HSEN_EN12 / LSEN_EN34 and stopped by the voltage transition (50%) on ZPx1 or ZPx2.

Squib Driver: Highside and Lowside:

T_j = -40 to + 150°C, $V_{VZ1,2,3,4}$=6 to 33V, V_{EVZ}=**8.5** to 33V, V_{VCC5}=4.8 to 5.2V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
15.13	Total sum of saturation voltages of high and lowside switches x=1,2,3,4 of No.: 14.1 and 15.1	V_{VZx} - V_{ZPx1} + V_{ZPx2}			3.0	V	see test conditions for specification 14.1 and 15.1 I_{ZPx} = 1.75A [2]
15.14	Total absorbed energy of one high side switch	W_{HS}			120	mJ	starting temperature: ≤ 85°C Squib firing on / off timing see: Max. Rat. and No. 1.31 [1]
15.15	Total absorbed energy of one low side switch	W_{LS}			140	mJ	starting temperature: ≤ 85°C Squib firing on / off timing see: Max. Rat. and No. 1.31 [1]

1) W_{HS} = I_{ZPx1} x (V_{VZx} - V_{ZPx1}) x ton W_{LS} = I_{ZPx2} x V_{ZPx2} x ton

2) On-Resistance of high and low side switches together:
Ron [T=Tabs] = 1.71Ω x {1 - 3.65 E-3 x (150°C - Tabs)} Tabs ... temperature in °C
ATE-testing for 14.1, 15.1 and 15.13 will be performed at maximum 125°C, however with guard bands.

AC/DC Characteristics (continued)

Squib Resistance Measurement:

T_j = -40 to + 125°C, V_{EVZ}=15 to 33V, V_{VCC5}=4.8 to 5.2V

No.	Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Condition
	Basic reference current:						
16.1	Basic current on pin IMESS	I_{IMESS}	-6.2		-4.8	mA	SPI: $(4XXX)_H$ 5) R_{ROS}=5.0kΩ ± 0.1%
	Measurement current reference input WDR:						
16.2	Operating voltage range on pin Zpx1, if the switch between pin WDR and pin Zpx1 is closed	V_{ZPx1}	0		V_{EVZ}-6	V	I_{WDR} = 55mA SPI: $(6XXX)_H$
16.3	On resistance between pin WDR and pin ZPx1	$R_{WDR-ZPx1}$	8		30	Ω	I_{WDR} = 40mA 3) SPI: $(6XXX)_H$
16.3A	On resistance between pin WDR and pin ZPx1	$R_{WDR-ZPx1}$	10		40	Ω	I_{WDR} = 5mA 3) V_{EVZ} = 30V, V_{ZPx1} = 25V, SPI: $(6XXX)_H$
16.4	Current on pin WDR	I_{WDR}			60.0	mA	squib resistance <3Ω
16.4A	Short circuit current on pin WDR	I_{WDR}	60		200	mA	V_{WDR} = V_{EVZ} = 30V, V_{ZPx1} = 0V
	Measurement current output IMESS:						
16.5	Linear voltage range for measurement on pin IMESS	V_{IMESS}	0		V_{VCC5}	V	I_{WDR} ≤ 55mA, SPI: $(6XXX)_H$
16.5A	Clamping voltage on pin IMESS	V_{IMESS}	V_{VCC5}		V_{VCC5} + 0.6	V	R_{IMESS} ≥ V_{VCC5} / 60mA 4)
16.6	Leakage current on pin IMESS (measurement inactive)	I_{IMESS}	-10.0		0	µA	V_{ZPx2} =33V (x=1,2,3,4)
16.7	Current difference of the basic reference current on pin IMESS between I_{ZPx2} (x=1,2,3,4) and -I_{IMESS}	ΔI_1	-0.2		0.2	%	SPI: $(4XXX)_H$, 4) V_{IMESS} = 4.8V, 1) I_{ZPx2} = 0 and 55mA
16.8	Current difference of the basic reference current on pin IMESS between I_{WDR} and -I_{IMESS} (measurement of channel 1 to 4 active)	ΔI_{IMESS}	0		60	µA	1. SPI: $(4XXX)_H$, 2. SPI: $(6XXX)_H$ with pin WDR = open and squibs connected V_{IMESS} = 4.8V 4)
16.9	Current difference of the basic reference current on pin IMESS between I_{WDR} and -I_{IMESS} (measurement of channel 1 to 4 active)	ΔI_2	-0.2		0.2	%	SPI: $(6XXX)_H$ 4) V_{IMESS} = 4.8V, 2) I_{WDR} = 0 and 55mA, squibs connected

1) $\Delta I_1 = \frac{(I_{IMESS2} - I_{IMESS1}) - 55mA}{55mA} \times 100$ (I_{IMESS2}: at I_{ZPx2}=55mA, I_{IMESS1}: at I_{ZPx2}=0mA)

After characterization the values will be guaranteed by design.

2) $\Delta I_2 = \frac{(I_{IMESS2} - I_{IMESS1}) - 55mA}{55mA} \times 100$ (I_{IMESS2}: at I_{WDR}=55mA, I_{IMESS1}: at I_{WDR}=0mA)

After characterization the values will be guaranteed by design.

3) Typical temperature dependence of the ON-resistance: $R_{on\ 125\ °C} = 2.5 \times R_{on\ -40\ °C}$

4) Garanteed by design.

5) $I_{IMESS} = (V_{ROS} / R_{ROS}) \times 275 / 12$ (± 8 %) V_{ROS} specified under No. 6.2

AC/DC Characteristics (continued)

Squib Resistance Measurement: (continued)

T_j = -40 to + 125°C, V_{EVZ}=15 to 33V, V_{VCC5}=4.8 to 5.2V, x=1,2,3,4

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	UZP Voltage Output for Resistance Measurement:						
16.10	Voltage on pin UZP (measurement active)	V_{UZP}	0.0		V_{VCC5} + 0.6	V	
16.10 A	Voltage on pin UZP (gain = **10** amplifier active)	V_{UZP}	0.85 x V_{VCC5}		0.93 x V_{VCC5}	V	$V_{ZPx1} = V_{ZPx2}$
16.10 B	Voltage on pin UZP (gain = **30** amplifier active)	V_{UZP}	0.85x V_{VCC5}		0.95 x V_{VCC5}	V	$V_{ZPx1} = V_{ZPx2}$
16.11	Voltage on pin UZP (measurement inactive)	V_{UZP}	0.0		30	mV	
16.12	Current on pin UZP (measurement active)	I_{UZP}	-3.0		-1.0	mA	V_{ZPx1}-V_{ZPx2} = 0V V_{UZP} = 0V
16.13	internal pull down resistor on pin UZP (measurement inactive)	R_{UZP}	30		80	kΩ	V_{UZP} = 3V
	Measurement amplifier	**(gain = 10)**					0), 1), 2)
16.14	Voltage gain	a_{10}	9.90		10.30		V_{ZPX1}-V_{ZPX2}=400mV $V_{CM} = V_{ZPX2} \pm 0.4V$, the value of V_{ZPX2} is the actual measurement result of No. 16.21
16.18	Common mode rejection ratio	$CMRR_{10}$	45			dB	$V_{CM} = V_{ZPX2} \pm 0.4V$, the value of V_{ZPX2} is the actual measurement result of No. 16.21 3)
	Measurement amplifier	**(gain = 30)**					0), 1), 2)
16.19	Voltage gain	a_{30}	29.0		32.0		V_{ZPX1}-V_{ZPX2}=140mV $V_{CM} = V_{ZPX2} \pm 0.4V$, the value of V_{ZPX2} is the actual measurement result of No. 16.21
16.20	Common mode rejection ratio	$CMRR_{30}$	50			dB	$V_{CM} = V_{ZPX2} \pm 0.4V$, the value of V_{ZPX2} is the actual measurement result of No. 16.21 3)

0) The 'Gain-10-Amplifier' measurements will be done between pin UZP (as an output) and pins ZP_{x1} , ZP_{x2} (as differential inputs).

1) From one squib output ZP11 / ZP12 (or ZP21 / ZP22, ZP31 / ZP32, ZP41 / ZP42) a short to ground or a connection to the automotive supply voltage VBAT has no influence to the other squib resistance measurement function and vice-versa.

2) A squib difference voltage > 0.4 V has no influence to the other squib resistance measurement function and vice-versa. In this case the output voltage on pin UZP will be set to values as specified under No. 16.10.

3) $CMRR = 20 \times \log(a_x \times \Delta V_{ZPx2} / \Delta V_{UZP})$

AC/DC Characteristics (continued)

Squib Resistance Measurement: (continued)

T_j = -40 to + 125°C, V_{EVZ}=15 to 33V, V_{VCC5}=4.8 to 5.2V, x=1,2,3,4

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	Pins ZP12, ZP22,ZP32, ZP42 voltage regulator						
16.21	Regulated voltage on pins ZPx2	V_{ZPx2}	7.5		8.5	V	V_{IMESS} = 4.8V I_{IMESS} = -5.0mA to -60mA
16.22	Voltage difference of the regulated voltage on pins ZPx2	ΔV_{ZPx2}			100	mV	1. SPI: $(4XXX)_H$; 2. SPI: $(6XXX)_H$ with I_{WDR} = 55mA, squibs connected, V_{IMESS} = 4.8V
16.23	Current limit on pin IMESS	I_{IMESS}	-220		-65	mA	V_{ZPx2} =40V, R_{IMESS} = 0Ω activated by SPI ton < 5ms
	Settling Time						
16.24	Total settling time on pin UZP	t_{UZP}	5		200	µs	I_{IMESS} = -5.0 to -60mA for 90% of the final value on pin UZP no capacitance on pins ZPx initial V_{ZPx} to 0...33V
	Pin IMESS Voltage Measurement Amplifier (gain = 2)						1)
16.25	Voltage gain	a_2	1.90		2.25		V_{IMESS} = 340mV to 1V
16.25 A	Voltage gain	a_2	1.95		2.05		V_{IMESS} = 1V to 2.5V
16.26	Input offset voltage	Vos			20	mV	2)

1) The 'Gain-2-Amplifier' measurements will be done between pin UZP (as an output) and pin IMESS (as input).

2) Will be guaranteed by design after characterization. (Vos = V_{UZP}/2 - V_{IMESS})

AC/DC Characteristics (continued)

Squib Leakage Measurement:

T_j = -40 to + 125°C, V_{EVZ}=15 to 33V, V_{VCC5}=4.8 to 5.2V; V_{UBRL}=5.25V to 20 V, (¾ x V_{UBRL})+2.5V ≤ V_{EVZ}

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	Outputs LL and LH for Leakage Measurement:						
17.1	Voltage on pin LL	V_{LL}			0.8	V	leakage to ground V_{ZPx1} < 1 / 4 x V_{UBRL} V_{ZPx1} is decreasing
17.2	Voltage on pin LH	V_{LH}			0.8	V	leakage to battey V_{ZPx1} > 3 / 4 x V_{UBRL} V_{ZPx1} is increasing
	Reference output RLM:						
17.3	Output voltage on pin RLM	V_{RLM}	0.31x V_{UBRL}		0.35 x V_{UBRL}	V	R_{RLM} = 2k to 20kΩ, I_{RLM}=-0.2 to -3.5mA
17.4	Output current on pin RLM during measurement	I_{RLM}	-3.5		0	mA	stable state
17.5	Dynamic output voltage on pin RLM	V_{RLM}	0.2 x V_{UBRL}		0.46x V_{UBRL}	V	R_{RLM} = 220Ω V_{UBRL} = 6V
17.6	Dynamic output current capability on pin RLM	I_{RLM}			-6.0	mA	R_{RLM} = 220Ω V_{UBRL} = 6V
17.7	Current ratio of pin RLM to pin ZPx1	$\lvert I_{RLM}/I_{ZPx1} \rvert$	0.9		1.1		stable state, I_{RLM} = -3.5mA
17.8	Current ratio of pin RLM to pins ZPx1	$\lvert I_{RLM}/I_{ZPx1} \rvert$	0.75		1.25		dynamic state, I_{RLM} = -6mA
17.9	Resistance ratio of resistor on pin RLM to leakage resistance	R_{RLM}/R_{leak}		4/3			
	Leakage detection voltages:						
17.10	Leakage low threshold voltage	V_{ZPx1}	-5%	1/4 x V_{UBRL}	5%	V	leakage to ground V_{ZPx1} is decreasing target: V_{LL} = 'low'
17.11	Leakage high threshold voltage	V_{ZPx1}	-5%	3/4 x V_{UBRL}	5%	V	leakage to battery V_{ZPx1} is increasing target: V_{LH} = 'low'
17.12	Leakage detection hysteresis	ΔV_{ZPx1}	-20%	1/48 x V_{UBRL}	20%	V	leakage to ground or leakage to battery
	Reference input UBRL:						
17.13	Internal resistor at pin UBRL	R_{UBRL}	35		150	kΩ	V_{UBRL} < 24V
	Settling time						
17.14	Total settling time on pins LL or LH	t_{LL} t_{LH}			50	µs	I_{RLM} = -0.5 mA no capacitance on pins ZPx1 and ZPx2 initialise: V_{ZPx2} = 0 to 33V
17.15	LL output response after Squib **Low** Side Switch activation via LSEN	t_{dLL}			30	µs	no external leakage
17.16	LH output response after Squib **High** Side Switch activation via HSEN	t_{dLH}			30	µs	no external leakage

Note: The pin RLM is protected against a short circuit to ground during leakage measurement (ton ≤ 400ms). In this case the minimum expected current I_{RLM} ≥ -100mA and $\lvert I_{ZPx1} \rvert$ ≤ 100mA.

AC/DC Characteristics (continued)

Internal Dummy Squib Resistance:

T_j = -40 to + 125°C; V_{EVZ}=15 to 33V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	Squib outputs:						
18.1	Leakage current of switch x=1,2,3,4	I_{ZPx}	-20.0		20.0	µA	switch off; ZPx1=ZPx2 V_{VZx}=33V V_{ZPx}=16,5V
18.1 A	Leakage current of switch x=1,2,3,4	I_{ZPx}	-20.0		20.0	µA	switch off; ZPx1=ZPx2 V_{VZx}=33V V_{ZPx}=**0**V
18.2	Internal dummy resistor from ZPx1 to ZPx2 (x=1,2,3,4)	$R_{ZPx1-ZPx2}$	10		50	kΩ	no firing or measure V_{ZPx1}-V_{ZPx2} = 20V, V_{ZPx1}-V_{ZPx2} ≤ V_{EVZ}

Supply Voltage Measurements:

T_j = -40 to + 125°C, V_{VCC5}=4.8 to 5.2V; $V_{VZ1,2,3,4}$=6 to 33V, V_{EVZ}=V_{EVZ2}=15 to 33V, V_{UBATT}=V_{UBRL}=6 to 18 V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	UZP Voltage Output for Supply Voltage Measurements:						
19.1	Voltage on pin UZP (measurement inactive)	V_{UZP}	0.0		30	mV	
19.2	Voltage on pin UZP (measurement active)	V_{UZP}	0		V_{VCC5} +0.6	V	
19.3	UBATT Voltage to UZP output voltage ratio	V_{UBATT}/V_{UZP}	-5%	5	5%		selection via SPI: MUB1 V_{UBATT} ≤ V_{EVZ}-6V
19.4	UBRL Voltage to UZP output voltage ratio	V_{UBRL}/V_{UZP}	-5%	5	5%		selection via SPI: MUB2 V_{UBRL} ≤ V_{EVZ}-6V
19.5	EVZ Voltage to UZP output voltage ratio	V_{EVZ} / V_{UZP}	-5%	8	5%		selection via SPI: MEVZ1 V_{EVZ} ≥ +6V
19.6	EVZ2 Voltage to UZP output voltage ratio	V_{EVZ2} / V_{UZP}	-5%	8	5%		selection via SPI: MEVZ2 V_{EVZ2} ≥ +6V
19.7	VZx Voltage to UZP output voltage ratio (x=1,2,3,4)	V_{VZx} / V_{UZP}	-5%	8	5%		selection via SPI: MVZx V_{VZx} ≥ +6V
19.8	Total settling time on pin UZP	t_{UZPM}			200	µs	for 90% of the final value on pin UZP
19.9	Reference Voltage on UZP pin	V_{UZP}	-7%	2.8	+7%	V	selection via SPI: REF; $(AAAA)_H$
19.10	ZPx1 Voltage to UZP output voltage ratio	V_{ZPx1}/V_{UZP}	-5%	5	5%		selection via SPI: MZPx V_{ZPx1} ≤ V_{EVZ}-6V

AC/DC Characteristics (continued)

Detection of Safing Sensor Closure:

T_j = -40 to + 125°C, V_{VCC5}=4.8 to 5.2V;

V_{VZ1}=6 to 40V, V_{EVZ}=V_{EVZ2}=15 to 40V, V_{UBATT}=V_{UBRL}=6 to 18 V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
20.1	Threshold voltage on pin ISS for the choice between LS - and HS - detection	V_{ISS}	V_{VCC5} + 0.6	V_{VCC5} + 1.2	V_{VCC5} + 1.8	V	V_{MSS}='low', V_{ISS} decreases, $V_{VZ1} \geq V_{ISS}$-0.3V **$V_{EVZ} \geq 5V$**
	High Side Detection:						
20.2	Threshold voltage of difference between pins ISS and VZ1	V_{ISS}-V_{VZ1}	0.3	0.4	0.6	V	V_{MSS}='low', V_{ISS}-V_{VZ1} increases
20.3	Threshold voltage of difference between pins ISS and VZ1 in case of firing	V_{ISS}-V_{VZ1}	2.0	2.3	2.5		
20.4	Hysteresis of difference between pins ISS and VZ1	Δ(V_{ISS} - V_{VZ1})	10		150	mV	0)
	Low Side Detection:						
20.4A	Threshold voltage on pin ISS	V_{ISS}	V_{VCC5}/2 - 0.1	V_{VCC5}/2	V_{VCC5}/2 + 0.1	V	V_{MSS}='high', V_{ISS} decreases
20.4B	Time limit for V_{ISS} < threshold for time prolonguation on pin MSS	t_{ISSMIN}	0.5		1	$\frac{100}{f_{OS}}$	2)
20.4C	V_{MSS} time prolonguation (starting from V_{ISS} exceeding threshold)	t_{SUM}	97		97.5	$\frac{100}{f_{OS}}$	2)
20.4D	Time limit for a valid retrigger for V_{ISS} > threshold	t_{RTRIG}	0.5			$\frac{100}{f_{OS}}$	2)
	Current source from pin VZ1 to ground:						
20.5	Current on pin VZ1	I_{VZ1}	1.2	1)	6	mA	R_{ROS}=5kΩ selection via SPI: SMSSH
20.6	Current on pin ISS	I_{ISS}			50	µA	NO firing
20.7	Current on pin ISS	I_{ISS}			200	µA	Firing active

0) Guaranteed by design.

1) $$I_{VZ1min,max} = 15 \times \frac{V_{ROS}}{R_{ROS}} \times (1 \pm 0.6)$$

2) Accelerated testing can be performed by the test mode C, described in the chapter 'Watchdog Operation and Generation of the Squib Driver Enable Signal ZKEN'.
If the pin RTP is set to V_{VCC5} + 2 x Vdiode, the units for 20.4B, 20.4C, 20.4 D are 4/fos instead of 100/fos.

AC/DC Characteristics (continued)

Average Chip Temperature Measurement:

T_j = -40 to + 150°C, V_{EVZ}=15 to 33V, V_{VCC5}=4.8 to 5.2V

No.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
21.1	Voltage on pin UZP	V_{UZP}	2.7	1)	3.1	V	T = 25 °C; R_{ROS}=5kΩ, SPI: MTMP $(9XXX)_H$
21.2	Temperature coefficient of the voltage on pin UZP	dV_{UZP}/dT	-7.5		-6.0	mV/K	SPI: MTMP $(9XXX)_H$

1) Calculation of the voltage on pin UZP at T = 25 °C depending on the value of the resistor on pin ROS:

$$V_{UZP} = 2.9V + 4 \times 26mV \times \ln\frac{5\ k\Omega}{R_{ROS}} \quad (\pm 7\%)$$

J. Serial Peripheral Interface (SPI)

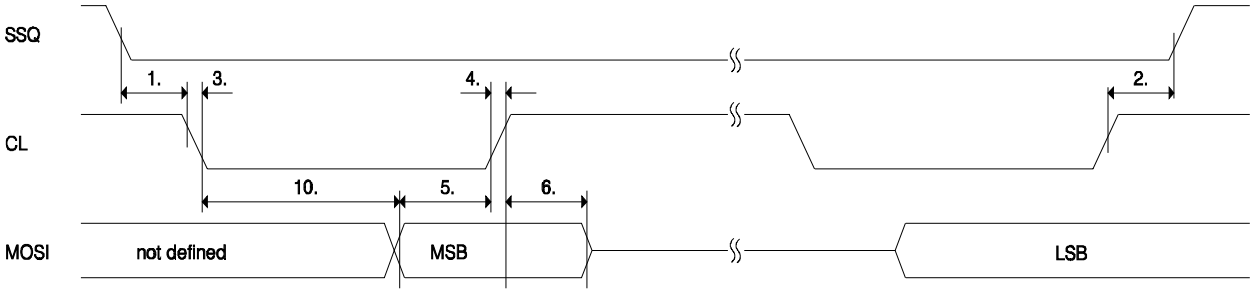
J.1: SPI Timing Characteristics:

T_j = -40 to + 125°C, V_{VCC5}=4.8 to 5.2V;

No.	Parameter	Symbol	Limit Values			Unit
			min.	typ.	max.	
22.1	SSQ Lead Time	**t**lead	40			ns
22.2	SSQ Lag Time	**t**lag	100			ns
22.3	Fall Time for SSQ, CL, MOSI	**t**f			25	ns
22.4	Rise Time for SSQ, CL, MOSI	**t**r			25	ns
22.5	MOSI Data Setup Time	**t**SU	40			ns
22.6	MOSI Data Hold Time	**t**h	40			ns
22.10	MOSI Data Valid Time 2)	**t**v			120	ns
22.12	Clock frequency	**f**CL	0		4	MHz

Note : All timing is shown with respect to 20% and 70% of VVCC5.

2) Parameter No.: 22.10 is necessary, if 68HC11 is used.
TLE 6710 function is independent of this parameter.



SPI Timing

J.2: SPI Commands:

J.2.1: General Information on SPI Command Structure:

The TLE 6710 hardware can be configured as MODE0- or MODE1. With a ‘low’ or ‘open’ on pin MODE, after start up the system works in the MODE0-default mode and decodes SPI instruction commands. A MODE1 operation requires an initializing SPI ‘Mode command’ (FExx)H and a ‘high’ on pin MODE before starting with SPI instructions like diagnostic, control or firing commands. If the software and hardware settings for the mode definition do not fit together, then the transmission of all SPI-commands will be prevented.
All functions e.g. 'Firing' or 'Measurement' are controlled by a 16 bit instruction command. The 16 bit word consists of two bytes (8 bit) and will be decoded by the decoder logic circuit of the TLE 6710 and latched for some functions.
After a Watchdog activated 'reset' all internal control registers and decoded signals are reset to its inactive default value.

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB

Function Byte: a0: indicates valid control command
a1..a3 control bits
a4..a7 SPI command bits

Selection Byte b0..b1 channel select
b2..b3 function select, firing and test commands
b4..b6 switch or measurement select
b7 not used except firing and test commands
in case of firing command: b0..b7 selects the squib driver transistors, all combinations are allowed.

If RESQ=0 is generated, then the SPI-control register is reset to its inactive default value. All commands will be interrupted.
Default states:

1. MODE0 (pin MODE = 0 or open)
2. all squib drivers off,
3. all measurements off
4. Lamp Driver 1(AWL1) depends on AW1CT.
   See table in the description ‘Alarm Warning Lamp Driver (AWL1)
5. Lamp Driver 2 (AWL2) is off
6. Watchdog Trigger signal is low,
7. Safing Sensor Closure Detection: Current source to ground = 0mA

J.2.2: Summary of SPI Commands:

Code (hex)	Name	Short Description
0000	NOMEAS	Deactivate all measurements, no change of latched status via control command (J.2.9)
0xxx	CTRL	Control Commands for Lamps, Watchdog and Safing Sensor Detection (only if used as a stand alone command!!)
1xxx	MSUPL	Supply Voltage and Lamp Measurement Command, Squib Leakage Measurement with squib switches in OFF state
2xxx	VIM28	V/I-Sources Command; Set IASGx (x=1,2,3,4) voltage source to low voltage: 2.8 V
3xxx	MFSUP	Firing Voltage Measurement Command
4xxx	RES5	Resistance measurement 'reference current' active (5mA)
5555	OSC	100kHz Test Mode Command
6xxx	RES40	Resistance measurement 'main current' active (defined on WDR Pin) and 'reference current' active (5mA)
7xxx	RES5H	Resistance measurement with 'activated high side-switch and 'reference current' active (5mA)
8xxx	FIRE	Firing Command
9xxx	MTEMP	Temperature measurement
AAAA	REF	2.8V Reference Test Mode Command
Bxxx	VIM5	V/I-Sources Command; Set IASGx (x=1,2,3,4) voltage source to high voltage: 5.0 V
Cxxx	MSQL	Squib Leakage Measurement Command with one of eight squib switches in ON state
Dxxx		This command could be reserved for future purposes
Exxx		not used
FExx	MODE3	Latch Command for the MODE1. First command after start up. Pin MODE must be 'high' during transmission
FFFF	RESET	Reset by SPI Command. Deactivate all measurements. Reset all latched control commands (J.2.9) to it's default state. Does not change the MODE1 to MODE0!

J.2.3: Firing Commands: $(8XXX)_H$

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB
1	**0**	**0**	**0**	x	x	x	x	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

b7 = 1: High-Side-Switch of squib 4 active
b6 = 1: High-Side-Switch of squib 3 active
b5 = 1: High-Side-Switch of squib 2 active
b4 = 1: High-Side-Switch of squib 1 active

b3 = 1: Low-Side-Switch of squib 4 active
b2 = 1: Low-Side-Switch of squib 3 active
b1 = 1: Low-Side-Switch of squib 2 active
b0 = 1: Low-Side-Switch of squib 1 active

Also more than one switch can be activated, all combinations may be allowed.

Hardware requirements depending on MODE0- or MODE1

Mode	MODE	ZKEN	ZKEN_int	HSEN_EN12	LSEN_EN34	Function
MODE0	0	1	1	1	0	$(8xxx)_H$: firing of HSx and / or LSx
MODE1	1	1	1	1	0	$(8xxx)_H$: firing of squib 1 and 2
MODE1	1	1	1	0	1	$(8xxx)_H$: firing of squib 3 and 4
MODE1	1	1	1	1	1	$(8xxx)_H$: firing of squibs 1 to 4

For MODE1 operation an initializing SPI 'Mode command' needs to be sent once after start up. If RESQ = 0 is generated, then the measurement will be interrupted and the ASIC will return to it's default state of the MODE0. A soft reset $(FFFF)_H$ does not change the mode.

J.2.4: Squib Resistance Measurement-, Squib Voltage Measurement- and IMESS-pin Voltage Measurement Commands:

Resistance measurement 'reference current' active (5.5 mA)

(4XXX)$_H$

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB
0	**1**	**0**	**0**	x	x	x	x	X	x	x	x	**0/1**	**0/1**	0/1	0/1

Resistance measurement 'main current' active (defined on pin WDR) and 'reference current' active (5.5 mA)

(6XXX)$_H$

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB
0	**1**	**1**	**0**	x	x	x	x	x	x	x	x	**0/1**	**0/1**	0/1	0/1

Resistance measurement 'activated high side-switch' (current defined on pin VZx) and 'reference current' active (5.5 mA)

(7XXX)$_H$

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB
0	**1**	**1**	**1**	x	x	x	x	x	x	x	x	**0/1**	**0/1**	0/1	0/1

b0..b1 : Channel select

b1	b0	channel select
0	0	Channel 1
0	1	Channel 2
1	0	Channel 3
1	1	Channel 4

b2..b3 : Selection of the functions on pin UZP

b3	b2	additional functions select		
0	0	Gain **10** Amplifier to UZP	[$-\Delta V_{UZP} / \Delta(V_{ZPx1} - V_{ZPx2}) = 10$]	(x=1,2,3,4)
0	1	Gain **30** Amplifier to UZP	[$-\Delta V_{UZP} / \Delta(V_{ZPx1} - V_{ZPx2}) = 30$]	(x=1,2,3,4)
1	0	Gain **2** Amplifier to UZP	[$\Delta V_{UZP} / \Delta V_{IMESS} = 2$]	
1	1	Squib Voltage to UZP	[$V_{ZPx1} = 5 \times V_{UZP}$]	(x=1,2,3,4)

Hardware requirements depending on MODE0 - or MODE1

Mode	MODE	ZKEN	ZKEN_int	HSEN_EN12	LSEN_EN34	Function
MODE0	0	x	1	x	x	(4xxx)H: reference current
MODE0	0	x	1	x	x	(6xxx)H: reference + WDR main current
MODE0	0	x	1	1	1	(7xxx)H: reference + HSx main current
MODE1	1	x	1	0	0	(4xxx)H: reference current
MODE1	1	x	1	0	0	(6xxx)H: reference + WDR main current
MODE1	1	x	1	0	0	(7xxx)H: reference + HSx main current

For MODE1 operation an initializing SPI 'Mode command' needs to be sent once after start up. If RESQ = 0 is generated, then the measurement will be interrupted and the ASIC will return to it's default state of the MODE0. A soft reset (FFFF)H does not change the mode.

J.2.5: Firing Voltage Measurement Commands:

(3XXX)H

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB
0	**0**	**1**	**1**	x	x	x	x	x	x	x	x	x	x	1/0	1/0

b0..b1 : channel select

b1	b0	channel select
0	0	Firing voltage VZ1 measurement channel 1 active
0	1	Firing voltage VZ2 measurement channel 2 active
1	0	Firing voltage VZ3 measurement channel 3 active
1	1	Firing voltage VZ4 measurement channel 4 active

J.2.6: Squib Leakage Measurement Commands with one of eight squib switches in ON-state: (CXXX)H

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB
1	**1**	**0**	**0**	x	x	x	x	x	1/0	1/0	1/0	x	x	1/0	1/0

b0..b1 : channel select

b1	b0	channel select
0	0	Leakage measurement channel 1 active
0	1	Leakage measurement channel 2 active
1	0	Leakage measurement channel 3 active
1	1	Leakage measurement channel 4 active

b4..b6 : HS-/ LS-switch selection

b6	b5	b4	HS-/ LS-switch selection
0	0	0	Low-Side-Switch of squib 1 ON
0	0	1	Low-Side-Switch of squib 2 ON
0	1	0	Low-Side-Switch of squib 3 ON
0	1	1	Low-Side-Switch of squib 4 ON
1	0	0	High-Side-Switch of squib 1 ON
1	0	1	High-Side-Switch of squib 2 ON
1	1	0	High-Side-Switch of squib 3 ON
1	1	1	High-Side-Switch of squib 4 ON

Hardware requirements depending on MODE0 - or MODE1

Mode	MODE	ZKEN	ZKEN_int	HSEN_EN12	LSEN_EN34	Function
MODE0	0	x	1	1	x	(Cxxx)H: measurement with HSx on
MODE0	0	x	1	x	0	(Cxxx)H: measurement with LSx on
MODE1	1	x	1	0	0	(Cxxx)H: measurement with HSx on
MODE1	1	x	1	0	0	(Cxxx)H: measurement with LSx on

For MODE1 operation an initializing SPI ‘Mode command’ needs to be sent once after start up. If RESQ = 0 is generated, then the measurement will be interrupted and the ASIC will return to it’s default state of the MODE0. A soft reset (FFFF)H does not change the mode.

J.2.7: Voltage-/ Current-Sources (V/I) Commands:

V/I-Sources Command; Set IASGx (x=1,2,3,4) voltage source to low voltage: 2.8 V (2XXX)H

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB
0	**0**	**1**	**0**	x	x	x	x	x	x	x	x	x	x	1/0	1/0

V/I-Sources Command; Set IASGx (x=1,2,3,4) voltage source to high voltage: 5.0 V (BXXX)H

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB
1	**0**	**1**	**1**	x	x	x	x	x	x	x	x	x	x	1/0	1/0

b0..b1 : source select

b1	b0	source select
0	0	IASG1 voltage source active
0	1	IASG2 voltage source active
1	0	IASG3 voltage source active
1	1	IASG4 voltage source active

J.2.8: Supply Voltage-, Lamp-Measurement and Squib Leakage Measurement with squib switches in OFF-state
Commands: (1XXX)H

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB
0	**0**	**0**	**1**	x	x	x	x	x	1/0	1/0	1/0	x	1/0	1/0	1/0

b0..b1 : channel select b2 : Leakage Measurement active or inactive

b2	b1	b0	channel select
1	0	0	Leakage measurement channel 1 active
1	0	1	Leakage measurement channel 2 active
1	1	0	Leakage measurement channel 3 active
1	1	1	Leakage measurement channel 4 active
0	x	x	Leakage measurement INACTIVE

b4..b6 : select measurement channel

Name	b6	b5	b4	select voltage measurement
UEVZ	0	0	0	EVZ voltage measurement active
UEVZ2	0	0	1	EVZ2 voltage measurement active
UUBATT	0	1	0	UBATT voltage measurement active
UUBRL	0	1	1	UBRL voltage measurement active
UAWL1	1	0	0	AWL1 voltage measurement active
IAWL1	1	0	1	AWL1 current measurement active
UAWL2D	1	1	0	AWL2D voltage measurement active
UAWL2S	1	1	1	AWL2S voltage measurement active

J.2.9: Control Commands for Lamps, Watchdog and Safing Sensor Detection:

(0XXX)H : If used as a stand alone command

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB
0	**0**	**0**	**0**	1/0	1/0	1/0	1/0	x	x	x	x	x	x	x	x

(XXXX)H, except (5XXX)H and (FXXX)H: If used during transmission of other commands

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB
x	x	x	x	1/0	1/0	1/0	1/0	x	x	x	x	x	x	x	x

a0: if its value is **0**: **no** valid control command is transmitted
if its value is **1**: **a** valid control command is transmitted,
bit a1..a3 will act as stated in the following table;
a1,a2 selects actions; a3 defines on/off state

Name	a3	a2	a1	Function	
SAWL1B	0	0	0	Lamp Driver 1 (AWL1) = ON (AW1CT is open)	**(default)**
SAWL2D	0	0	1	Lamp Driver 2 (AWL2) = OFF	**(default)**
WDTRL	0	1	0	Watchdog Trigger = 0 (LOW)	**(default)**
SMSSL	0	1	1	Safing Sensor Closure Detection: Current = 0mA	**(default)**
SAWL1D	1	0	0	Lamp Driver 1 (AWL1) = OFF (AW1CT is open)	
SAWL2B	1	0	1	Lamp Driver 2 (AWL2) = ON	
WDTRH	1	1	0	Watchdog Trigger = 1 (HIGH)	
SMSSH	1	1	1	Safing Sensor Closure Detection: Current ≥ 1.2 mA	

If RESQ=0 is generated, then the SPI-control register is reset to its inactive default value:
Lamp Driver 1(AWL1) is activated if AW1CT is open,
Lamp Driver 2 (AWL2) is deactivated,
Watchdog Trigger signal is low,
Safing Sensor Closure Detection: Current source to ground = 0mA

The Control Commands can be transmitted alone as a 16bit word [command $(0XXX)_H$] or in combination with other commands [command $(XXXX)_H$]. The Control Command is latched and active till reprogramming via SPI.

J.2.10: Oscillator Frequency Test Mode Command: $(5555)_H$

If RESQ=0 is generated, then the test mode is interrupted and the SPI-decoder is reset.
After activating the 'Oscillator Frequency Test Mode' the internal generated oscillator frequency is reported to the pin LL and LH. The signal shape is the inverted curve of the FOSC signal in the description of 'Oscillator for...'.

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB
0	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**

J.2.11: 2.8V Reference Test Mode Command: $(AAAA)_H$

If RESQ=0 is generated, then the test mode is interrupted and the SPI-decoder is reset.
After activating the '2.8 V Reference Test Mode' the internal generated voltage reference is reported to the pin UZP.

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB
1	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**

J.2.12: Reset by SPI Command: $(FFFF)_H$

By applying this command, the SPI-decoder is reset to its default state. Measurements will be interrupted. Latched control commands (J.2.9) return to it's default value. If the system works in the MODE1, then this command will not change the state of MODE1 operation. This command has no effect on the RESQ pin.

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

J.2.13: Average Chip Temperature Test Mode Command: $(9XXX)_H$

If RESQ=0 is generated, then the test mode is interrupted and the SPI-decoder is reset to its default state. After activating the 'Average Chip Temperature Test Mode' an internal generated temperature stable reference current (approx. 40 µA) supplies four serial connected bipolar diodes, which are distributed on the chip surface. The temperature dependent voltage drop (approx. -7mV/K) is reported to the pin UZP.
The voltage on pin UZP will be divided by two and it's temperature dependence will be reduced to approximately -3.5mV/K, if the Alarm Warning Lamp Driver AWL2 goes into the over temperature shut down. Then the signal on pin UZP can be interpreted as a digital information of an AWL2 over temperature shut down. A SAWL2D command to switch off the lamp AWL2 after temperature decreasing returns the ASIC to the 'Average Chip Temperature Test Mode'.

Byte **A**: FUNCTION - BYTE								Byte **B**: SELECTION - BYTE							
a7 MSB	a6	a5	a4	a3	a2	a1	a0 LSB	b7 MSB	b6	b5	b4	b3	b2	b1	b0 LSB
1	**0**	**0**	**1**	x	x	x	x	x	x	x	x	x	x	x	x

Application Notes

1. It is recommended that a RC snubber is connected directly to pin SVZ to reduce ringing due to Boost converter switching.

2. If pins ZPx1 and ZPx2 are connected to inductive loads/wiring then it may be necessary to add protection devices to reduce negative transients caused by external shorts to ground during deployment.

3. IASGx pins connected to loads with chassis ground reference may require protection against negative voltage offsets.

4. An open/disconnected M1 pin cannot be detected with a Leakage Measurement which turns on the LS driver of channel 1, i.e. C000 Hex. Instead a cross coupled Leakage Measurement must be performed. That is, look for leakage on channel **2** while activating the LS driver of channel **1**, i.e. C001 Hex.

5. Due to the low VZx leakage currents a longer delay time or external discharge resistor is necessary t detect an open VZx pin with a voltage measurement via UZP.

6. When AWL2 is configured as a low side driver it is necessary to add an external discharge resistor to detect an open load with the driver off.

7. It is recommended that a low ESR capacitor is used for the VCC5 output of the Buck converter to reduce ripple.

8. A series diode connection is required for the VZx pins to prevent reverse current flow through the high side driver transistor body diode charging up the deployment caps due to external short to battery.

9. It is recommended that a MOV is connected to the battery line of the airbag module to prevent violations of the maximum ratings. The MOV is not required in case of an existing central load dump protection.

10. If the UBRL pin voltage is protected against negative voltages by an external blocking diode, the series resistor to UBRL is not required.

Edition 05.2001

**Published by Infineon Technologies AG i. Gr.,
Bereichs Kommunikation, St.-Martin-Strasse 53
D-81541 München**

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologiesis an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.