256K x 8 CMOS FLASH MEMORY WITH LPC INTERFACE

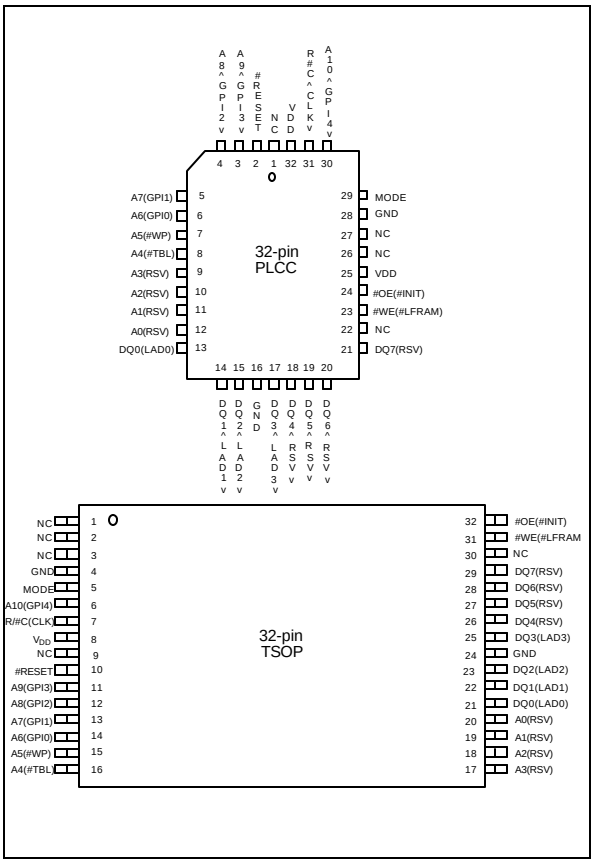
GENERAL DESCRIPTION

The W49V002A is a 2megabit, 3.3-volt only CMOS flash memory organized as 256K × 8 bits. The device can be programmed and erased in-system with a standard 3.3V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W49V002A results in fast program/erase operations with extremely low current consumption. This device can operate at two modes, Programmer bus interface mode and LPC bus interface mode. As in the Programmer interface mode, it acts like the traditional flash but with a multiplexed address inputs. But in the LPC interface mode, this device complies with the Intel LPC specification 1.0. The device can also be programmed and erased using standard EPROM programmers.

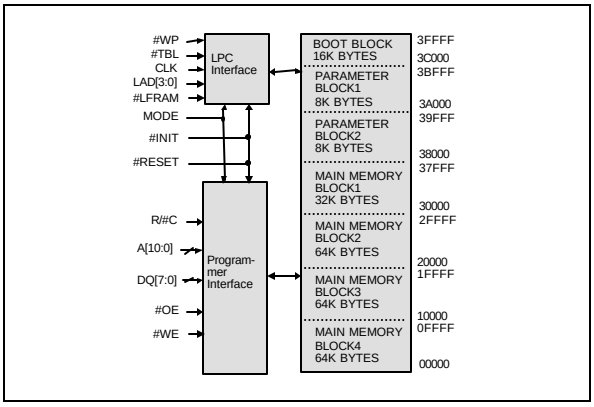
FEATURES

- Single 3.3-volt operations:
  - 3.3-volt Read
  - 3.3-volt Erase
  - 3.3-volt Program
- Fast Program operation:
  - Byte-by-Byte programming: 50 μS (typ.)
- Fast Erase operation: 150 mS (typ.)
- Endurance: 10K cycles (typ.)
- Twenty-year data retention
- Hardware data protection
  - #TBL & #WP serve as hardware protection
- One 16K bytes Boot Block with lockout protection
- Two 8K bytes Parameter Blocks
- Four Main Memory Blocks (with 32K bytes, 64K bytes, 64K bytes, 64K bytes each)
- Low power consumption
  - Active current: 25 mA (typ.)
  - Standby current: 20 μA (typ.)
- Automatic program and erase timing with internal V_{PP} generation
- End of program or erase detection
  - Toggle bit
  - Data polling
- Latched address and data
- TTL compatible I/O
- Available packages: 32L PLCC and 32L STSOP

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMB	INTERFACE		PIN NAME
	PGM	LPC	
MODE	*	*	Interface Mode Selection
#RESET	*	*	Reset
#INIT		*	Initialize
#TBL		*	Top Boot Block Lock
#WP		*	Write Protect
CLK		*	CLK Input
GPI[4:0]		*	General Purpose Inputs
LAD[3:0]		*	Address/Data Inputs
#LFRAM		*	LPC Cycle Initial
R/#C	*		Row/Column Select
A[10:0]	*		Address Inputs
DQ[7:0]	*		Data Inputs/Outputs
#OE	*		Output Enable
#WE	*		Write Enable
VDD	*	*	Power Supply
GND	*	*	Ground
RSV	*	*	Reserve Pins
NC	*	*	No Connection

FUNCTIONAL DESCRIPTION

Interface Mode Selection And Description

This device can be operated in two interface modes, one is Programmer interface mode, the other is LPC interface mode. The MODE pin of the device provides the control between these two interface modes. These interface modes need to be configured before power up or return from #RESET. When MODE pin is set to high state, the device is in the Programmer mode; while the MODE pin is set to low state(or leaved no connection), it is in the LPC mode. In Programmer mode, this device just behaves like traditional flash parts with 8 data lines. But the row and column address inputs are multiplexed, which go through the address inputs A[10:0]. For LPC mode, It complies with the LPC Interface Specification Revision 1.0. Through LAD[3:0] to communicate with the system chipset .

Read(Write) Mode

In Programmer interface mode, the read(write) operation of the W49V002A is controlled by #OE (#WE). The #OE (#WE) is held low for the host to obtain(write) data from(to) the outputs(inputs). #OE is the output control and is used to gate data from the output pins. The data bus is in high impedance state when #OE is high. As in the LPC interface mode, the read or write is determined by the "bit 1 of CYCLE TYPER+DIR".

Reset Operation

The #RESET input pin can be used in some application. When #RESET pin is at high state, the device is in normal operation mode. When #RESET pin is at low state, it will halt the device and all outputs will be at high impedance state. As the high state re-asserted to the #RESET pin, the device will return to read or standby mode, it depends on the control signals.

Chip Erase Operation

The chip-erase mode can be initiated by a six-byte command sequence. After the command loading cycle, the device enters the internal chip erase mode, which is automatically timed and will be completed within fast 100 mS (typical). The host system is not required to provide any control or timing during this operation. If the boot block programming lockout is activated, only the data in the other memory blocks will be erased to FF(hex) while the data in the boot block will not be erased (remains as the same state before the chip erase operation). The entire memory array will be erased to FF(hex) by the chip erase operation if the boot block programming lockout feature is not activated. The device will automatically return to normal read mode after the erase operation completed. Data polling and/or Toggle Bits can be used to detect end of erase cycle.

Sector Erase Operation

The seven sectors, one boot block and two parameter blocks and four main blocks, can be erased individually by initiating a six-byte command sequence. Sector address is latched on the falling #WE edge of the sixth cycle, while the 30(hex) data input command is latched at the rising edge of #WE. After the command loading cycle, the device enters the internal sector erase mode, which is automatically timed and will be completed within fast 150 mS (typical). The host system is not required to provide any control or timing during this operation. The device will automatically return to normal read mode after the erase operation completed. Data polling and/or Toggle Bits can be used to detect end of erase cycle.

Program Operation

The W49V002A is programmed on a byte-by-byte basis. Program operation can only change logical data

"1" to logical data "0." The erase operation, which changed entire data in main memory and/or boot block from "0" to "1", is needed before programming.

The program operation is initiated by a 4-byte command cycle (see Command Codes for Byte Programming). The device will internally enter the program operation immediately after the byte-program command is entered. The internal program timer will automatically time-out (100 µS max. - T_{BP}) once it is completed and then return to normal read mode. Data polling and/or Toggle Bits can be used to detect end of program cycle.

Boot Block Operation and Hardware Protection at Initial- #TBL & #WP

There are two alternatives to set the boot block. One is software command sequences method; the other is hardware method. 16K-byte in the top location of this device can be locked as boot block, which can be used to store boot codes. It is located in the last 16K bytes of the memory with the address range from 3C000(hex) to 3FFFF(hex).

Please see Command Codes for Boot Block Lockout Enable for the specific code. Once this feature is set, the data for the designated block cannot be erased or programmed (programming lockout), other memory locations can be changed by the regular programming method.

Besides the software method, there is a hardware method to protect the top boot block and other sectors. Before program/erase to this device, set the #TBL pin to low state and then the top boot block will not be programmed/erased. When enabling hardware top boot block, #TBL being low state, it will override the software method setting. That is, if #TBL is at low state, then top boot block cannot be programmed/erased no matter how the software boot block lock setting.

Another pin, #WP, will protect the whole chip if this pin is set to low state before program/erase. The enable of this pin will override the #TBL setting. That is, the top boot block cannot be programmed/erased if this pin is set to low no matter how the #TBL or software boot block lock setting.

Hardware Data Protection

The integrity of the data stored in the W49V002A is also hardware protected in the following ways:

(1) Noise/Glitch Protection: A #WE pulse of less than 15 nS in duration will not initiate a write cycle.

(2) V_{DD} Power Up/Down Detection: The programming operation is inhibited when V_{DD} is less than 1.5V typical.

(3) Write Inhibit Mode: Forcing #OE low or #WE high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

(4) V_{DD} power-on delay: When V_{DD} has reached its sense level, the device will automatically time-out 5 mS before any write (erase/program) operation.

Data Polling (DQ_7)- Write Status Detection

The W49V002A includes a data polling feature to indicate the end of a program or erase cycle. When the W49V002A is in the internal program or erase cycle, any attempts to read DQ_7 of the last byte loaded will receive the complement of the true data. Once the program or erase cycle is completed, DQ_7 will show the true data. Note that DQ_7 will show logical "0" during the erase cycle, and when erase cycle has been completed it becomes logical "1" or true data.

Toggle Bit (DQ_6)- Write Status Detection

In addition to data polling, the W49V002A provides another method for determining the end of a program cycle. During the internal program or erase cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's. When the program or erase cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

Memory Address Map

There are 8M bytes space reserved for BIOS Addressing. The ROM will respond to 256K byte pages whenever the memory address rang is within the top 4M bytes and bottom 128K bytes.

The 32bit address space is as below:

Block	Address Range
4M Byte BIOS ROM	FFFF,FFFFh:FFC0,0000h
128K Byte BIOS ROM	000F,FFFFh:000E,0000h
Registers	FFBC,0100h

General Purpose Inputs Register

This register reads the GPI[4:0] pins on the W49V002A.This is a pass-through register which can read via memory address FFBC0100(hex). Since it is pass-through register, there is no default value.

Bit	Function
7-5	Reserved
4	Read GPI4 pin status
3	Read GPI3 pin status
2	Read GPI2 pin status
1	Read GPI1 pin status
0	Read GPI0 pin status

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software operation. In the software access mode, a six-byte (or JEDEC 3-byte) command sequence can be used to access the product ID. A read from address 0000(hex) outputs the manufacturer code, DA(hex). A read from address 0001(hex) outputs the device code, B0(hex)." The product ID operation can be terminated by a three-byte command sequence or an alternate one-byte command sequence (see Command Definition table).

TABLE OF OPERATING MODES

Operating Mode Selection - Programmer Mode

(V_{HH} = 12V ± 5%)

MODE	PINS				
	#OE	#WE	#RESET	ADDRESS	DQ.
Read	VIL	VIH	VIH	AIN	Dout
Write	VIH	VIL	VIH	AIN	Din
Standby	X	X	VIL	X	High Z
Write Inhibit	VIL	X	VIH	X	High Z/DOUT
	X	VIH	VIH	X	High Z/DOUT
Output Disable	VIH	X	VIH	X	High Z

Operating Mode Selection - LPC Mode

Operation modes in LPC interface mode are determined by "cycle type" when it is selected. When it is not selected, its outputs (LAD[3:0]) will be disable. Please reference to the "Standard LPC Memory Cycle Definition".

TABLE OF COMMAND DEFINITION

COMMAND DESCRIPTION	NO. OF Cycles	1ST CYCLE	2ND CYCLE	3RD CYCLE	4TH CYCLE	5TH CYCLE	6TH CYCLE
		Addr. Data	Addr. Data	Addr. Data	Addr. Data	Addr. Data	Addr. Data
Read	1	A_{IN} D_{OUT}					
Chip Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 10
Sector Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	SA 30
Byte Program	4	5555 AA	2AAA 55	5555 A0	A_{IN} D_{IN}		
Boot Block Lockout	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 40
Product ID Entry	3	5555 AA	2AAA 55	5555 90			
Product ID Exit (1)	3	5555 AA	2AAA 55	5555 F0			
Product ID Exit (1)	1	XXXX F0					

Note: 1. The cycle means the write command cycle not the LPC clock cycle.

2. The Column Address / Row Address are mapped to the Low / High order Internal Address. i.e. Column Address A[10:0] are mapped to the internal A[10:0], Row Address A[6:0] are mapped to the internal A[17:11]
3. Address Format: A14–A0 (Hex); Data Format: DQ7-DQ0 (Hex)
4. Either one of the two Product ID Exit commands can be used.
5. SA : Sector Address
   SA = 3C000h to 3FFFFh for Boot Block
   SA = 3A000h to 3BFFFh for Parameter Block1
   SA = 38000h to 39FFFh for Parameter Block2
   SA = 30000h to 37FFFh for Main Memory Block1
   SA = 2XXXXh for Main Memory Block2
   SA = 1XXXXh for Main Memory Block3
   SA = 0XXXXh for Main Memory Block4

STANDARD LPC MEMORY CYCLE DEFINITION

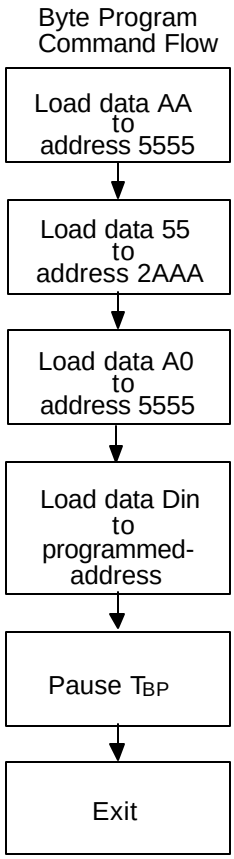
FIELD	NO. OF CLOCKS	DESCRIPTION
Start	1	"0000b" appears on LPC bus to indicate the initial
Cycle Type & Dir	1	"010Xb" indicates memory read cycle; while "011xb" indicates memory write cycle. "X" mean don't have to care.
TAR	2	Turned Around Time
Addr.	8	Address Phase for Memory Cycle. LPC supports the 32 bits address protocol. The addresses transfer most significant nibble first and least significant nibble last. (i.e. Address[31:28] on LAD[3:0] first , and Address[3:0] on LAD[3:0] last.)
Sync.	N	Synchronous to add wait state. "0000b" means Ready, "0101b" means Short Wait, "0110b" means Long Wait, "1001b" for DMA only, "1010b" means error, and other values are reserved.
Data	2	Data Phase for Memory Cycle. The data transfer least significant nibble first and most significant nibble last. (i.e. DQ[3:0] on LAD[3:0] first , then DQ[7:4] on LAD[3:0] last.)

Note: 1. For detail related LPC specification, please refer to Intel LPC spec. 1.0 or later.

Command Codes for Byte Program

BYTE SEQUENCE	ADDRESS	DATA
0 Write	5555H	AAH
1 Write	2AAAH	55H
2 Write	5555H	A0H
3 Write	Programmed-Address	Programmed-Data

Byte Program Flow Chart

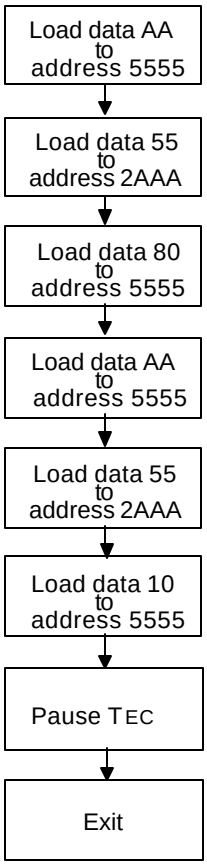


Notes for software program code:
Data Format: DQ7–DQ0 (Hex); XX = Don't Care
Address Format: A14–A0 (Hex)

Command Codes for Chip Erase

BYTE SEQUENCE	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	5555H	10H

Chip Erase Acquisition Flow

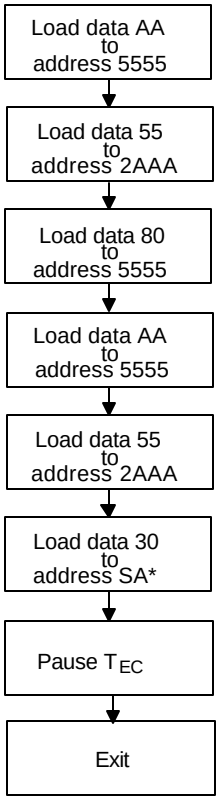


Notes for chip erase:
Data Format: DQ7–DQ0 (Hex)
Address Format: A14–A0 (Hex)

Command Codes for Sector Erase

BYTE SEQUENCE	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	SA*	30H

Sector Erase Acquisition Flow



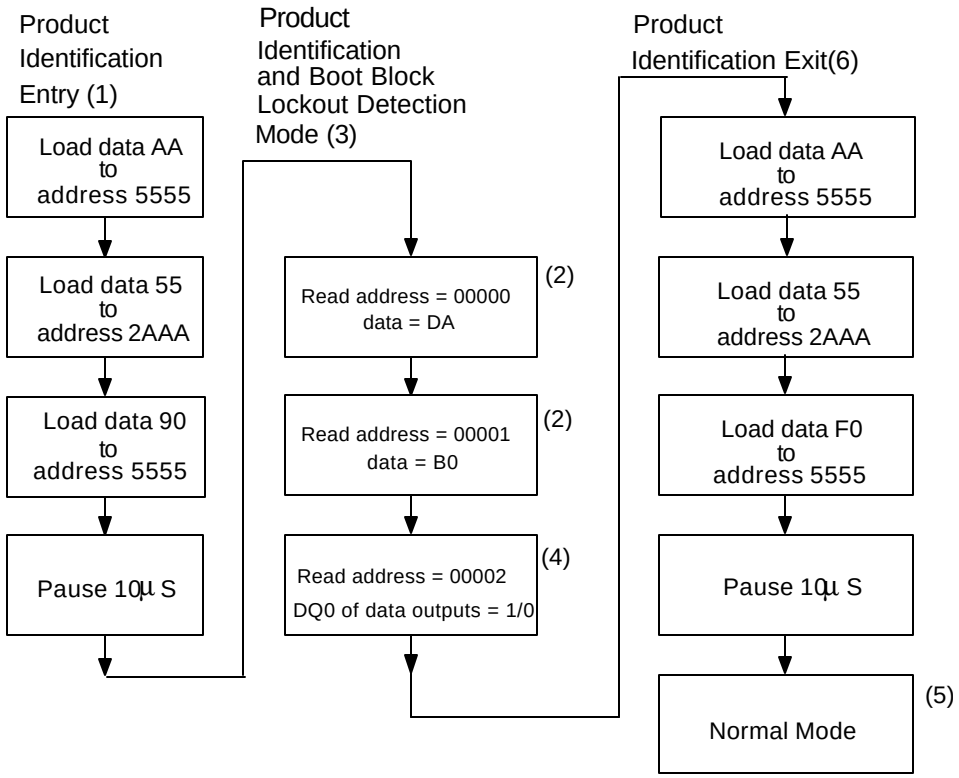
Notes for chip erase:

Data Format: DQ7–DQ0 (Hex)
Address Format: A14–A0 (Hex)
SA : Sector Address
SA = 3C000h to 3FFFFh for Boot Block
SA = 3A000h to 3BFFFh for Parameter Block1 SA = 2XXXXh for Main Memory Block2
SA = 38000h to 39FFFh for Parameter Block2 SA = 1XXXXh for Main Memory Block3
SA = 30000h to 37FFFh for Main Memory Block1 SA = 0XXXXh for Main Memory Block4

Command Codes for Product Identification and Boot Block Lockout Detection

BYTE SEQUENCE	SOFTWARE PRODUCT IDENTIFICATION / BOOT BLOCK LOCKOUT DETECTION ENTRY		SOFTWARE PRODUCT IDENTIFICATION / BOOT BLOCK LOCKOUT DETECTION EXIT (6)	
	ADDRESS	DATA	ADDRESS	DATA
1 Write	5555	AA	5555H	AAH
2 Write	2AAA	55	2AAAH	55H
3 Write	5555	90	5555H	F0H
	Pause 10µS		Pause 10µS	

Software Product Identification and Boot Block Lockout Detection Acquisition Flow



Notes for software product identification/boot block lockout detection:

(1) Data Format: DQ7–DQ0 (Hex); Address Format: A14–A0 (Hex)

(2) A1–A17 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.

(3) The device does not remain in identification and boot block lockout detection mode if power down.

(4) If the DQ0 of output data is "1," the boot block programming lockout feature is activated; if the DQ0 of output data "0," the lockout feature is inactivated and the block can be programmed.

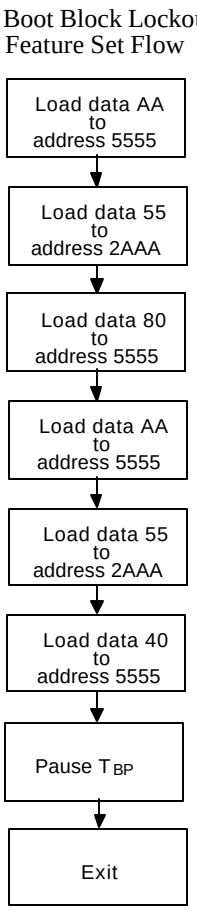
(5) The device returns to standard operation mode.

(6) Optional 1-write cycle (write F0 hex at XXXX address) can be used to exit the product identification/boot block lockout detection.

Command Codes for Boot Block Lockout Enable

BYTE SEQUENCE	BOOT BLOCK LOCKOUT FEATURE SET	
	ADDRESS	DATA
1 Write	5555H	AAH
2 Write	2AAAH	55H
3 Write	5555H	80H
4 Write	5555H	AAH
5 Write	2AAAH	55H
6 Write	5555H	40H
	Pause 1 Sec.	

Boot Block Lockout Enable Acquisition Flow



Notes for boot block lockout enable:
Data Format: DQ7–DQ0 (Hex)
Address Format: A14–A0 (Hex)

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-0.5 to +4.1	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential	-0.5 to V_{DD} +0.5	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to V_{DD} +0.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Programmer interface Mode DC Operating Characteristics

(V_{DD} 3.3V ± 5%, V_{GND}= 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I_{CC}	In Read or Write mode, all DQs open Address inputs = 3.0V/0V, at f = 3 MHz	-	20	30	mA
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{DD}	-	-	10	µA
Output Leakage Current	I_{LO}	V_{OUT} = GND to V_{DD}	-	-	10	µA
Input Low Voltage	V_{IL}	-	-0.3	-	0.8	V
Input High Voltage	V_{IH}	-	2.0	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -0.1mA	2.4	-	-	V

LPC interface Mode DC Operating Characteristics

(V_{DD} = 3.3V ± 5%, V_{GND}= 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I_{CC}	All I_{out} = 0A, CLK = 33MHz, in LPC mode operation.	-	40	60	mA
CMOS Standby Current	Isb1	#LFRAM = 0.9 V_{DD}, CLK = 33MHz, all inputs = 0.9 V_{DD} / 0.1 V_{DD}	-	20	100	uA
TTL Standby Current	Isb2	#LFRAM = 0.1 V_{DD}, CLK = 33MHz, all inputs = 0.9 V_{DD} / 0.1 V_{DD}	-	3	10	mA
Input Low Voltage	V_{IL}	-	-0.3	-	0.2 V_{DD}	V
Input High Voltage	V_{IH}	-	0.6 V_{DD}	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 1.5 mA	-	-	0.1 V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = -0.5 mA	0.9 V_{DD}	-	-	V

Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	$T_{PU. READ}$	100	µS
Power-up to Write Operation	$T_{PU. WRITE}$	5	mS

CAPACITANCE

(V_{DD} = 3.3V, T_A = 25° C, f = 1 MHz)

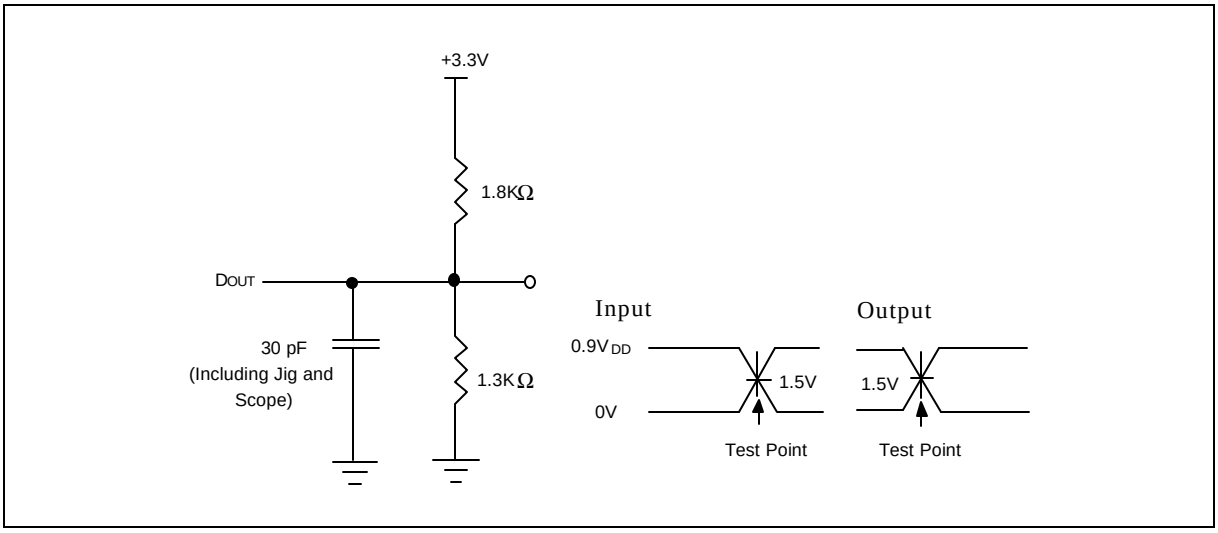
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	12	pf
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pf

PROGRAMMER INTERFACE MODE AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 0.9VDD
Input Rise/Fall Time	< 5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 30 pF

AC Test Load and Waveform



Programmer Interface Mode AC Characteristics, continued

AC Characteristics

Read Cycle Timing Parameters

(V_{DD} = 3.3V ± 5%, V_{GND} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	W49V002A		UNIT
		MIN.	MAX.	
Read Cycle Time	T_{RC}	300	-	nS
Row / Column Address Set Up Time	T_{AS}	50	-	nS
Row / Column Address Hold Time	T_{AH}	50	-	nS
Address Access Time	T_{AA}	-	200	nS
Output Enable Access Time	T_{OE}	-	100	nS
#OE Low to Active Output	T_{OLZ}	0	-	nS
#OE High to High-Z Output	T_{OHZ}	-	50	nS
Output Hold from Address Change	T_{OH}	0	-	nS

Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Reset Time	T_{RST}	1	-	-	µS
Address Setup Time	T_{AS}	50	-	-	nS
Address Hold Time	T_{AH}	50	-	-	nS
R/#C to Write Enable High Time	T_{CWH}	50	-	-	nS
#WE Pulse Width	T_{WP}	100	-	-	nS
#WE High Width	T_{WPH}	100	-	-	nS
Data Setup Time	T_{DS}	50	-	-	nS
Data Hold Time	T_{DH}	50	-	-	nS
#OE Hold Time	T_{OEH}	0	-	-	nS
Byte programming Time	T_{BP}	-	50	100	µS
Erase Cycle Time	T_{EC}	-	0.15	0.2	S

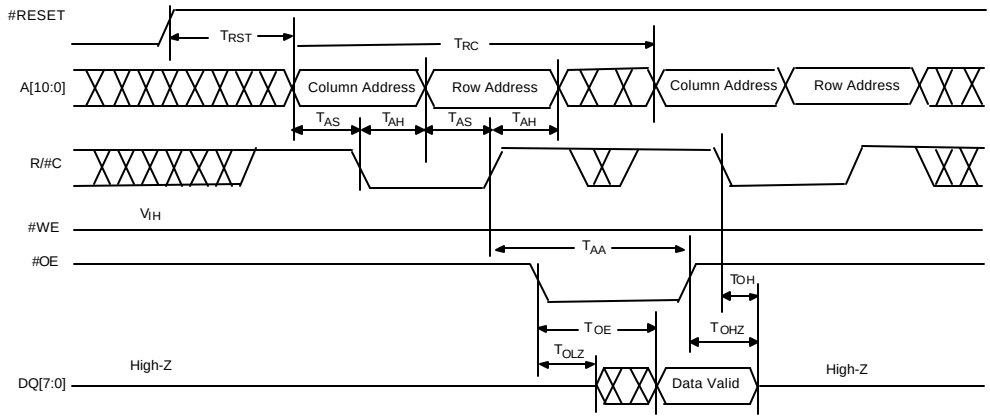
Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is input high and (b) low level signal's reference level is input low.
Ref. to the AC testing condition.

Data Polling and Toggle Bit Timing Parameters

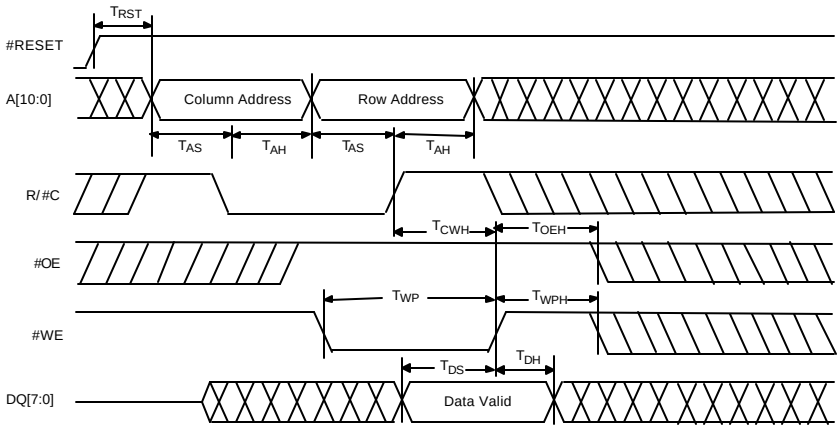
PARAMETER	SYM.	W49V002A		UNIT
		MIN.	MAX.	
#OE to Data Polling Output Delay	T_{OEP}	-	40	nS
#OE to Toggle Bit Output Delay	T_{OET}	-	40	nS

TIMING WAVEFORMS FOR PROGRAMMER INTERFACE MODE

Read Cycle Timing Diagram

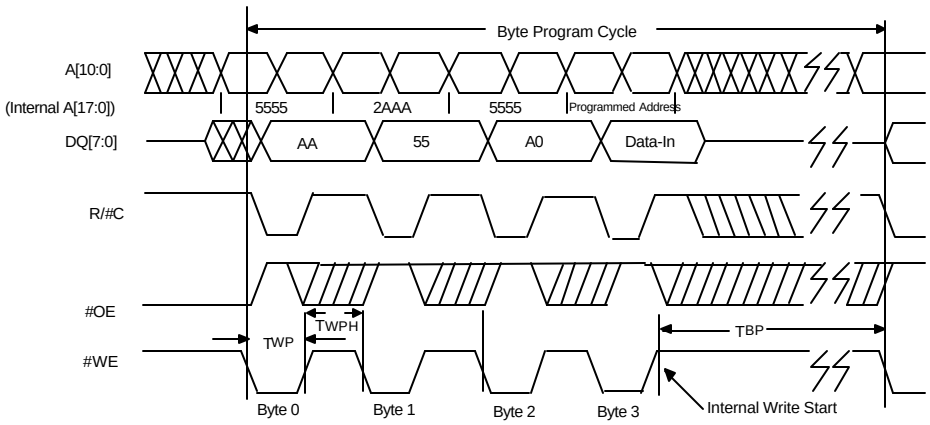


Write Cycle Timing Diagram



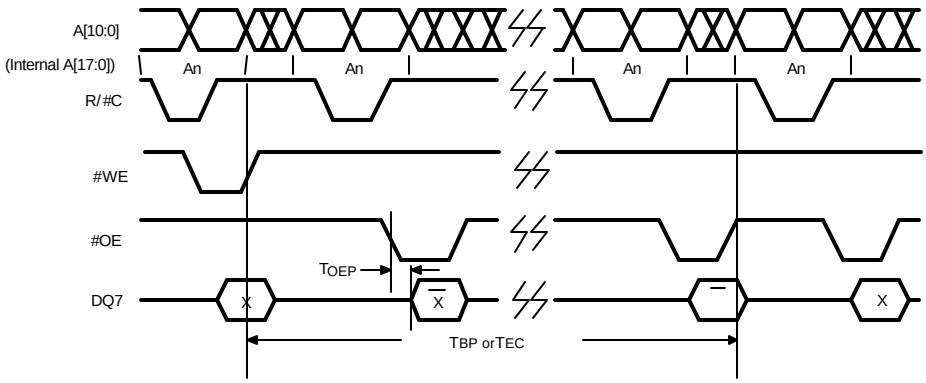
Timing Waveforms for Programmer Interface Mode, continued

Program Cycle Timing Diagram



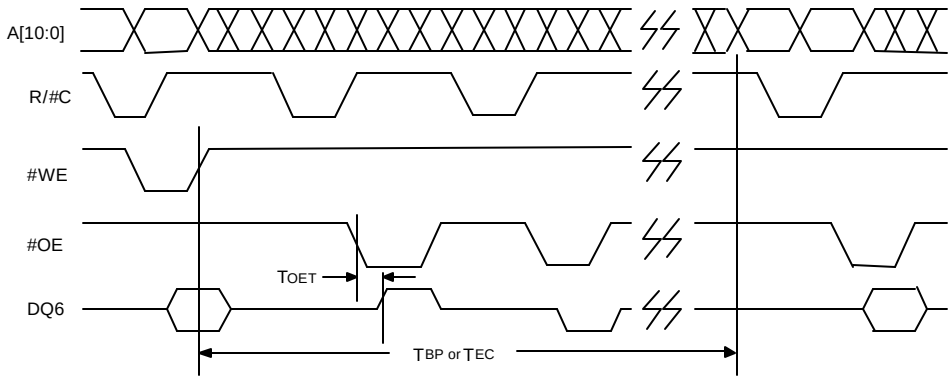
Note: The internal address A[17:0] are converted from external Column/Row address.
Column/Row Address are mapped to the Low/High order internal address.
i.e. Column Address A[10:0] are mapped to the internal A[10:0],
Row Address A[6:0] are mapped to the internal A[17:11].

#DATA Polling Timing Diagram

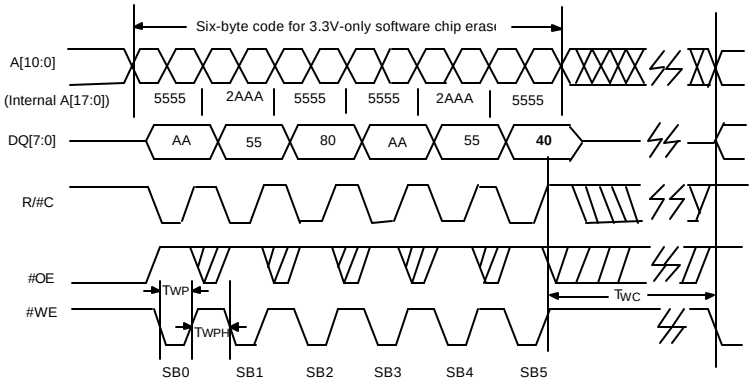


Timing Waveforms for Programmer Interface Mode, continued

Toggle Bit Timing Diagram



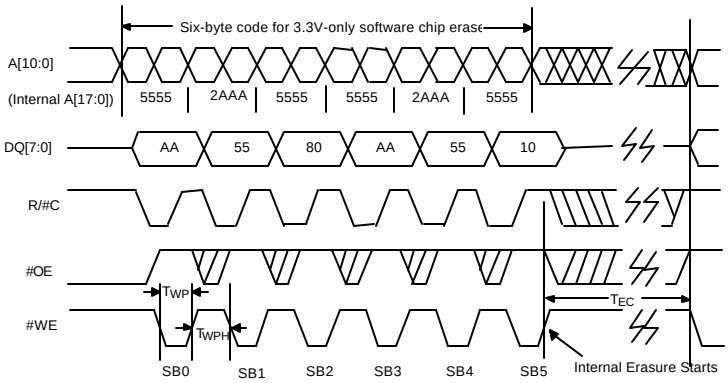
Boot Block Lockout Enable Timing Diagram



Note: The internal address A[17:0] are converted from external Column/Row adc
Column/Row Address are mapped to the Low/High order internal addr
i.e. Column Address A[10:0] are mapped to the internal A[10:0],
Row Address A[6:0] are mapped to the internal A[17:11].

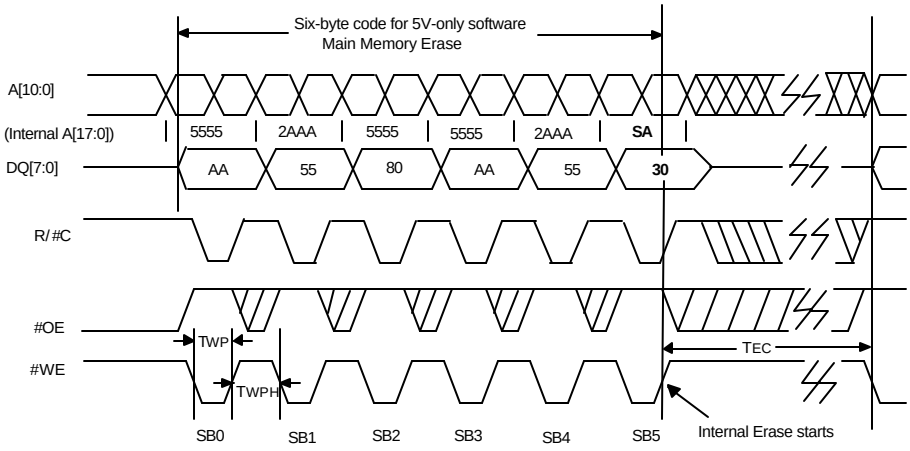
Timing Waveforms for Programmer Interface Mode, continued

Chip Erase Timing Diagram



Note: The internal address A[17:0] are converted from external Column/Row add
Column/Row Address are mapped to the Low/High order internal addre
i.e. Column Address A[10:0] are mapped to the internal A[10:0],
Row Address A[6:0] are mapped to the internal A[17:11].

Sector Erase Timing Diagram



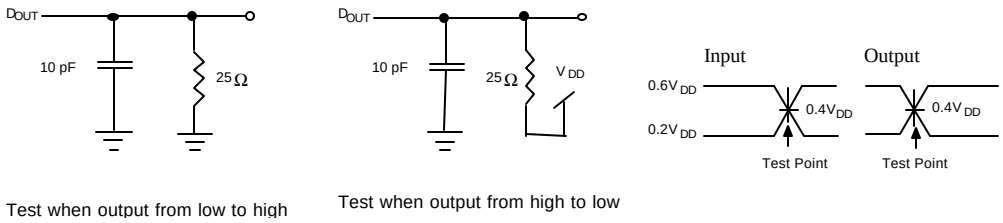
Note: The internal address A[17:0] are converted from external Column/Row address.
Column/Row Address are mapped to the Low/High order internal address.
i.e. Column Address A[10:0] are mapped to the internal A[10:0],
Row Address A[6:0] are mapped to the internal A[17:11].
SA = Sector Address, Please ref. to the "Table of Command Definition"

LPC INTERFACE MODE AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0.6 V_{DD} to 0.2 V_{DD}
Input Rise/Fall Slew Rate	1 V/nS
Input/Output Timing Level	0.4V_{DD} / 0.4V_{DD}
Output Load	1 TTL Gate and C_L = 10 pF

AC Test Load and Waveform



Test when output from low to high

Test when output from high to low

Read/Write Cycle Timing Parameters

(V_{DD} = 3.3V ± 5%, V_{GND} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	W49V002A		UNIT
		MIN.	MAX.	
Clock Cycle Time	T_{CYC}	30	-	nS
Input Set Up Time	T_{SU}	7	-	nS
Input Hold Time	T_{HD}	0	-	nS
Clock to Data Valid	T_{KQ}	-	11	nS

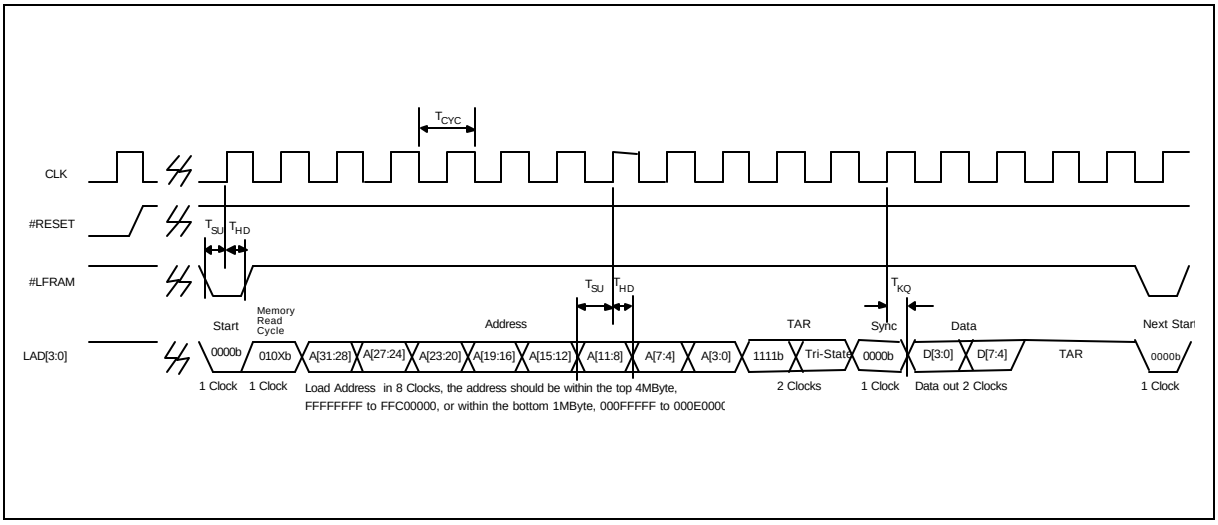
Reset Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Vdd stable to Reset Active	T_{PRST}	1	-	-	mS
Clock Stable to Reset Active	T_{KRST}	100	-	-	µS
Reset Pulse Width	T_{RSTP}	100	-	-	nS
Reset Active to Output Float	T_{RSTF}	-	-	50	nS
Reset Inactive to Input Active	T_{RST}	1	-	-	µS

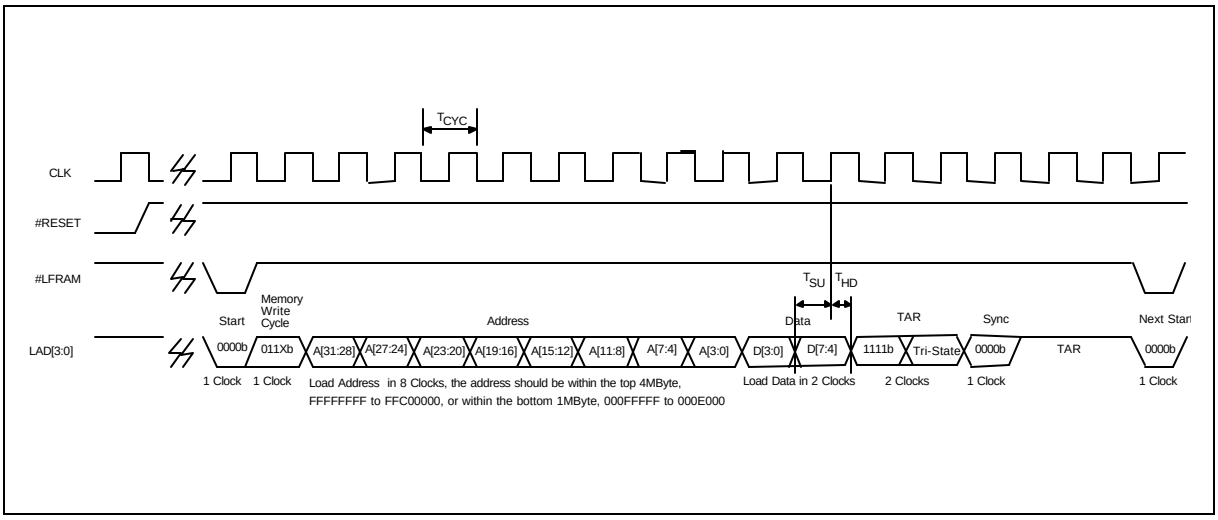
Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is input high and (b) low level signal's reference level is input low.
Ref. to the AC testing condition.

TIMING WAVEFORMS FOR LPC INTERFACE MODE

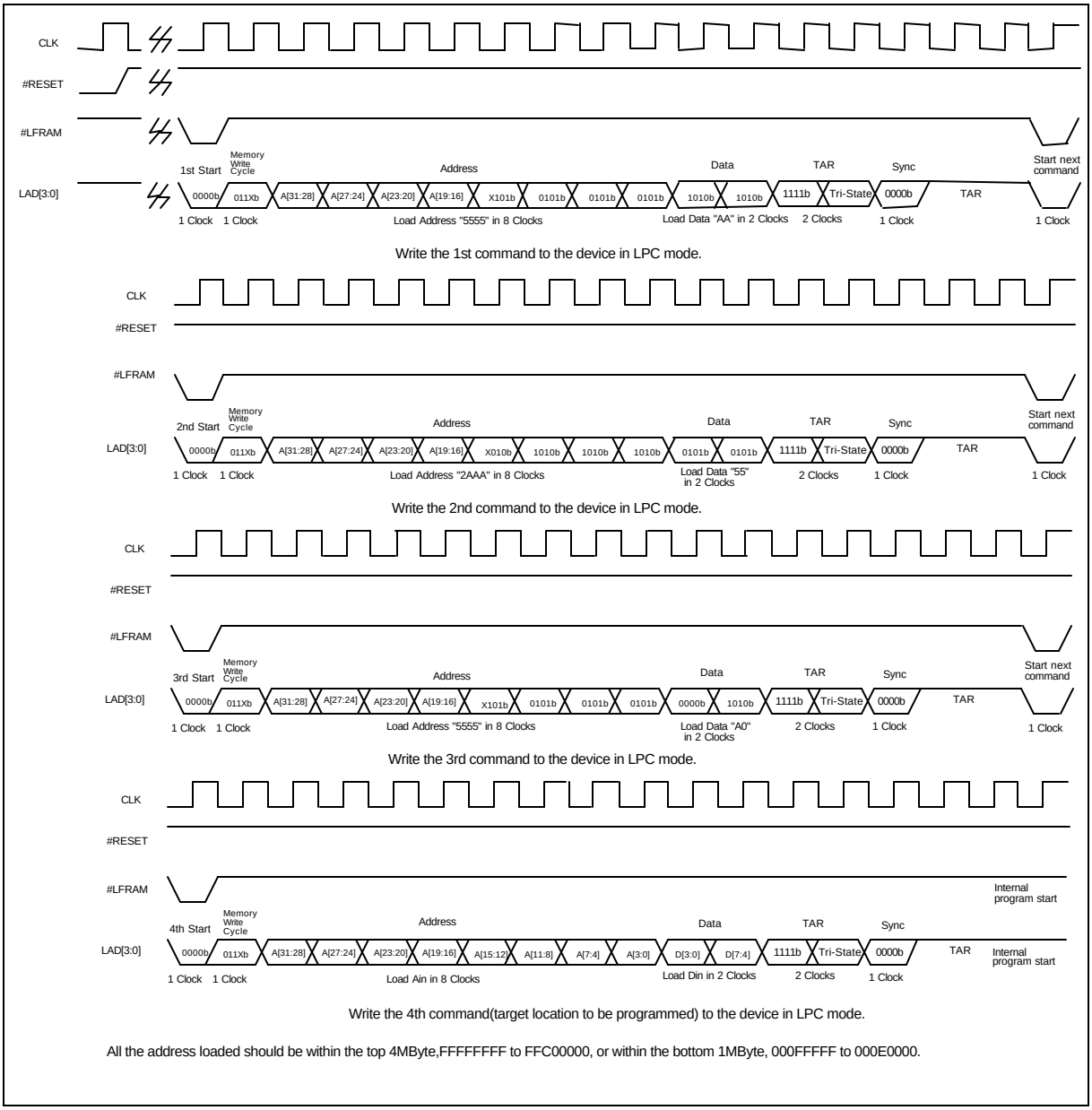
Read Cycle Timing Diagram



Write Cycle Timing Diagram



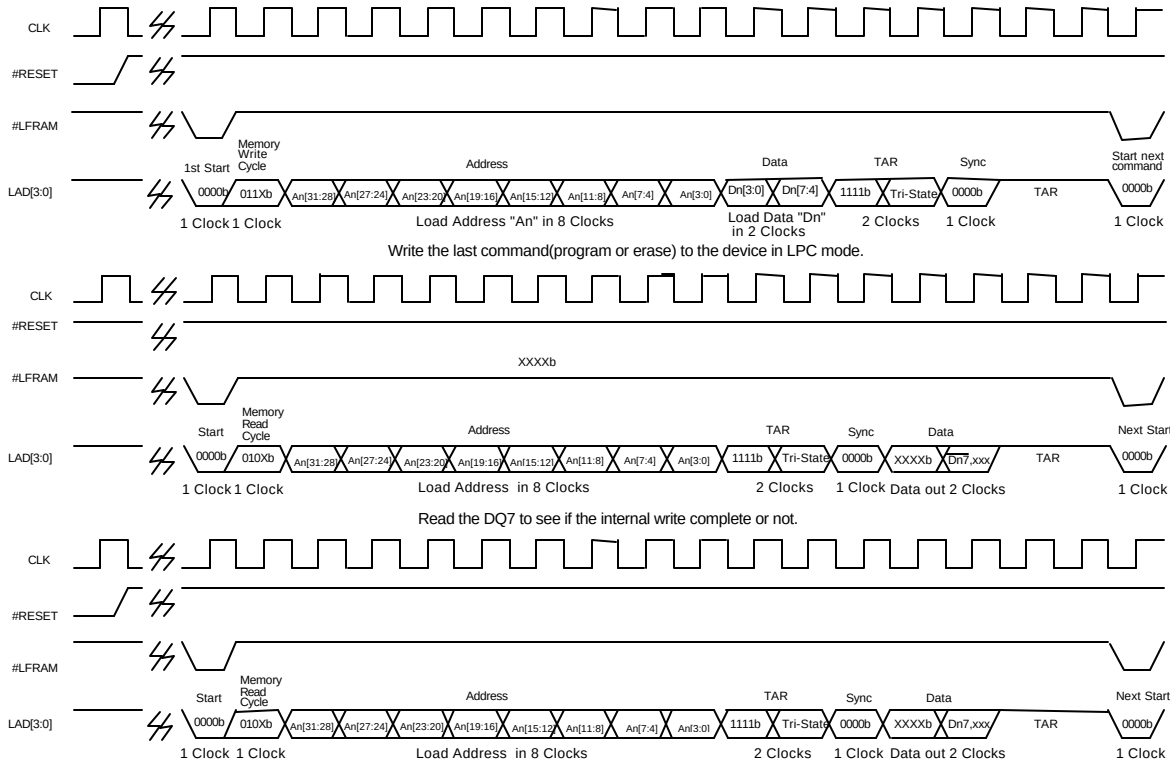
Program Cycle Timing Diagram



All the address loaded should be within the top 4MByte,FFFFFFFF to FFC00000, or within the bottom 1MByte, 000FFFFF to 000E0000.

Timing Waveforms for LPC Interface Mode, continued

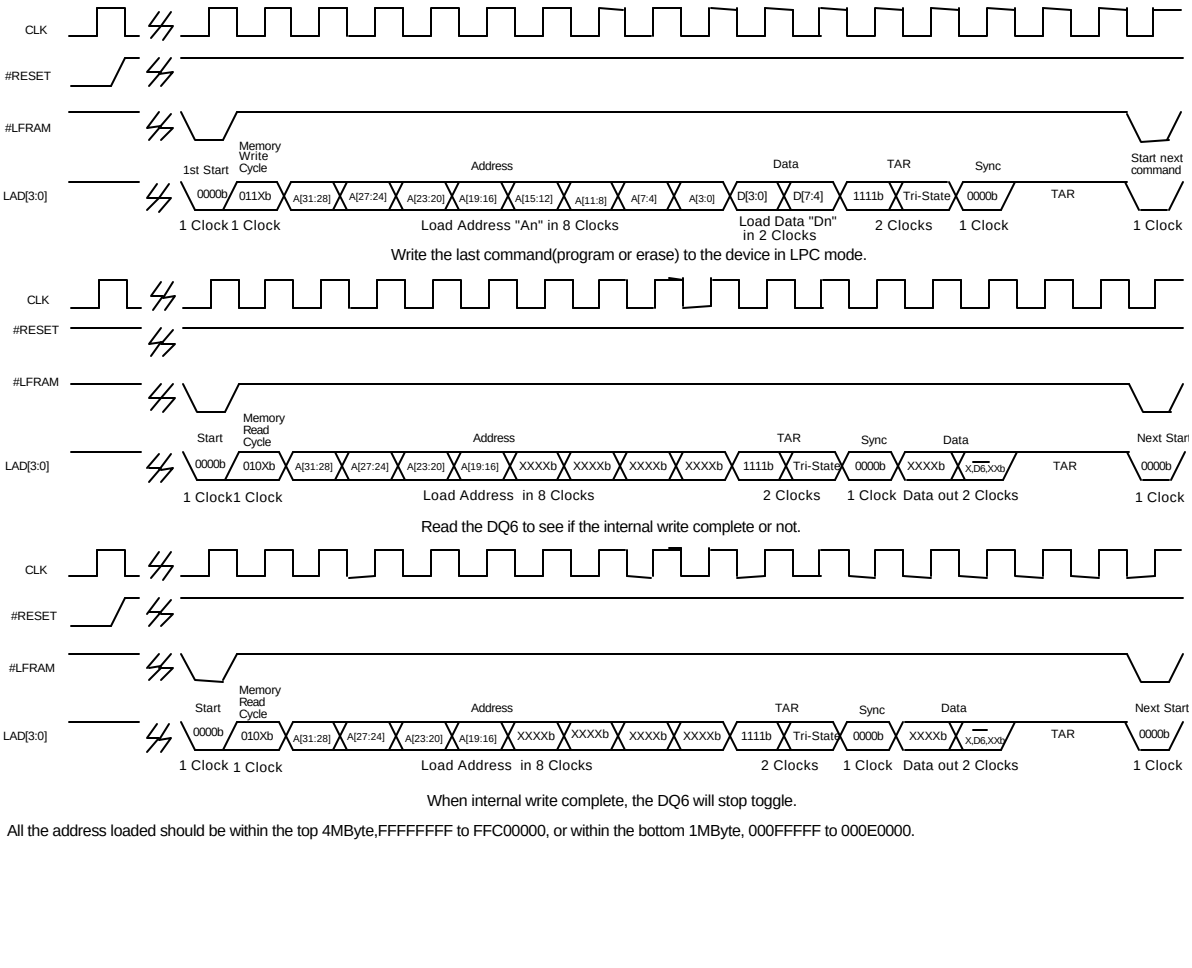
#DATAPolling Timing Diagram



All the address loaded should be within the top 4MByte,FFFFFFFF to FFC00000, or within the bottom 1MByte, 000FFFFF to 000E0000.

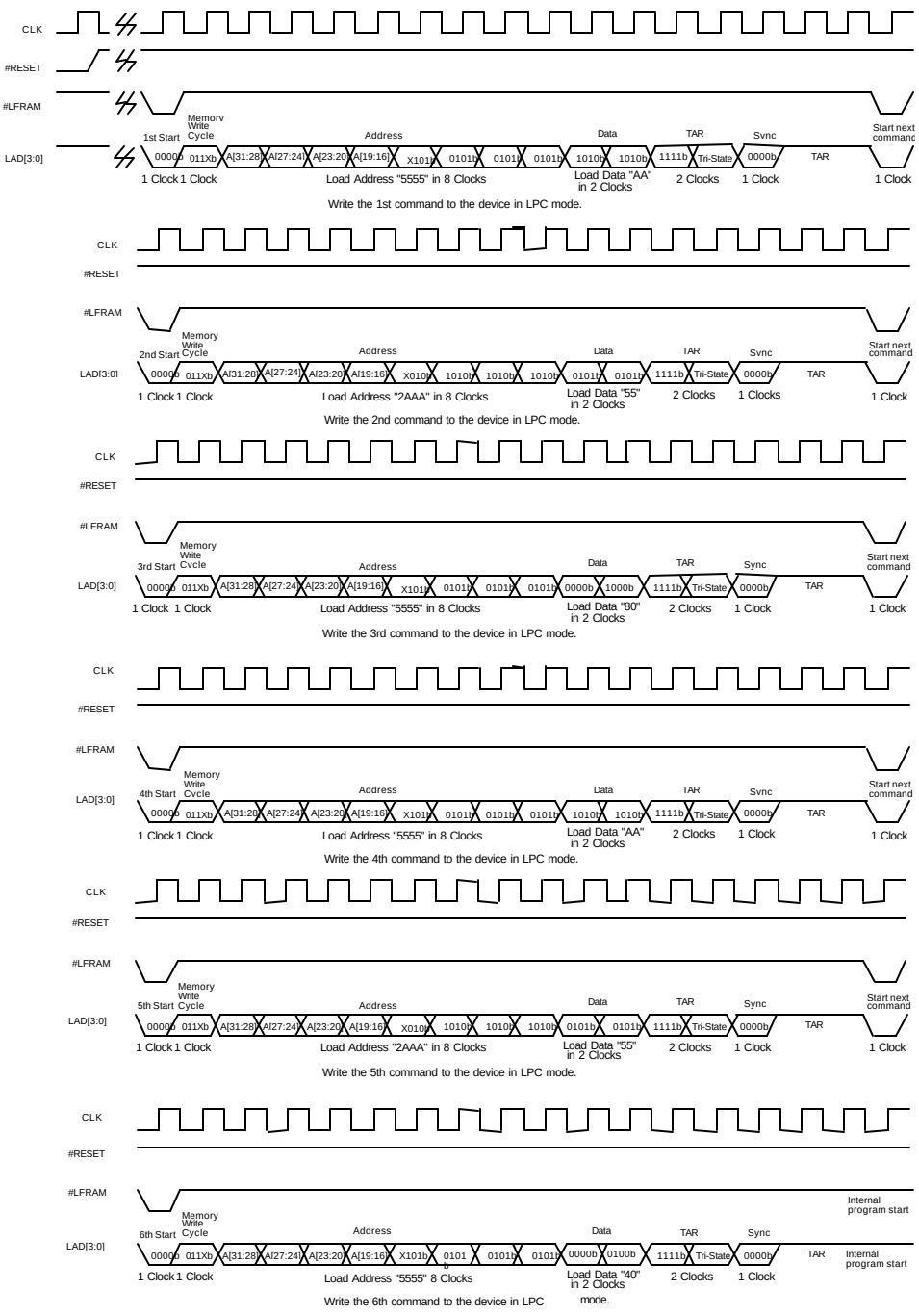
Timing Waveforms for LPC Interface Mode, continued

Toggle Bit Timing Diagram



Timing Waveforms for LPC Interface Mode, continued

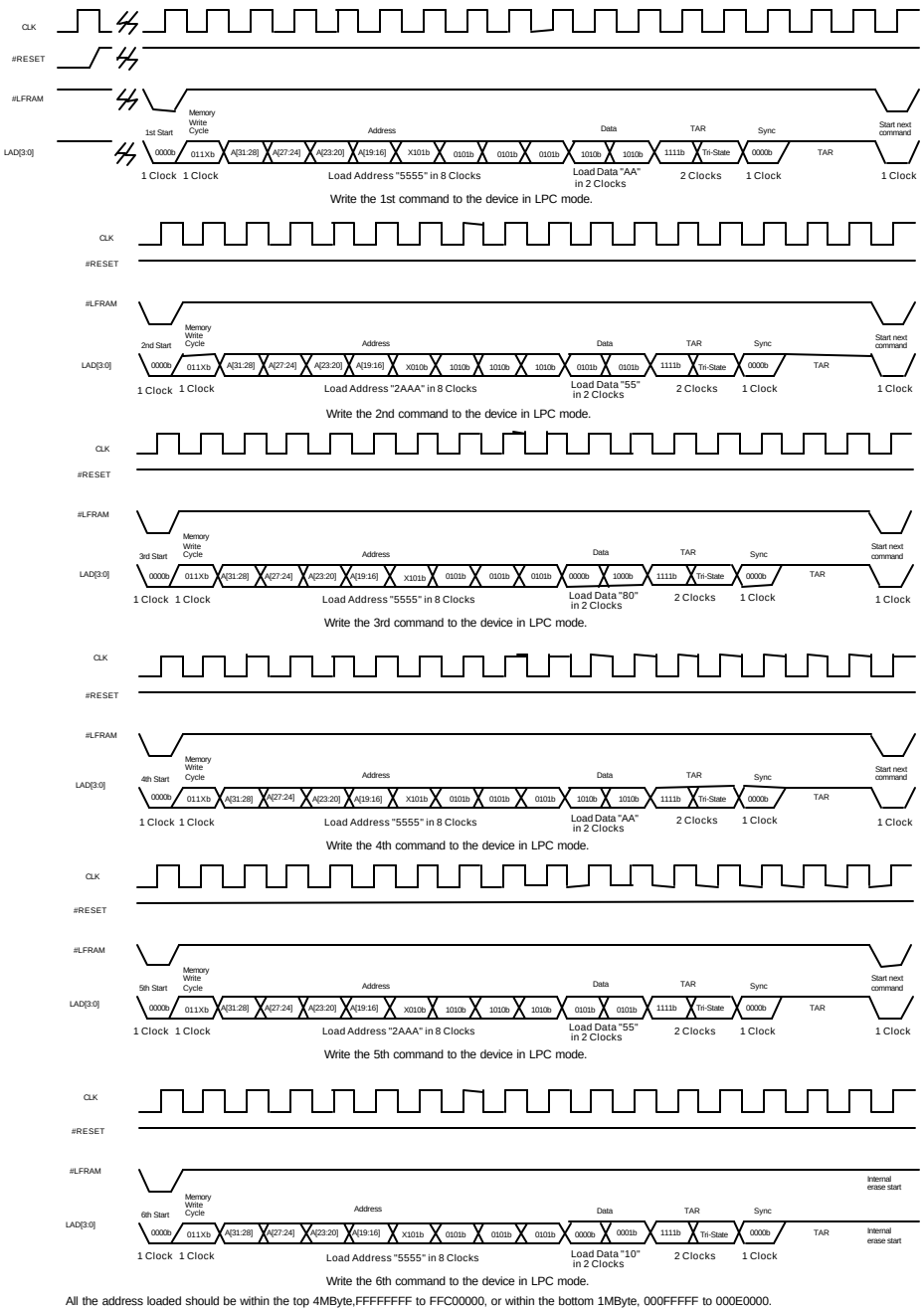
Boot Block Lockout Enable Timing Diagram



All the address loaded should be within the top 4MByte,FFFFFFFF to FFC00000, or within the bottom 1MByte, 000FFFFF to 000E0000.

Timing Waveforms for LPC Interface Mode, continued

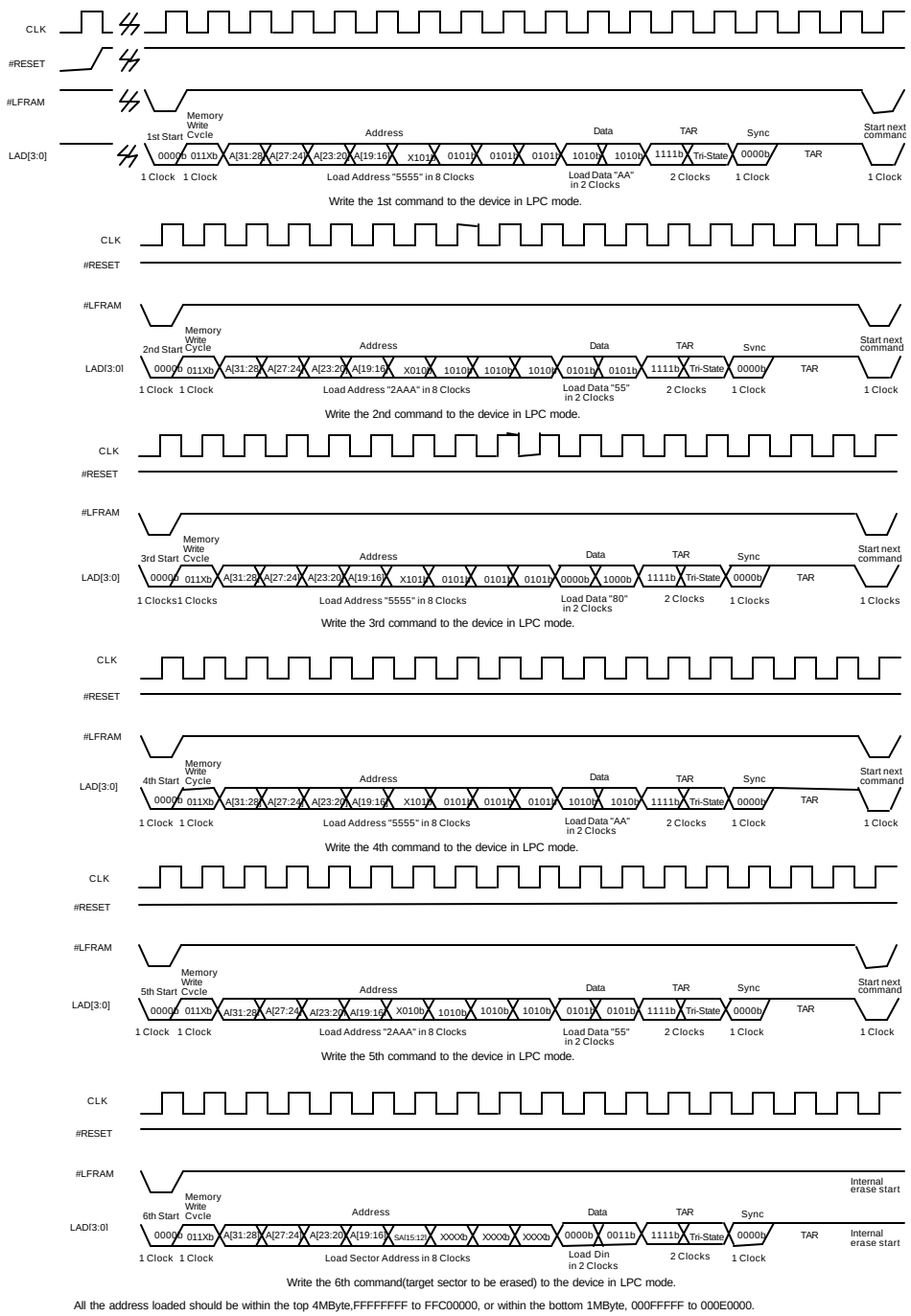
Chip Erase Timing Diagram



All the address loaded should be within the top 4MByte,FFFFFFFF to FFC00000, or within the bottom 1MByte, 000FFFFF to 000E0000.

Timing Waveforms for LPC Interface Mode, continued

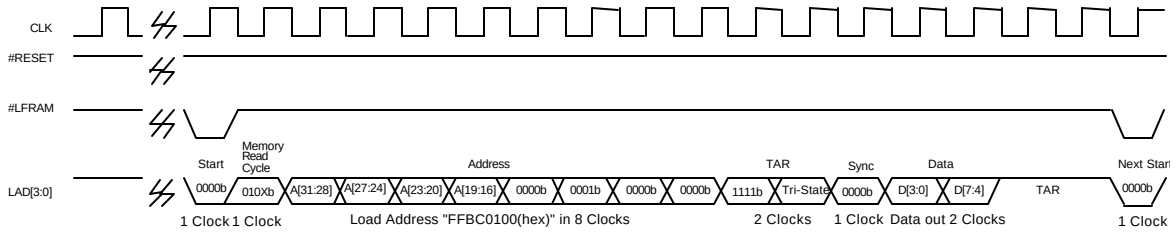
Sector Erase Timing Diagram



All the address loaded should be within the top 4MByte,FFFFFFFF to FFC00000, or within the bottom 1MByte, 000FFFFF to 000E0000.

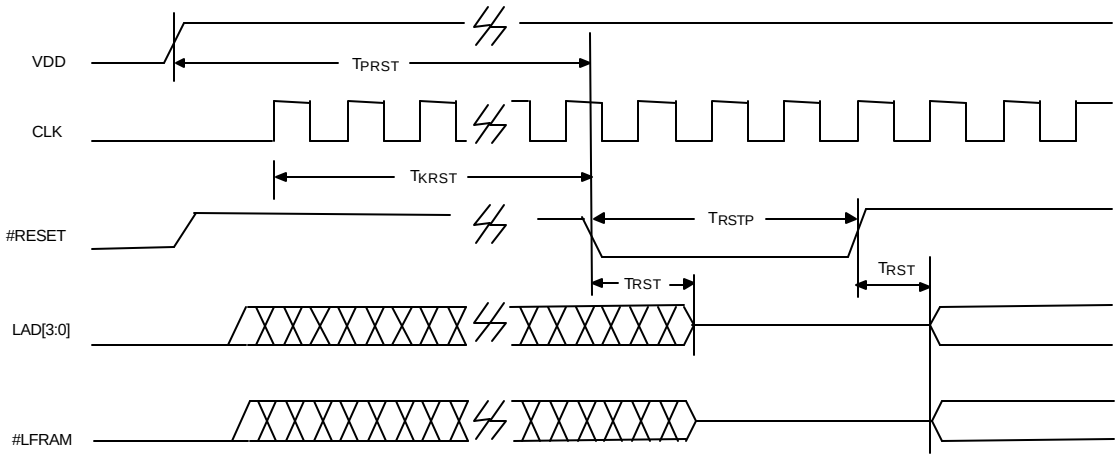
Timing Waveforms for LPC Interface Mode, continued

GPI Register Readout Timing Diagram



Note: Read the DQ[4:0] to capture the states(High or Low) of the GPI[4:0] input pins. The DQ[7:5] are reserved pins.

Reset Timing Diagram



ORDERING INFORMATION

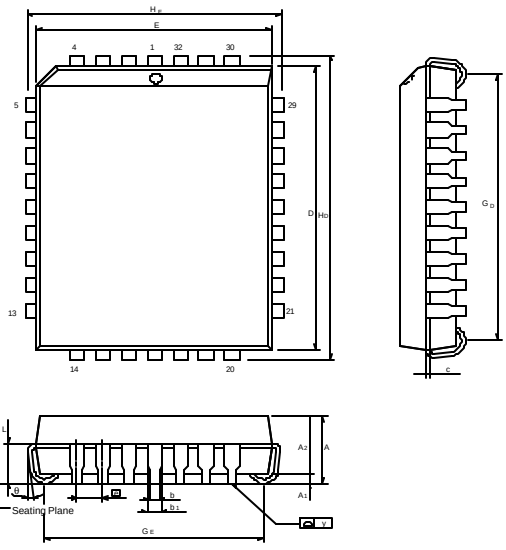
PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY VDD CURRENT MAX. (μA)	PACKAGE
W49V002AP	11	25	20	32L PLCC
W49V002AQ	11	25	20	32L STSOP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

32L PLCC

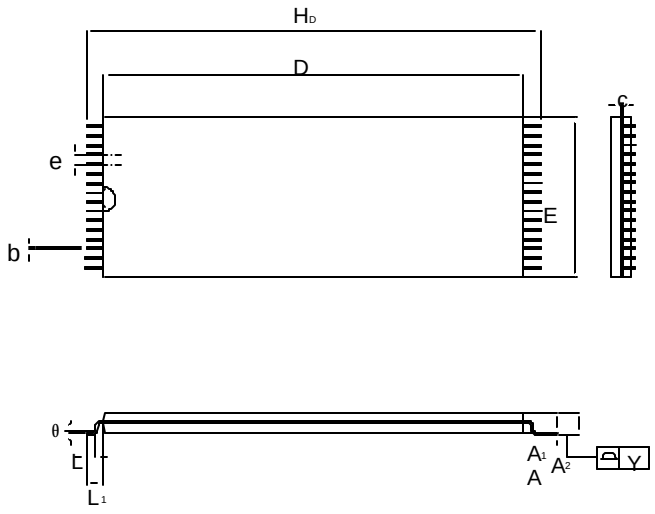


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.020	—	—	0.50	—	—
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
θ	0	—	10	0	—	10

Notes:

1. Dimensions D & E do not include interlead flasl
2. Dimension b1 does not include dambar protrusion/ir
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection sepc.

32L STSOP(8 x 14mm)



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			0.047			1.20
A_1	0.002		0.006	0.05		0.15
A_2	0.035	0.040	0.041	0.95	1.00	1.05
b	0.007	0.009	0.010	0.17	0.22	0.27
c	0.004	-----	0.008	0.10	-----	0.21
D		0.488			12.40	
E		0.315			8.00	
H_D		0.551			14.00	
e		0.020			0.50	
L	0.020	0.024	0.028	0.50	0.60	0.70
L_1		0.031			0.80	
Y	0.000		0.004	0.00		0.10
θ	0	3	5	0	3	5

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Apr. 2001	-	Initial Issued

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Note: All data and specifications are subject to change without notice.