

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- **DOC™ Circuitry Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation**
- **Dynamic Drive Capability Is Equivalent to Standard Outputs With  $I_{OH}$  and  $I_{OL}$  of  $\pm 24$  mA at 2.5-V  $V_{CC}$**
- **Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage**
- **If Either  $V_{CC}$  Input Is at GND, Both Ports Are in the High-Impedance State**
- **Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications**

- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.4-V to 3.6-V Power-Supply Range
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

This 16-bit (dual-octal) noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.4 V to 3.6 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.4 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCAH164245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the outputs so the buses are effectively isolated.

The SN74AVCAH164245 is designed so that the control pins (1DIR, 2DIR, 1 $\overline{OE}$ , and 2 $\overline{OE}$ ) are supplied by  $V_{CCA}$ . Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CCA}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. If either  $V_{CC}$  input is at GND, then both ports are in the high-impedance state.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	$SN74AVCAH164245GR$	AVCAH164245
	TVSOP – DGV	$SN74AVCAH164245VR$	WAH4245
	VFBGA – GQL	$SN74AVCAH164245KR$	WAH4245

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

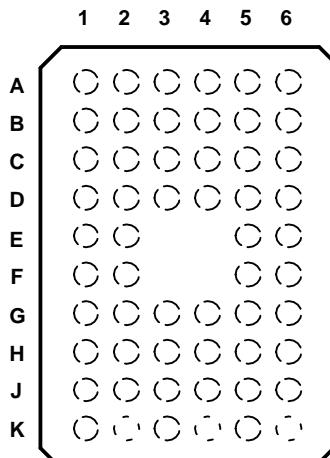
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## TERMINAL ASSIGNMENTS

DGG OR DGV PACKAGE  
(TOP VIEW)

1DIR	1	48	1 $\bar{OE}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V <sub>CCB</sub>	7	42	V <sub>CCA</sub>
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V <sub>CCB</sub>	18	31	V <sub>CCA</sub>
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	2 $\bar{OE}$

GQL PACKAGE  
(TOP VIEW)



TERMINAL ASSIGNMENTS<sup>(1)</sup>

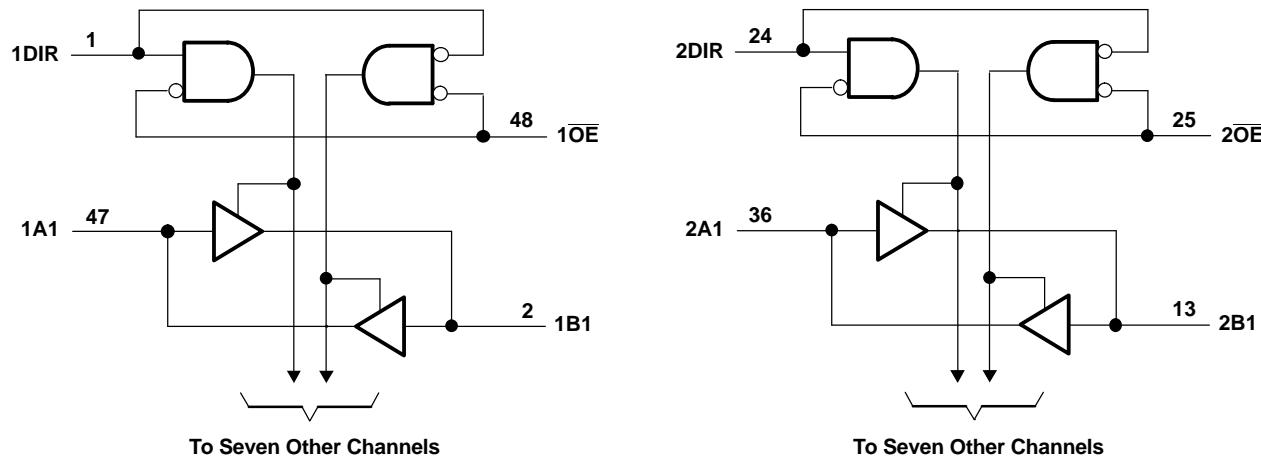
	1	2	3	4	5	6
<b>A</b>	1DIR	NC	NC	NC	NC	$\overline{1OE}$
<b>B</b>	1B2	1B1	GND	GND	1A1	1A2
<b>C</b>	1B4	1B3	$V_{CCB}$	$V_{CCA}$	1A3	1A4
<b>D</b>	1B6	1B5	GND	GND	1A5	1A6
<b>E</b>	1B8	1B7			1A7	1A8
<b>F</b>	2B1	2B2			2A2	2A1
<b>G</b>	2B3	2B4	GND	GND	2A4	2A3
<b>H</b>	2B5	2B6	$V_{CCB}$	$V_{CCA}$	2A6	2A5
<b>J</b>	2B7	2B8	GND	GND	2A8	2A7
<b>K</b>	2DIR	NC	NC	NC	NC	$\overline{2OE}$

(1) NC – No internal connection

FUNCTION TABLE  
(EACH 8-BIT SECTION)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

**LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers shown are for the DGG and DGV packages.

**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CCA}$ $V_{CCB}$	Supply voltage range	-0.5	4.6	V
$V_I$	I/O ports (A port)	-0.5	4.6	V
	I/O ports (B port)	-0.5	4.6	
	Control inputs	-0.5	4.6	
$V_O$	A port	-0.5	4.6	V
	B port	-0.5	4.6	
$V_O$	A port	-0.5	$V_{CCA} + 0.5$	V
	B port	-0.5	$V_{CCB} + 0.5$	
$I_{IK}$	$I_{IK}$ Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	$I_{OK}$ Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		$\pm 50$	mA
	Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND		$\pm 100$	mA
$\theta_{JA}$	DGG package	70		°C/W
	DGV package	58		
	GQL package	28		
$T_{stg}$	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)(2)(3)</sup>**

		$V_{CCI}$	$V_{CCO}$	MIN	MAX	UNIT
$V_{CCA}$	Supply voltage			1.4	3.6	V
$V_{CCB}$	Supply voltage			1.4	3.6	V
$V_{IH}$	High-level input voltage	Data inputs	1.4 V to 1.95 V	$V_{CCI} \times 0.65$	V	
			1.95 V to 2.7 V	1.7		
			2.7 V to 3.6 V	2		
$V_{IL}$	Low-level input voltage	Data inputs	1.4 V to 1.95 V	$V_{CCI} \times 0.35$	V	
			1.95 V to 2.7 V	0.7		
			2.7 V to 3.6 V	0.8		
$V_{IH}$	High-level input voltage	Control inputs (referenced to $V_{CCA}$ )	1.4 V to 1.95 V	$V_{CCA} \times 0.65$	V	
			1.95 V to 2.7 V	1.7		
			2.7 V to 3.6 V	2		
$V_{IL}$	Low-level input voltage	Control inputs (referenced to $V_{CCA}$ )	1.4 V to 1.95 V	$V_{CCA} \times 0.35$	V	
			1.95 V to 2.7 V	0.7		
			2.7 V to 3.6 V	0.8		
$V_I$	Input voltage			0	3.6	V
$V_O$	Output voltage	Active state		0	$V_{CCO}$	V
		3-state		0	3.6	
$I_{OH}$	High-level output current		1.4 V to 1.6 V		-2	mA
			1.65 V to 1.95 V		-4	
			2.3 V to 2.7 V		-8	
			3 V to 3.6 V		-12	
$I_{OL}$	Low-level output current		1.4 V to 1.6 V		2	mA
			1.65 V to 1.95 V		4	
			2.3 V to 2.7 V		8	
			3 V to 3.6 V		12	
$\Delta t/\Delta V$	Input transition rise or fall rate				5	ns/V
$T_A$	Operating free-air temperature			-40	85	°C

(1)  $V_{CCI}$  is the  $V_{CC}$  associated with the data input port.

(2)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

(3) All unused data inputs of the device must be held at  $V_{CCI}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74AVCAH164245

16-BIT DUAL-SUPPLY BUS TRANSCEIVER  
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES396A–JULY 2002–REVISED JUNE 2005

Electrical Characteristics<sup>(1)(2)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP <sup>(3)</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 $\mu$ A, V <sub>I</sub> = V <sub>IH</sub>		1.4 V to 3.6 V	1.4 V to 3.6 V	V <sub>CCO</sub> – 0.2 V			V
	I <sub>OH</sub> = -2 mA, V <sub>I</sub> = V <sub>IH</sub>		1.4 V	1.4 V		1.05		
	I <sub>OH</sub> = -4 mA, V <sub>I</sub> = V <sub>IH</sub>		1.65 V	1.65 V		1.2		
	I <sub>OH</sub> = -8 mA, V <sub>I</sub> = V <sub>IH</sub>		2.3 V	2.3 V		1.75		
	I <sub>OH</sub> = -12 mA, V <sub>I</sub> = V <sub>IH</sub>		3 V	3 V		2.3		
V <sub>OL</sub>	I <sub>OH</sub> = 100 $\mu$ A, V <sub>I</sub> = V <sub>IL</sub>		1.4 V to 3.6 V	1.4 V to 3.6 V		0.2		V
	I <sub>OH</sub> = 2 mA, V <sub>I</sub> = V <sub>IL</sub>		1.4 V	1.4 V		0.35		
	I <sub>OH</sub> = 4 mA, V <sub>I</sub> = V <sub>IL</sub>		1.65 V	1.65 V		0.45		
	I <sub>OH</sub> = 8 mA, V <sub>I</sub> = V <sub>IL</sub>		2.3 V	2.3 V		0.55		
	I <sub>OH</sub> = 12 mA, V <sub>I</sub> = V <sub>IL</sub>		3 V	3 V		0.7		
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	1.4 V to 3.6 V	3.6 V		±2.5	$\mu$ A	
I <sub>BHL</sub> <sup>(4)</sup>	V <sub>I</sub> = 0.49 V		1.4 V	1.4 V		11		$\mu$ A
	V <sub>I</sub> = 0.57 V		1.65 V	1.65 V		30		
	V <sub>I</sub> = 0.7 V		2.3 V	2.3 V		45		
	V <sub>I</sub> = 0.8 V		3 V	3 V		75		
I <sub>BHH</sub> <sup>(5)</sup>	V <sub>I</sub> = 0.91 V		1.4 V	1.4 V		-11		$\mu$ A
	V <sub>I</sub> = 1.07 V		1.65 V	1.65 V		-30		
	V <sub>I</sub> = 1.7 V		2.3 V	2.3 V		-45		
	V <sub>I</sub> = 2 V		3 V	3 V		-75		
I <sub>BHLO</sub> <sup>(6)</sup>	V <sub>I</sub> = 0 to V <sub>CC</sub>		1.6 V	1.6 V		100		$\mu$ A
			1.95 V	1.95 V		200		
			2.7 V	2.7 V		300		
			3.6 V	3.6 V		525		
I <sub>BHHO</sub> <sup>(7)</sup>	V <sub>I</sub> = 0 to V <sub>CC</sub>		1.6 V	1.6 V		-100		$\mu$ A
			1.95 V	1.95 V		-200		
			2.7 V	2.7 V		-300		
			3.6 V	3.6 V		-525		
I <sub>off</sub>	A port	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V	0 V	0 to 3.6 V		±10		$\mu$ A
	B port		0 to 3.6 V	0 V		±10		
I <sub>OZ</sub> <sup>(8)</sup>	A or B ports	V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>I</sub> = V <sub>CCI</sub> or GND	$\overline{OE}$ = V <sub>IH</sub>	3.6 V	3.6 V		±12.5	$\mu$ A
	B port		$\overline{OE}$ = don't care	0 V	3.6 V		±12.5	
	A port		$\overline{OE}$ = don't care	3.6 V	0 V		±12.5	

(1) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.(2) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.(3) All typical values are at T<sub>A</sub> = 25°C.(4) The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub> max.(5) The bus-hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.(6) An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.(7) An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.(8) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**Electrical Characteristics<sup>(1)</sup>(continued)**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
I <sub>CCA</sub>	V <sub>I</sub> = V <sub>CC1</sub> or GND, I <sub>O</sub> = 0			1.6 V	1.6 V			20	μA	
				1.95 V	1.95 V			20		
				2.7 V	2.7 V			30		
				0 V	3.6 V			-40		
				3.6 V	0 V			40		
				3.6 V	3.6 V			40		
I <sub>CCB</sub>	V <sub>I</sub> = V <sub>CC1</sub> or GND, I <sub>O</sub> = 0			1.6 V	1.6 V			20	μA	
				1.95 V	1.95 V			20		
				2.7 V	2.7 V			30		
				0 V	3.6 V			40		
				3.6 V	0 V			-40		
				3.6 V	3.6 V			40		
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3.3 V or GND		3.3 V	3.3 V			4	pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 3.3 V or GND		3.3 V	3.3 V			5	pF	

 (1) V<sub>CC1</sub> is the V<sub>CC</sub> associated with the input port.

 (2) All typical values are at T<sub>A</sub> = 25°C.

**Switching Characteristics**

 over recommended operating free-air temperature range, V<sub>CCA</sub> = 1.5 V ± 0.1 V (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.5 V ± 0.1 V		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	B	1.7	6.7	1.9	6.3	1.8	5.5	1.7	5.8	ns
	B	A	1.8	6.8	2.2	7.4	2.1	7.6	2.1	7.3	
t <sub>en</sub>	OE	A	2.6	8.4	2.7	8.2	2.3	6.3	2.1	5.6	ns
		B	2.7	8.6	3.2	10.2	3.2	10.8	3.2	10.7	
t <sub>dis</sub>	OE	A	2.1	7	2.5	7	1.7	5.3	2	6.1	ns
		B	2.1	7.1	2.5	7.1	2.1	6.5	2.1	6.4	

**Switching Characteristics**

 over recommended operating free-air temperature range, V<sub>CCA</sub> = 1.8 V ± 0.15 V (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.5 V ± 0.1 V		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	B	1.7	6.4	1.8	6	1.7	4.7	1.6	4.3	ns
	B	A	1.4	5.5	1.8	6	1.8	5.8	1.8	5.5	
t <sub>en</sub>	OE	A	2.5	8	2.7	7.8	2.2	5.8	2	5.1	ns
		B	1.8	6.7	2.7	7.8	2.7	8.1	2.7	8.1	
t <sub>dis</sub>	OE	A	2.1	6.4	2.5	6.4	1.5	4.5	1.8	5	ns
		B	2.1	6.6	2.5	6.4	2	5.5	2	5.5	

SN74AVCAH164245

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**Switching Characteristics**
over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	1.6	6	1.8	5.6	1.5	4	1.4	3.4	ns
	B	A	1.3	4.6	1.7	4.4	1.5	4	1.4	3.7	
$t_{en}$	$\overline{OE}$	A	2.6	7.4	2.7	7.2	2.2	5.3	2	4.5	ns
		B	1.2	4.1	2.2	5.1	2.2	5.3	2.2	5.3	
$t_{dis}$	$\overline{OE}$	A	2	5.7	2.3	5.7	1.4	3.7	1.6	4	ns
		B	0.9	4.5	1.7	4.5	1.4	3.7	1.4	3.7	

**Switching Characteristics**
over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	1.5	5.9	1.7	5.4	1.5	3.7	1.4	3.1	ns
	B	A	1.3	4.5	1.6	3.8	1.5	3.3	1.4	3.1	
$t_{en}$	$\overline{OE}$	A	2.5	7	2.6	6.9	2.1	5	1.9	4.1	ns
		B	0.8	2.6	1.9	4	2	4.1	1.9	4.1	
$t_{dis}$	$\overline{OE}$	A	1.2	5.4	2.2	5.2	1.2	3.3	1.5	3.6	ns
		B	1.2	5.4	1.7	4.4	1.5	3.6	1.5	3.6	

**Operating Characteristics**
 $V_{CCA}$  and  $V_{CCB} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

PARAMETER			TEST CONDITIONS				TYP	UNIT
$C_{pdA}$	Power dissipation capacitance per transceiver, A-port input, B-port output			Outputs enabled	$C_L = 0, f = 10 \text{ MHz}$	14	pF	
	Outputs disabled			Outputs enabled		7		
	Power dissipation capacitance per transceiver, B-port input, A-port output			Outputs disabled		20		
	Outputs enabled			Outputs disabled		7		
$C_{pdB}$	Power dissipation capacitance per transceiver, A-port input, B-port output			Outputs enabled	$C_L = 0, f = 10 \text{ MHz}$	14	pF	
	Outputs disabled			Outputs enabled		7		
	Power dissipation capacitance per transceiver, B-port input, A-port output			Outputs disabled		20		
	Outputs enabled			Outputs disabled		7		

## Output Description

The DOC™ circuitry is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical  $V_{OL}$  vs  $I_{OL}$  and  $V_{OH}$  vs  $I_{OH}$  curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

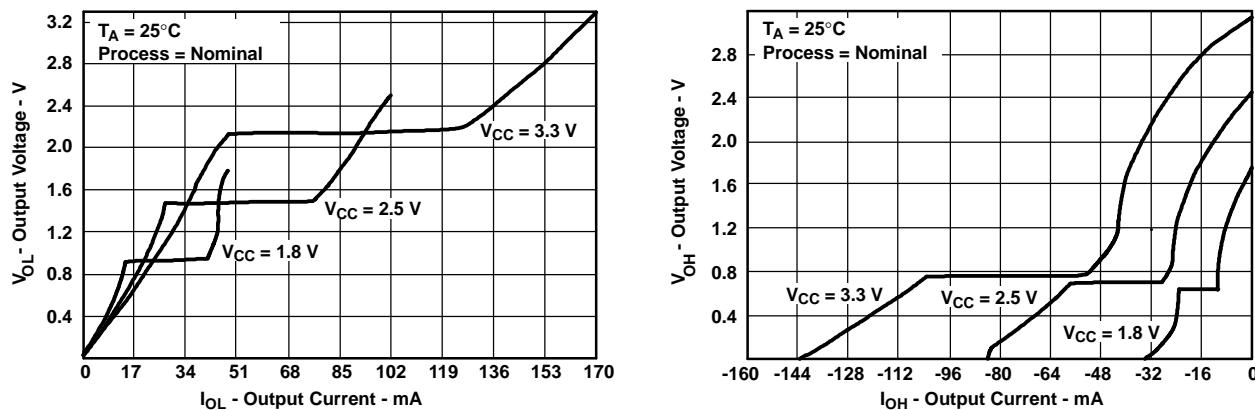
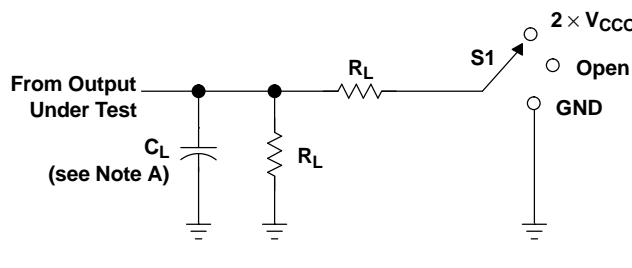


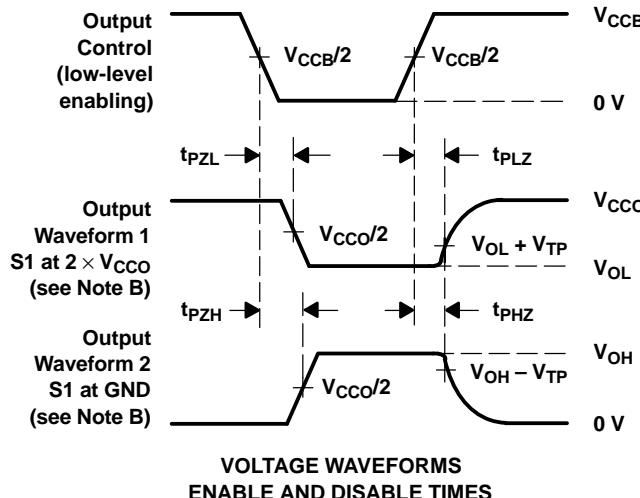
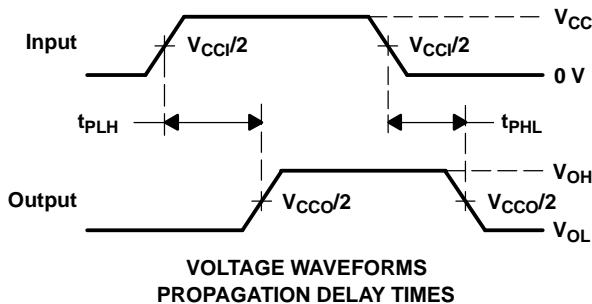
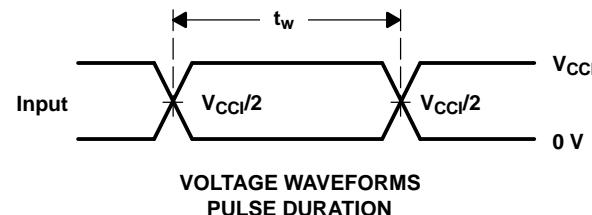
Figure 1. Output Voltage vs Output Current

**PARAMETER MEASUREMENT INFORMATION**



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CCO}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CCO}$	$C_L$	$R_L$	$V_{TP}$
$1.5 V \pm 0.1 V$	15 pF	2 k $\Omega$	0.1 V
$1.8 V \pm 0.15 V$	30 pF	1 k $\Omega$	0.15 V
$2.5 V \pm 0.2 V$	30 pF	500 $\Omega$	0.15 V
$3.3 V \pm 0.3 V$	30 pF	500 $\Omega$	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $dv/dt \geq 1$  V/ns.

D. The outputs are measured one at a time, with one transition per measurement.

E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

H.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.

I.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

**Figure 2. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
74AVCAH164245GRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCAH164245GRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCAH164245VRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCAH164245VRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74AVCAH164245ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
SN74AVCAH164245GR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AVCAH164245KR	OBsolete	BGA MICROSTAR JUNIOR	GQL	56		TBD	Call TI	Call TI	
SN74AVCAH164245VR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

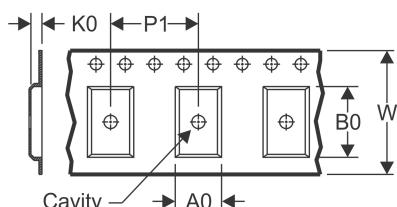
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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

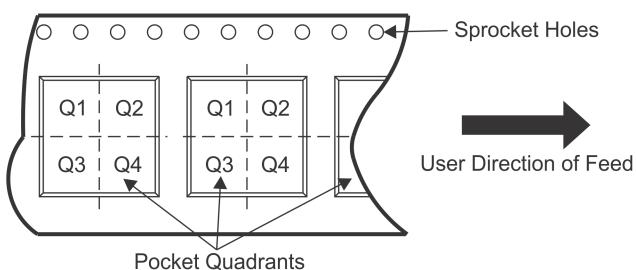
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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AVCAH164245ZQLR	BGA MLCROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
SN74AVCAH164245GR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74AVCAH164245VR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

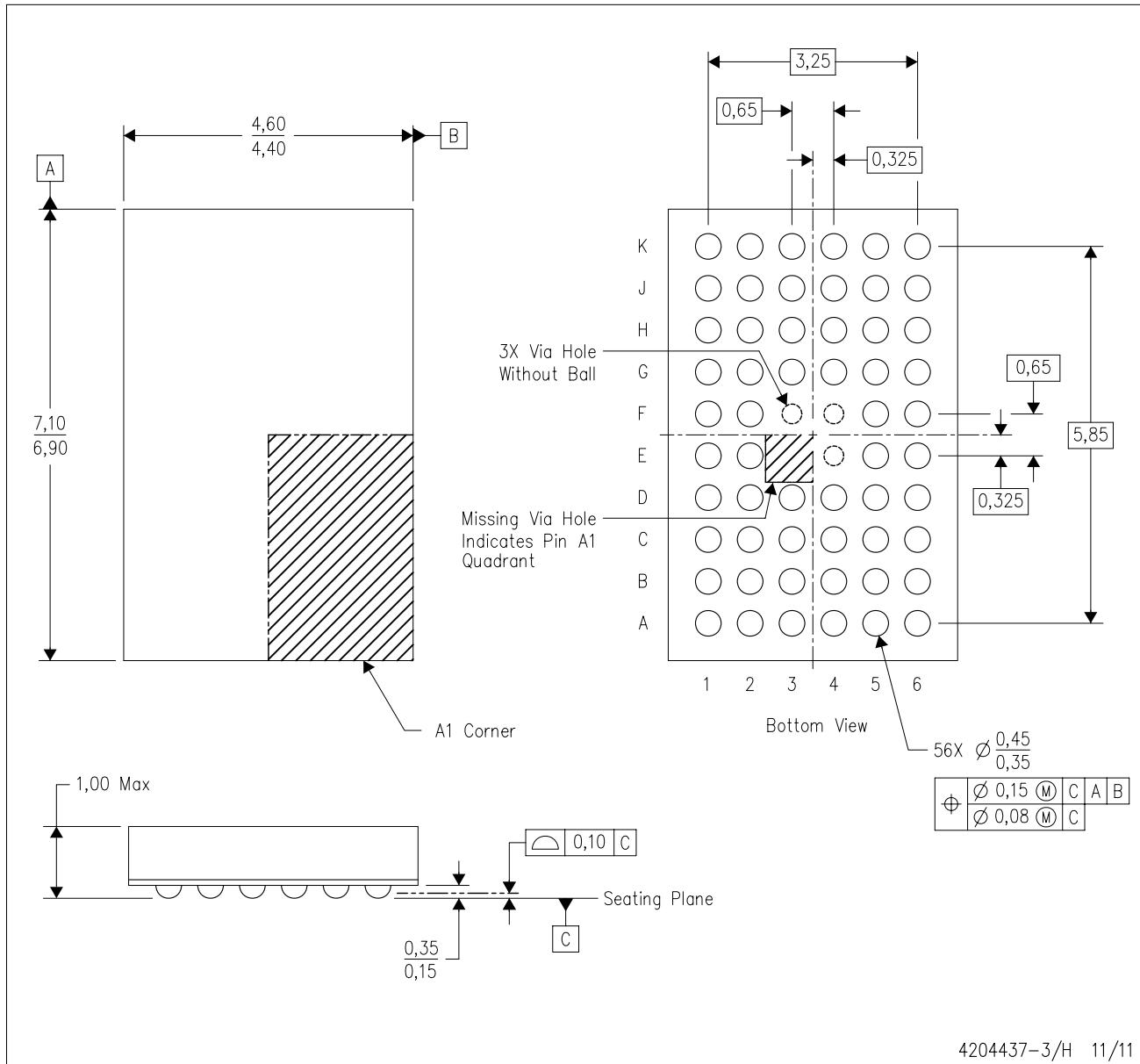
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AVCAH164245ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	333.2	345.9	28.6
SN74AVCAH164245GR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74AVCAH164245VR	TVSOP	DGV	48	2000	367.0	367.0	38.0

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Falls within JEDEC MO-285 variation BA-2.
- This package is Pb-free. Refer to the 56 QGL package (drawing 4200583) for tin-lead (SnPb).

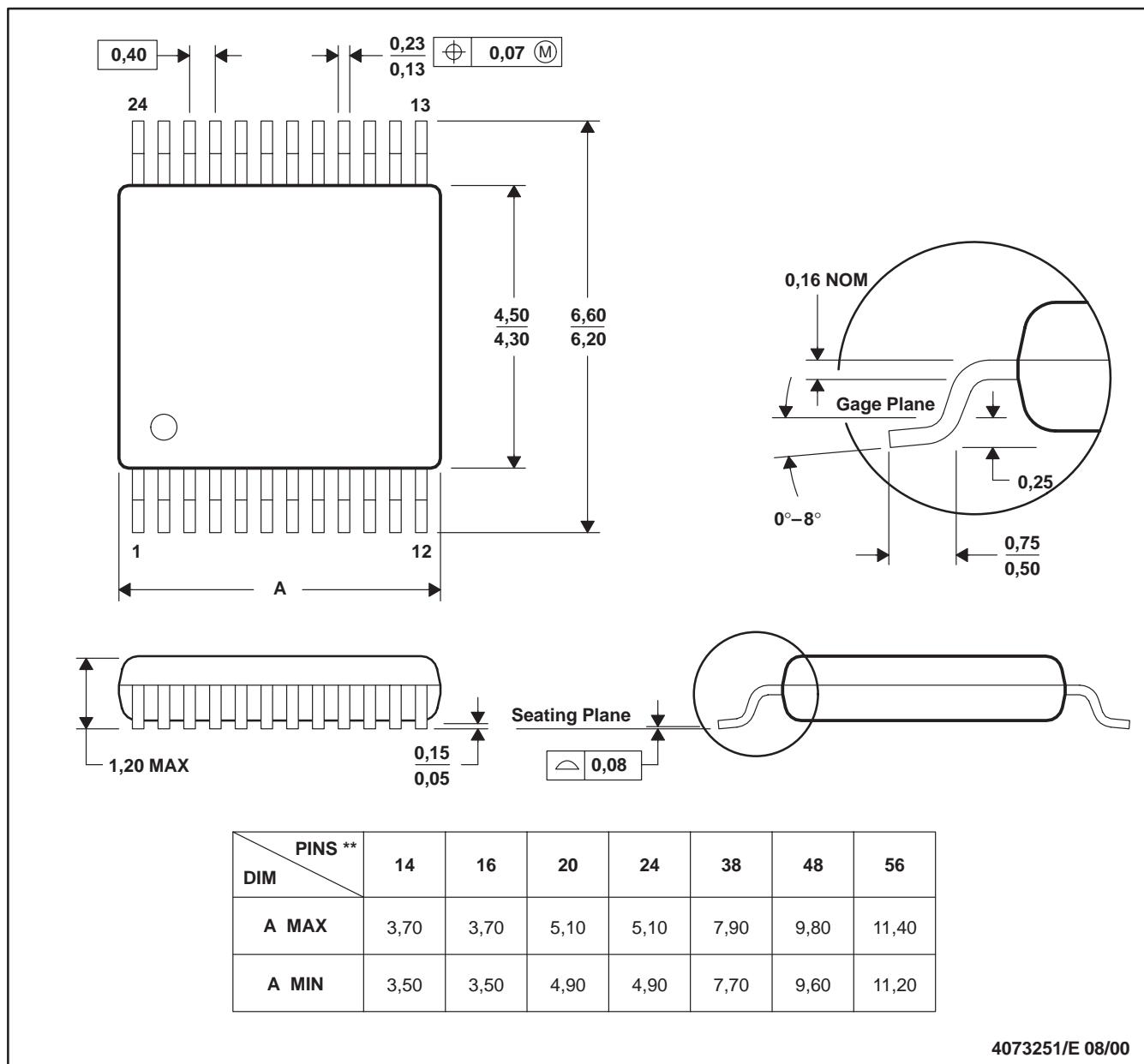
4204437-3/H 11/11

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## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

**24 PINS SHOWN**

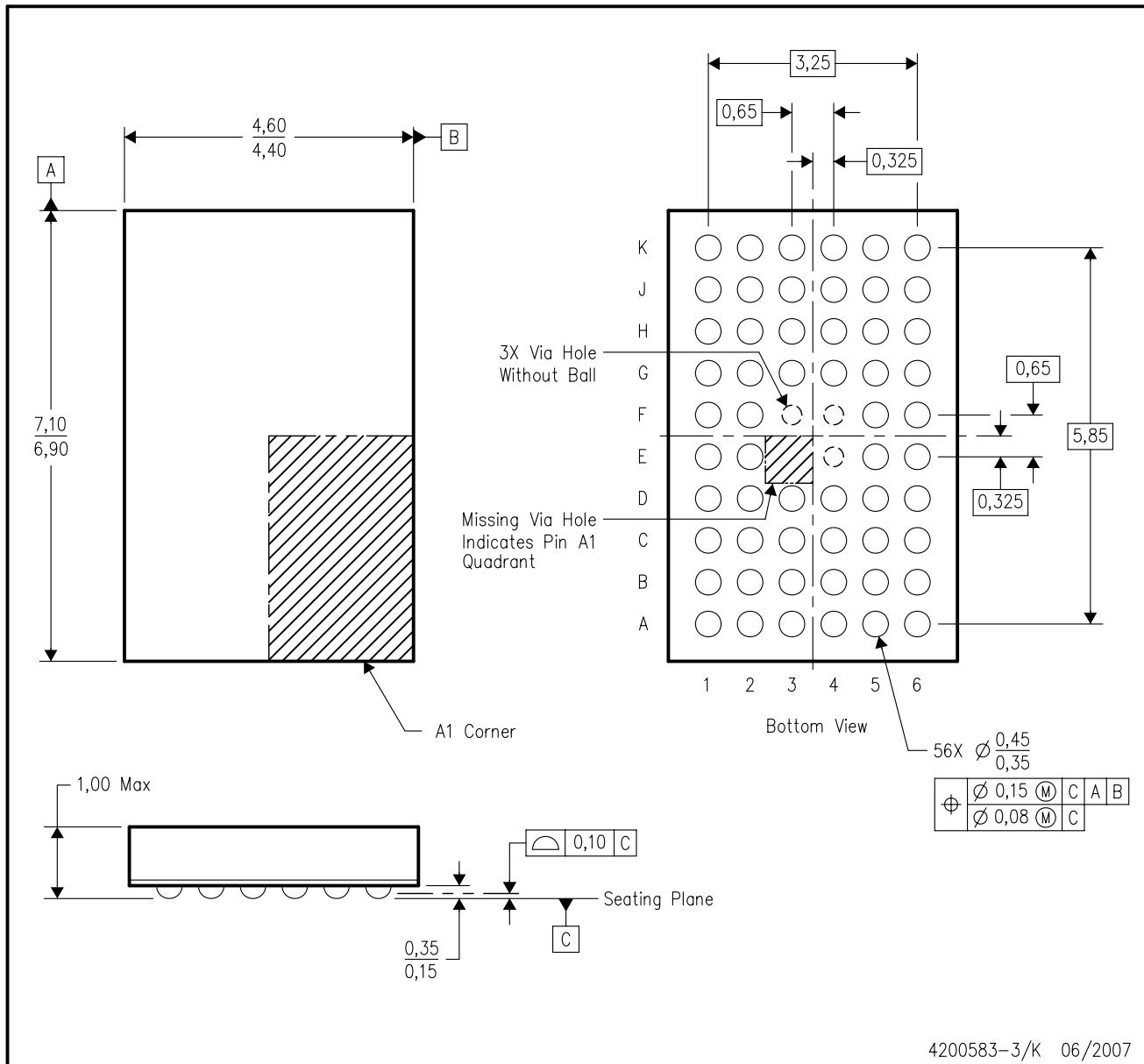


NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
D. Falls within JEDEC: 24/48 Pins – MO-153  
14/16/20/56 Pins – MO-194

14/16/20/56 Pins – MO-194

## GQL (R-PBGA-N56)

## PLASTIC BALL GRID ARRAY



4200583-3/K 06/2007

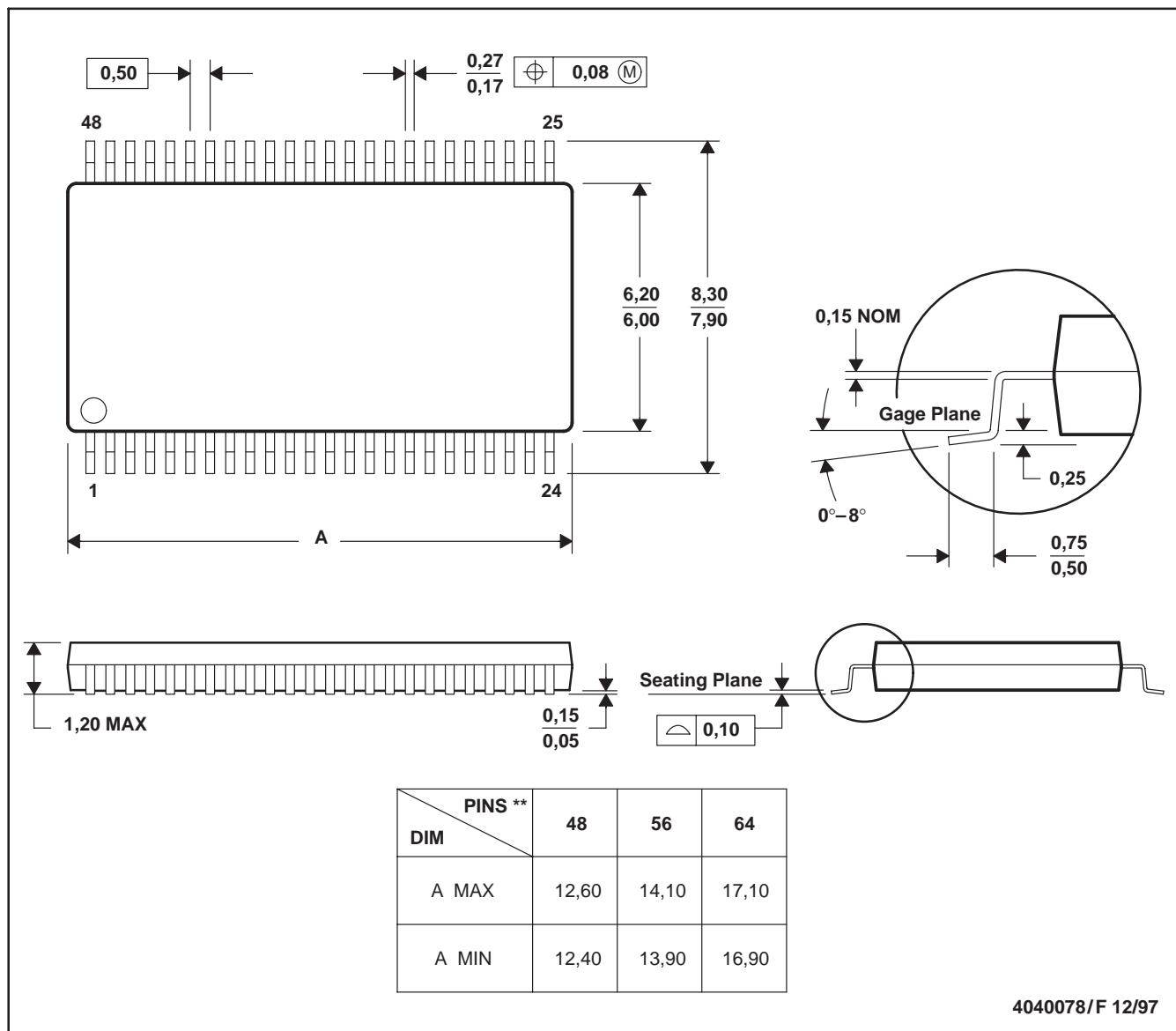
NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Falls within JEDEC MO-285 variation BA-2.
- This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
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Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
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