



ispLSI® 1032 Device Datasheet

September 2010

All Devices Discontinued!

Product Change Notifications (PCNs) have been issued to discontinue all devices in this data sheet.

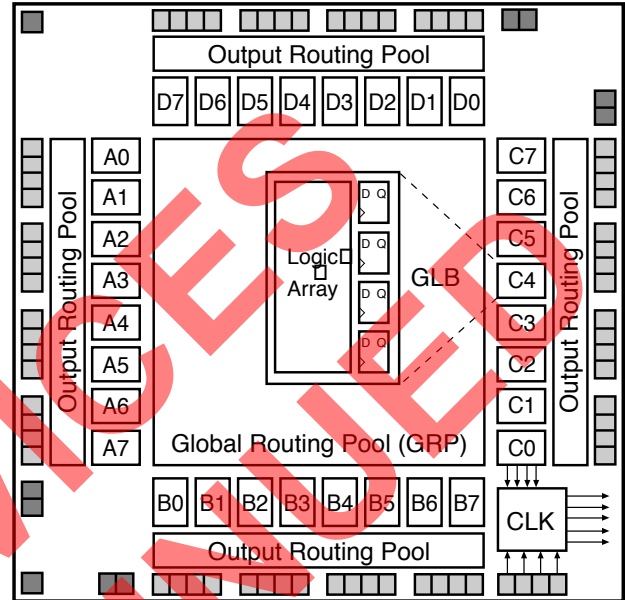
The original datasheet pages have not been modified and do not reflect those changes. Please refer to the table below for reference PCN and current product status.

Product Line	Ordering Part Number	Product Status	Reference PCN
ispLSI 1032	ispLSI 1032-60LT	Discontinued	PCN#13-10
	ispLSI 1032-80LT		
	ispLSI 1032-90LT		
	ispLSI 1032-60LTI		
	ispLSI 1032-60LJ		
	ispLSI 1032-80LJ		
	ispLSI 1032-90LJ		
	ispLSI 1032-60LJI		
	ispLSI 1016-60LH/883		PCN#05A-10
	5962-9476201MXC		

Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
 - High Speed Global Interconnect
 - 6000 PLD Gates
 - 64 I/O Pins, Eight Dedicated Inputs
 - 192 Registers
 - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
 - Small Logic Block Size for Fast Random Logic
 - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - $f_{max} = 90$ MHz Maximum Operating Frequency
 - $f_{max} = 60$ MHz for Industrial and Military/883 Devices
 - $t_{pd} = 12$ ns Propagation Delay
 - TTL Compatible Inputs and Outputs
 - Electrically Erasable and Reprogrammable
 - Non-Volatile E²CMOS Technology
 - 100% Tested
- **IN-SYSTEM PROGRAMMABLE**
 - In-System Programmable[™] (ISP[™]) 5-Volt Only
 - Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality
 - Reprogram Soldered Devices for Faster Prototyping
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
 - Complete Programmable Device Can Combine Glue Logic and Structured Designs
 - Four Dedicated Clock Input Pins
 - Synchronous and Asynchronous Clocks
 - Flexible Pin Placement
 - Optimized Global Routing Pool Provides Global Interconnectivity

Functional Block Diagram



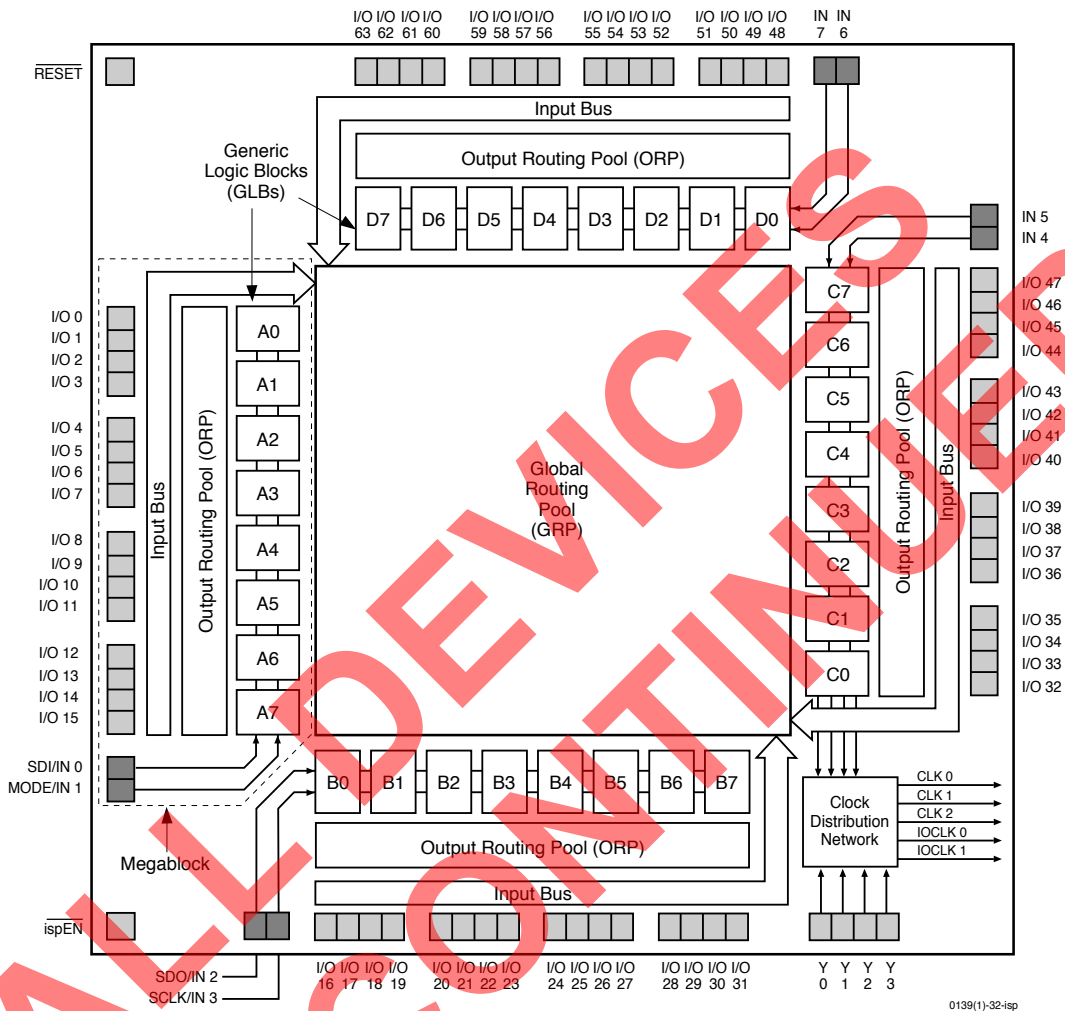
Description

The ispLSI 1032 is a High-Density Programmable Logic Device containing 192 Registers, 64 Universal I/O pins, eight Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1032 features 5-Volt in-system programming and in-system diagnostic capabilities. It is the first device which offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 1032 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. D7 (see figure 1). There are a total of 32 GLBs in the ispLSI 1032 device. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

Functional Block Diagram

Figure 1. ispLSI 1032 Functional Block Diagram



The device also has 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The I/O cells within the Megablock also share a common Output Enable (OE) signal. The ispLSI 1032 device contains four of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 1032 device are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (C0 on the ispLSI 1032 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings ¹

Supply Voltage V_{CC} -0.5 to +7.0V
 Input Voltage Applied -2.5 to $V_{CC} + 1.0V$
 Off-State Output Voltage Applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temp. with Power Applied -55 to 125°C
 Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
V _{CC}	Supply Voltage	Commercial T _A = 0°C to +70°C	4.75	5.25	V
		Industrial T _A = -40°C to +85°C	4.5	5.5	
		Military/883 T _C = -55°C to +125°C	4.5	5.5	
V _{IL}	Input Low Voltage		0	0.8	V
V _{IH}	Input High Voltage		2.0	V _{CC} + 1	V

Table 2- 0005Aisp w/mil.eps

Capacitance ($T_A=25^\circ\text{C}$, $f=1.0$ MHz)

SYMBOL	PARAMETER		□□MAXIMUM	UNITS	TEST CONDITIONS
C ₁	Dedicated Input Capacitance	Commercial/Industrial	8	pf	V _{CC} =5.0V, V _{IN} =2.0V
		Military	10	pf	V _{CC} =5.0V, V _{IN} =2.0V
C ₂	I/O and Clock Capacitance		10	pf	V _{CC} =5.0V, V _{I/O} , V _Y =2.0V

1. Guaranteed but not 100% tested.

Table 2- 0006

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	—	Years
Erase/Reprogram Cycles	10000	—	Cycles

Table 2- 0008B

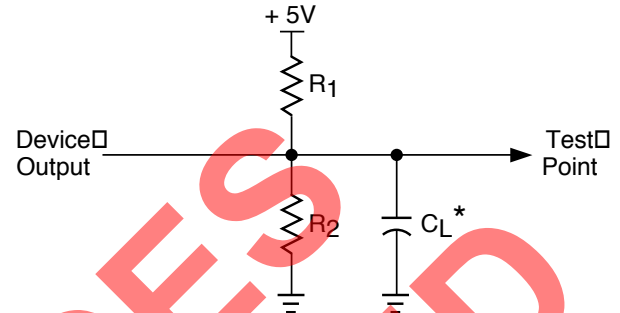
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	$\leq 3\text{ns}$ 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

Table 2- 0003

Figure 2. Test Load



* C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition	R1	R2	CL
A	470 Ω	390 Ω	35pF
B	470 Ω	390 Ω	Active High 35pF
			Active Low 35pF
C	470 Ω	390 Ω	Active High to Z at $V_{OH} - 0.5\text{V}$ 5pF
			Active Low to Z at $V_{OL} + 0.5\text{V}$ 5pF

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ³	MAX.	UNITS
VOL	Output Low Voltage	$I_{OL} = 8\text{ mA}$	—	—	0.4	V
VOH	Output High Voltage	$I_{OH} = -4\text{ mA}$	2.4	—	—	V
IIL	Input or I/O Low Leakage Current	$0\text{V} \leq V_{IN} \leq V_{IL} (\text{MAX.})$	—	—	-10	μA
IIH	Input or I/O High Leakage Current	$3.5\text{V} \leq V_{IN} \leq V_{CC}$	—	—	10	μA
IIL-isp	isp Input Low Leakage Current	$0\text{V} \leq V_{IN} \leq V_{IL} (\text{MAX.})$	—	—	-150	μA
IIL-PU	I/O Active Pull-Up Current	$0\text{V} \leq V_{IN} \leq V_{IL}$	—	—	-150	μA
IOS1	Output Short Circuit Current	$V_{CC} = 5\text{V}, V_{OUT} = 0.5\text{V}$	—	—	-200	mA
ICC^{2,4}	Operating Power Supply Current	$V_{IL} = 0.5\text{V}, V_{IH} = 3.0\text{V}$ $f_{\text{TOGGLE}} = 1\text{ MHz}$	Commercial	130	190	mA
			Industrial/Military	135	220	mA

Table 2- 0007A-32-isp

- One output at a time for a maximum duration of one second.
- Measured using eight 16-bit counters.
- Typical values are at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.
- Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC} .

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST ⁵ COND.	# ²	DESCRIPTION ¹	-90		-80		-60		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	—□	12	—□	15	—□	20	ns
t _{pd2}	A	2	Data Propagation Delay, Worst Case Path	—□	17	—□	20	—□	25	ns
f _{max} (Int.)	A	3	Clock Frequency with Internal Feedback ³	90.9	—□	80	—□	60	—□	MHz
f _{max} (Ext.)	—□	4	Clock Frequency with External Feedback ³ $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	58.8	—□	50	—□	38	—□	MHz
f _{max} (Tog.)	—□	5	Clock Frequency, Max Toggle ⁴	125	—□	100	—□	83	—□	MHz
t _{su1}	—□	6	GLB Reg. Setup Time before Clock, 4PT bypass	6	—□	7	—□	9	—□	ns
t _{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	—□	8	—□	10	—□	13	ns
t _{h1}	—□	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	—□	0	—□	0	—□	ns
t _{su2}	—□	9	GLB Reg. Setup Time before Clock	9	—□	10	—□	13	—□	ns
t _{co2}	—□	10	GLB Reg. Clock to Output Delay	—□	10	—□	12	—□	16	ns
t _{h2}	—□	11	GLB Reg. Hold Time after Clock	0	—□	0	—□	0	—□	ns
t _{r1}	A	12	Ext. Reset Pin to Output Delay	—□	15	—□	17	—□	22.5	ns
t _{rw1}	—□	13	Ext. Reset Pulse Duration	10	—□	10	—□	13	—□	ns
t _{en}	B	14	Input to Output Enable	—□	15	—□	18	—□	24	ns
t _{dis}	C	15	Input to Output Disable	—□	15	—□	18	—□	24	ns
t _{wh}	—□	16	Ext. Sync. Clock Pulse Duration, High	4	—□	5	—□	6	—□	ns
t _{wl}	—□	17	Ext. Sync. Clock Pulse Duration, Low	4	—□	5	—□	6	—□	ns
t _{su5}	—□	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2	—□	2	—□	2.5	—□	ns
t _{h5}	—□	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	—□	6.5	—□	8.5	—□	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.

Table 2-0030-32/90,80,60C

2. Refer to Timing Model in this data sheet for further details.

3. Standard 16-Bit counter using GRP feedback.

4. f_{max} (Toggle) may be less than 1/(t_{wh} + t_{wl}). This is to allow for a clock duty cycle of other than 50%.

5. Reference Switching Test Conditions section.

Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-90		-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t _{iobp}	20	I/O Register Bypass	–	1.6	–	2.0	–	2.7	ns
t _{iolat}	21	I/O Latch Delay	–	2.4	–	3.0	–	4.0	ns
t _{iosu}	22	I/O Register Setup Time before Clock	4.8	–	5.5	–	7.3	–	ns
t _{ioh}	23	I/O Register Hold Time after Clock	2.1	–	1.0	–	1.3	–	ns
t _{ioco}	24	I/O Register Clock to Out Delay	–	2.4	–	3.0	–	4.0	ns
t _{ior}	25	I/O Register Reset to Out Delay	–	2.8	–	2.5	–	3.3	ns
t _{din}	26	Dedicated Input Delay	–	3.2	–	4.0	–	5.3	ns
GRP									
t _{grp1}	27	GRP Delay, 1 GLB Load	–	1.2	–	1.5	–	2.0	ns
t _{grp4}	28	GRP Delay, 4 GLB Loads	–	1.6	–	2.0	–	2.7	ns
t _{grp8}	29	GRP Delay, 8 GLB Loads	–	2.4	–	3.0	–	4.0	ns
t _{grp12}	30	GRP Delay, 12 GLB Loads	–	3.0	–	3.8	–	5.0	ns
t _{grp16}	31	GRP Delay, 16 GLB Loads	–	3.6	–	4.5	–	6.0	ns
t _{grp32}	32	GRP Delay, 32 GLB Loads	–	6.4	–	8.0	–	10.6	ns
GLB									
t _{4ptbp}	33	4 Product Term Bypass Path Delay	–	5.2	–	6.5	–	8.6	ns
t _{1ptxor}	34	1 Product Term/XOR Path Delay	–	5.7	–	7.0	–	9.3	ns
t _{20ptxor}	35	20 Product Term/XOR Path Delay	–	7.0	–	8.0	–	10.6	ns
t _{xoradj}	36	XOR Adjacent Path Delay ³	–	8.2	–	9.5	–	12.7	ns
t _{gbp}	37	GLB Register Bypass Delay	–	0.8	–	1.0	–	1.3	ns
t _{gsu}	38	GLB Register Setup Time before Clock	1.2	–	1.0	–	1.3	–	ns
t _{gh}	39	GLB Register Hold Time after Clock	3.6	–	4.5	–	6.0	–	ns
t _{gco}	40	GLB Register Clock to Output Delay	–	1.6	–	2.0	–	2.7	ns
t _{gr}	41	GLB Register Reset to Output Delay	–	2.0	–	2.5	–	3.3	ns
t _{ptre}	42	GLB Product Term Reset to Register Delay	–	8.0	–	10.0	–	13.3	ns
t _{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	7.8	–	9.0	–	12.0	ns
t _{ptck}	44	GLB Product Term Clock Delay	2.8	6.0	3.5	7.5	4.6	9.9	ns
ORP									
t _{orp}	45	ORP Delay	–	2.4	–	2.5	–	3.3	ns
t _{orpbp}	46	ORP Bypass Delay	–	0.4	–	0.5	–	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.

2. Refer to Timing Model in this data sheet for further details.

3. The XOR adjacent path can only be used by hard macros.

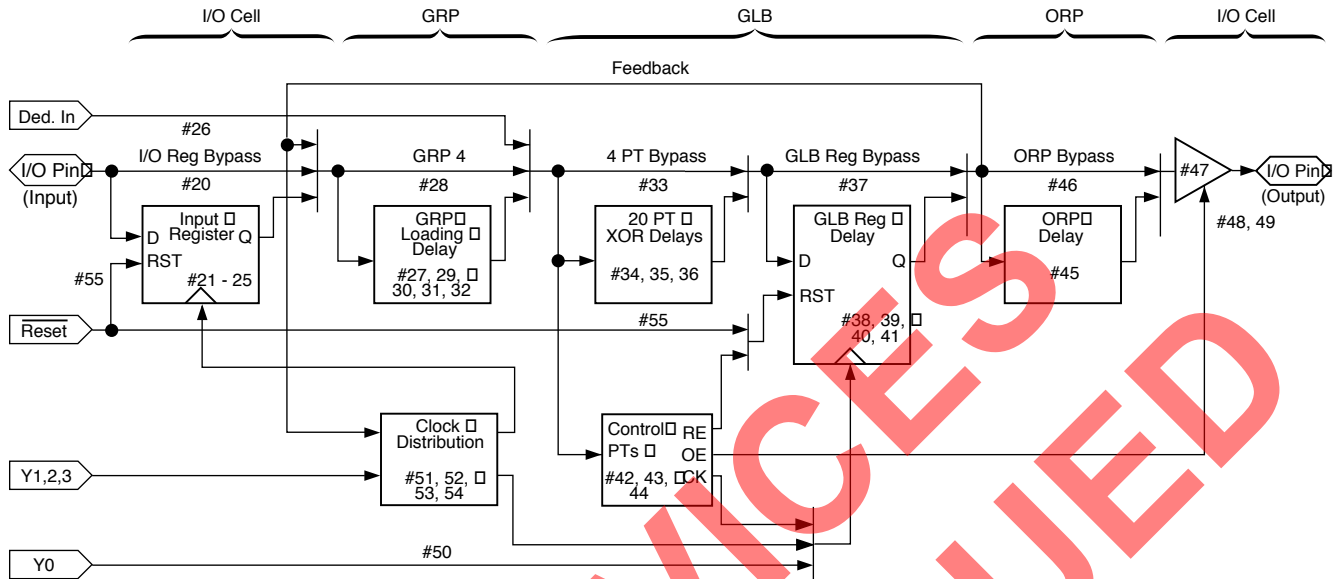
Internal Timing Parameters¹

PARAMETER	# ²	DESCRIPTION	-90		-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
tob	47	Output Buffer Delay	–	2.4	–	3.0	–	4.0	ns
toen	48	I/O Cell OE to Output Enabled	–	4.0	–	5.0	–	6.7	ns
todis	49	I/O Cell OE to Output Disabled	–	4.0	–	5.0	–	6.7	ns
Clocks									
tgy0	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	3.6	3.6	4.5	4.5	6.0	6.0	ns
tgy1/2	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.8	4.4	3.5	5.5	4.6	7.3	ns
tgcp	52	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	4.0	1.0	5.0	1.3	6.6	ns
tioy2/3	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	2.8	4.4	3.5	5.5	4.6	7.3	ns
tiocp	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	4.0	1.0	5.0	1.3	6.6	ns
Global Reset									
tgr	55	Global Reset to GLB and I/O Registers	–	8.2	–	9.0	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.

2. Refer to Timing Model in this data sheet for further details.

ispLSI 1032 Timing Model



Derivations of t_{su} , t_h and t_{co} from the Product Term Clock¹

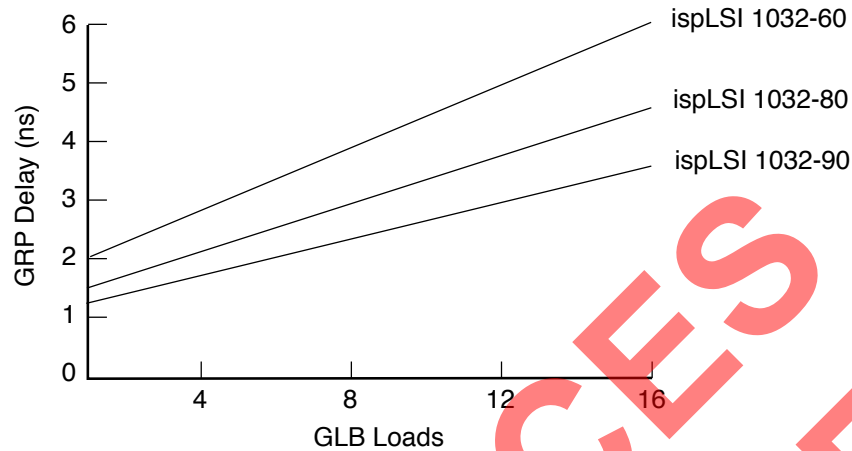
$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } su - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)}) \\
 &= (\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44) \\
 5.5 \text{ ns} &= (2.0 + 2.0 + 8.0) + (1.0) - (2.0 + 2.0 + 3.5) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35) \\
 4.0 \text{ ns} &= (2.0 + 2.0 + 7.5) + (4.5) - (2.0 + 2.0 + 8.0) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } co + \text{Output} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47) \\
 19.0 \text{ ns} &= (2.0 + 2.0 + 7.5) + (2.0) + (2.5 + 3.0)
 \end{aligned}$$

Derivations of t_{su} , t_h and t_{co} from the Clock GLB¹

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } su - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)}) \\
 &= (\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52) \\
 5.5 \text{ ns} &= (2.0 + 2.0 + 8.0) + (1.0) - (4.5 + 2.0 + 1.0) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35) \\
 4.0 \text{ ns} &= (4.5 + 2.0 + 5.0) + (4.5) - (2.0 + 2.0 + 8.0) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } co + \text{Output} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47) \\
 19.0 \text{ ns} &= (4.5 + 2.0 + 5.0) + (2.0) + (2.5 + 3.0)
 \end{aligned}$$

1. Calculations are based upon timing specifications for the ispLSI 1032-80.

Maximum GRP Delay vs GLB Loads

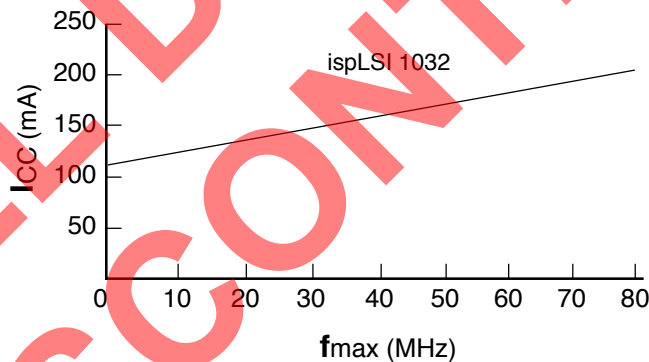


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Power Consumption

Power consumption in the ispLSI 1032 device depends on two primary factors: the speed at which the device is operating, and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of eight 16-bit Counters
Typical Current at 5V, 25°C

I_{CC} can be estimated for the ispLSI 1032 using the following equation:

$$I_{CC} = 52 + (\# \text{ of PTs} * 0.30) + (\# \text{ of nets} * \text{Max. freq} * 0.009) \text{ where:}$$

of PTs = Number of Product Terms used in design

of nets = Number of Signals used in device

Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions ($V_{CC} = 5.0V$, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A-32-80-isp

Pin Description

Name	PLCC Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 - IN 7	67, 84, 2, 19	Dedicated input pins to the device.
$\overline{\text{ispEN}}$	23	Input —Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0 ¹	25	Input —This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE/IN 1 ¹	42	Input —This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO/IN 2 ¹	44	Input/Output —This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK/IN 3 ¹	61	Input —This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
$\overline{\text{RESET}}$	24	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	20	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	66	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	63	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	62	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND VCC	1, 22, 43, 64 21, 65	Ground (GND) V _{CC}

1. Pins have dual function capability

Pin Description

Name	TQFP Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31, 32, 33, 34, 35, 36, 40, 41, 42, 43, 44, 45, 46, 47, 48, 53, 54, 55, 56, 57, 58, 59, 67, 68, 69, 70, 71, 72, 73, 78, 79, 80, 81, 82, 83, 84, 85, 86, 90, 91, 92, 93, 94, 95, 96, 97, 98, 3, 4, 5, 6, 7, 8, 9	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 - IN 7	66, 87, 89, 10	Dedicated input pins to the device.
ispEN	14	Input —Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0 ¹	16	Input —This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE/IN 1 ¹	37	Input —This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as a pin to control the operation of the isp state machine.
SDO/IN 2 ¹	39	Input/Output —This pin performs two functions. It is a dedicated input pin when ispEN is logic high. When ispEN is logic low, it functions as an output pin to read serial shift register data.
SCLK/IN 3 ¹	60	Input —This pin performs two functions. It is a dedicated input when ispEN is logic high. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register.
NC ²	1, 2, 24, 25, 26, 27, 49, 50, 51, 52, 74, 75, 76, 77, 99, 100	No Connect
RESET	15	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	11	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	65	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	62	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	61	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND VCC	13, 38, 63, 88 12, 64	Ground (GND) V _{CC}

1. Pins have dual function capability

2. NC pins are not to be connected to any active signals, Vcc or GND.

Pin Description

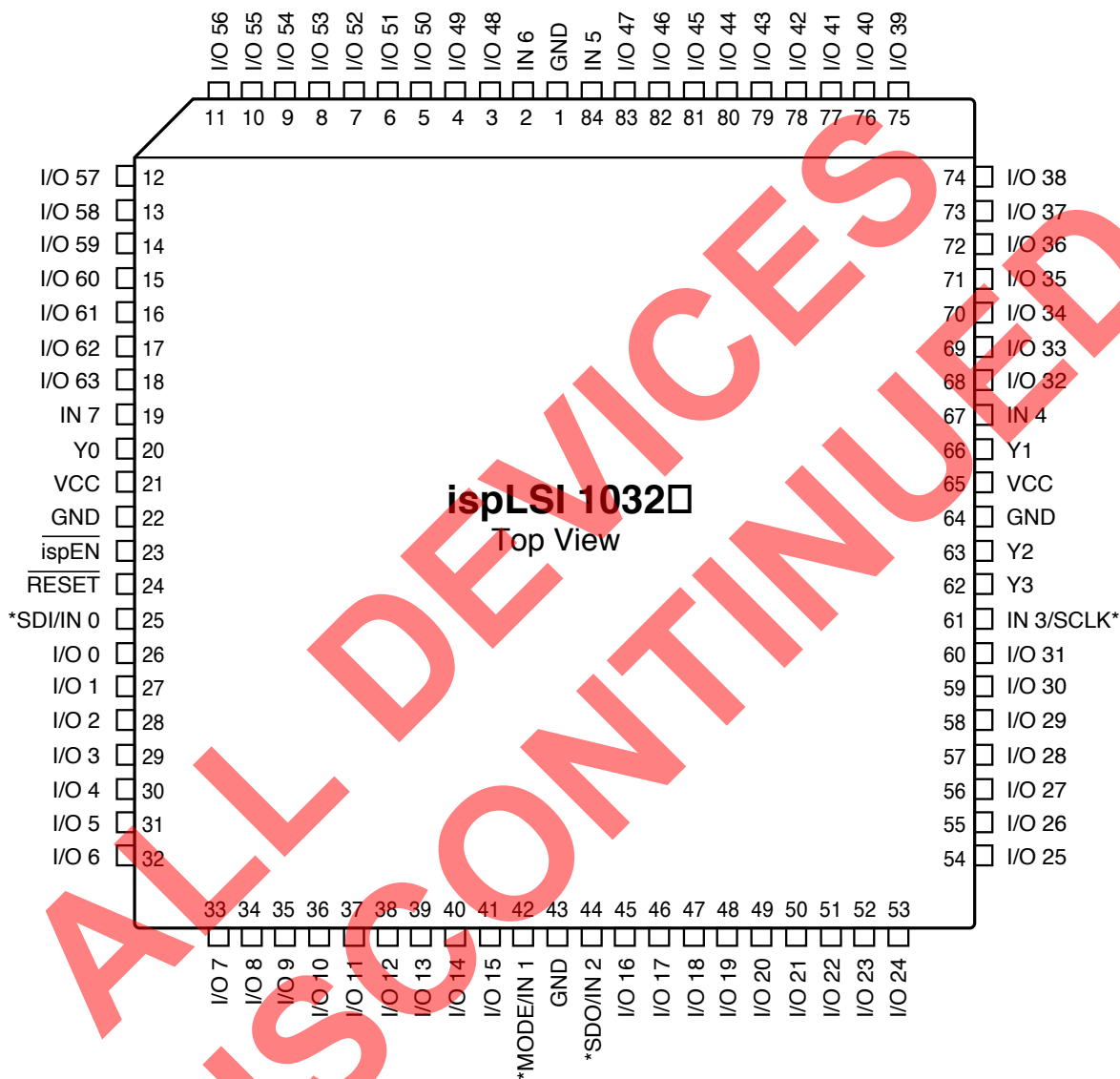
Name	CPGA Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	F1, H1, H2, J1, K1, J2, L1, K2, K3, L2, L3, K4, L4, J5, K5, L5, L7, K7, L6, L8, K8, L9, L10, K9, L11, K10, J10, K11, J11, H10, H11, F10, E9, D11, D10, C11, B11, C10, A11, B10, B9, A10, A9, B8, A8, B6, B7, A7, A5, B5, C5, A4, B4, A3, A2, B3, A1, B2, C2, B1, C1, D2, D1, E3	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 - IN 7	E10, C7, A6, E2	Dedicated input pins to the device.
$\overline{\text{ispEN}}$	G3	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0 ¹	G2	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE/IN 1 ¹	K6	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO/IN 2 ¹	J7	Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK/IN 3 ¹	G10	Input – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
$\overline{\text{RESET}}$	G1	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	E1	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	E11	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	G9	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	G11	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
NC ²	G3	No Connect
GND VCC	C6, F3, F9, J6 F2, F11	Ground (GND) V _{CC}

1. Pins have dual function capability.

2. NC pins are not to be connected to any active signals, Vcc or GND.

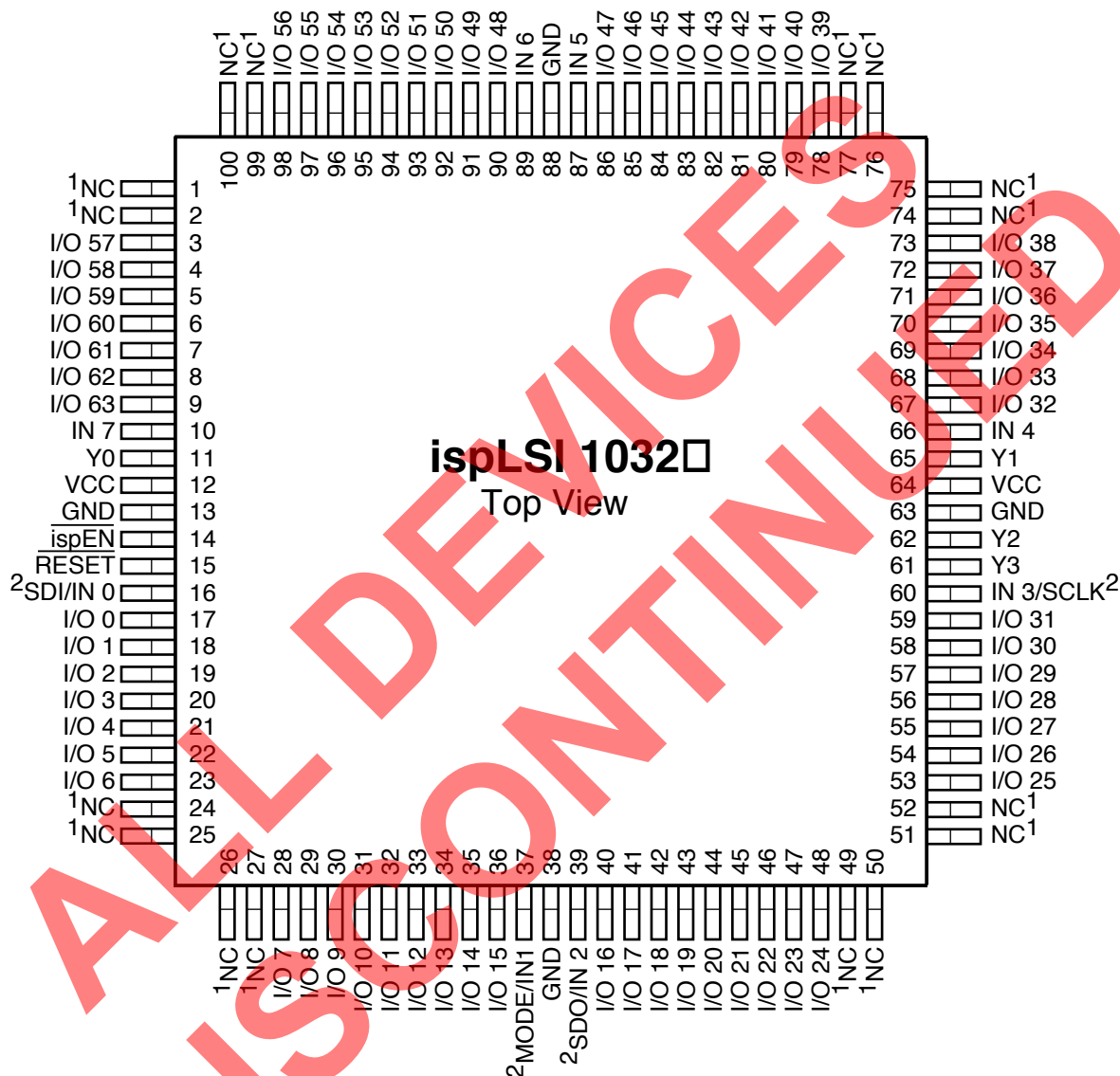
Pin Configuration

ispLSI 1032 84-Pin PLCC Pinout Diagram



Pin Configuration

ispLSI 1032 100-pin TQFP Pinout Diagram

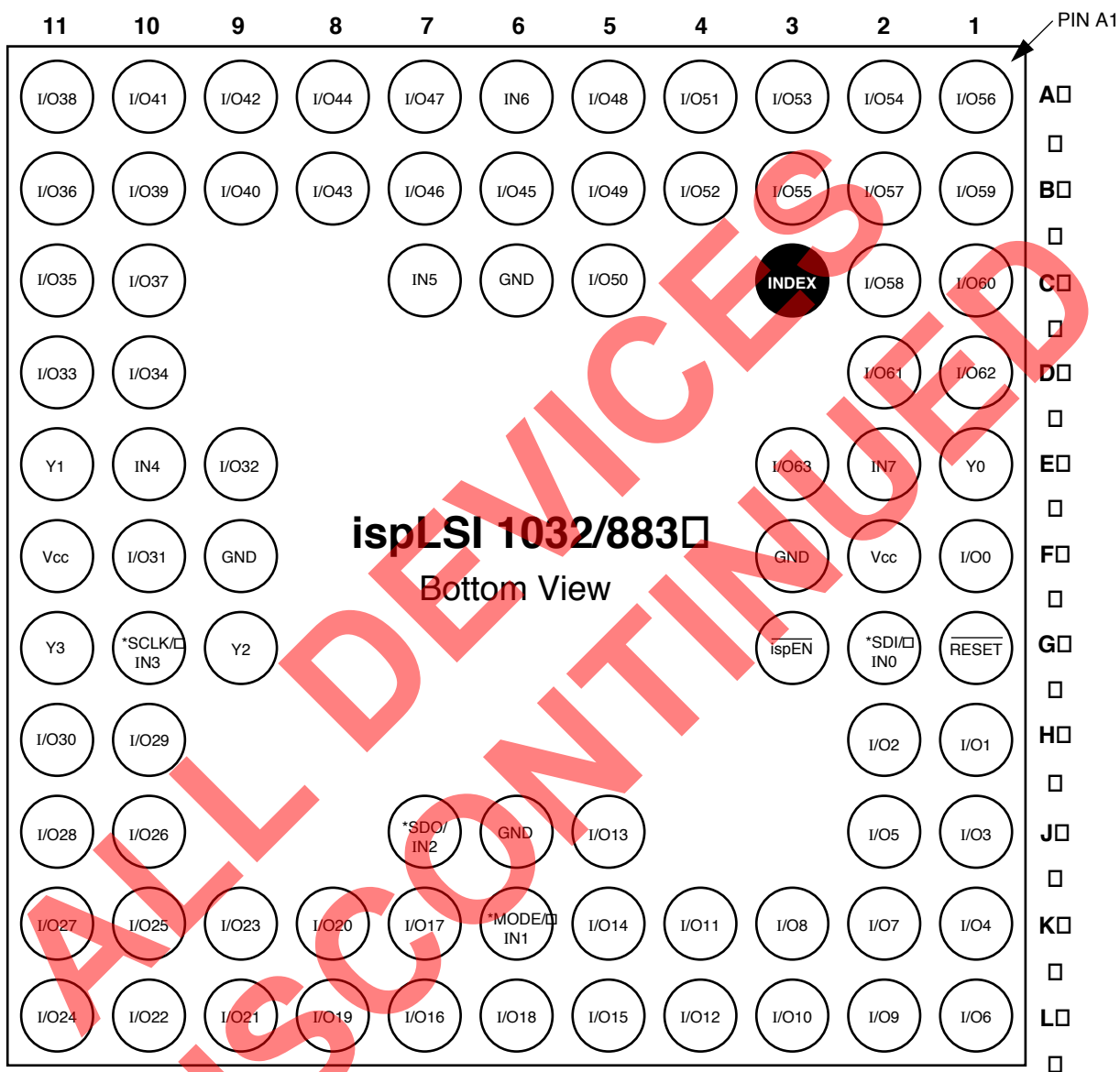


1. NC pins are not to be connected to any active signal, Vcc or GND.
2. Pins have dual function capability.

0766A-32-isp

Pin Configuration

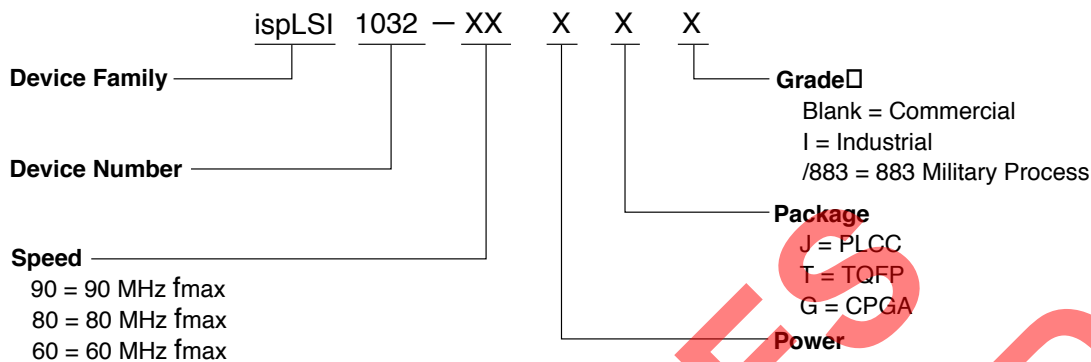
ispLSI 1032/883 84-Pin CPGA Pinout Diagram



*Pins have dual function capability.

0488A-32-isp/883

Part Number Description



0212-80B-isp1032

Ordering Information

COMMERCIAL

Family	f _{max} (MHz)	t _{pd} (ns)	Ordering Number	Package
ispLSI	90	12	ispLSI 1032-90LJ	84-Pin PLCC
	90	12	ispLSI 1032-90LT	100-Pin TQFP
	80	15	ispLSI 1032-80LJ	84-Pin PLCC
	80	15	ispLSI 1032-80LT	100-Pin TQFP
	60	20	ispLSI 1032-60LJ	84-Pin PLCC
	60	20	ispLSI 1032-60LT	100-Pin TQFP

INDUSTRIAL

Family	f _{max} (MHz)	t _{pd} (ns)	Ordering Number	Package
ispLSI	60	20	ispLSI 1032-60LJI	84-Pin PLCC
	60	20	ispLSI 1032-60LTI	100-Pin TQFP

MILITARY/883

Family	f _{max} (MHz)	t _{pd} (ns)	Ordering Number	SMD Number	Package
ispLSI	60	20	ispLSI 1032-60LG/883	5962-9308501MXC	84-Pin CPGA

Note: Lattice Semiconductor recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number is recommended.

Table 2- 0041A-32-isp