# 5-V Low Drop Fixed Voltage Regulator
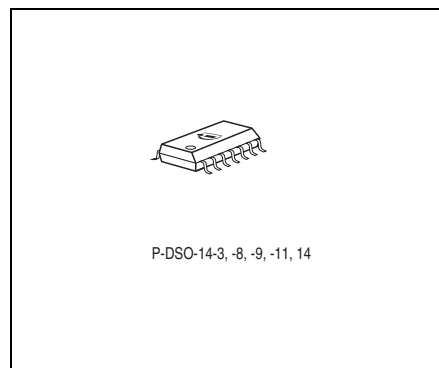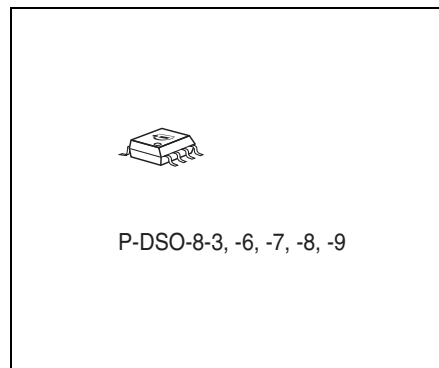
## TLE 4299

## Features

- Output voltage 5 V $\pm$ 2%
- 150 mA Output current
- Extreme low current consumption typical 65 $\mu$A in ON state
- Inhibit function: Below 1 $\mu$A current consumption in off mode
- Early warning
- Reset output low down to $V_Q = 1$ V
- Adjustable reset threshold
- Overtemperature protection
- Reverse polarity proof
- Wide temperature range

P-DSO-8-3, -6, -7, -8, -9

P-DSO-14-3, -8, -9, -11, 14

## Functional Description

The TLE 4299 is a monolithic voltage regulator with fixed 5-V output, supplying loads up to 150 mA. It is especially designed for applications that may not be powered down while the motor is off. It only needs a quiescent current of typical 65 $\mu$A. In addition the TLE 4299 GM includes an inhibit function. When the inhibit signal is removed, the device is switched off and the quiescent current is less than 1 $\mu$A. To achieve proper operation of the $\mu$-controller, the device supplies a reset signal. The reset delay time is selected application-specific by an external delay capacitor. The reset threshold is adjustable. An early warning signal supervises the voltage at pin SI. The TLE 4299 is pin-compatible to the TLE 4269 and functional similar with the additional inhibit function. The TLE 4299 is designed to supply microcontroller systems even under automotive environment conditions. Therefore it is protected against overload, short circuit and overtemperature.

| Type | Ordering Code | Package |
|---|---|---|
| TLE 4299 G | Q67006-A9417 | P-DSO-8-3 |
| TLE 4299 GM | Q67006-A9441 | P-DSO-14-8 |

## Circuit Description

The TLE 4299 is a PNP based very low drop linear voltage regular. It regulates the output voltage to $V_Q$ = 5 V for an input voltage range of 5.5 V $\leq V_I \leq$ 45 V. The control circuit protects the device against potential caused by damages overcurrent and overtemperature.

The internal control circuit achieves a 5 V output voltage with a tolerance of $\pm$2%.

The device includes a power on reset and an under voltage reset function with adjustable reset delay time and adjustable reset switching threshold as well as a sense control/early warning function. The device includes an inhibit function to disable it when the ECU is not used for example while the motor is off.

The reset logic compares the output voltage $V_Q$ to an internal threshold. If the output voltage drops below this level, the external reset delay capacitor $C_D$ is discharged. When $V_D$ is lower than $V_{LD}$, the reset output RO is switched Low. If the output voltage drop is very short, the $V_{LD}$ level is not reached and no reset-signal is asserted. This feature avoids resets at short negative spikes at the output voltage e.g. caused by load changes.

As soon as the output voltage is more positive than the reset threshold, the delay capacitor is charged with constant current. When the voltage reaches $V_{UD}$ the reset output RO is set High again.

The reset threshold is either the internal defined $V_{RT}$ voltage (typical 4.6 V) or can be lowered by a voltage level at the RADJ input down to 3.5 V. The reset delay time and the reset reaction time are defined by the external capacitor $C_D$. The reset function is active down to $V_I$ = 1 V.

In addition to the normal reset function, the device gives an early warning. When the SI voltage drops below $V_{SI,low}$, the devices asserts the SI output Low to indicate the logic and the μ-processor that this voltage has dropped. The sense function uses a hysteresis: When the SI-voltage reaches the $V_{SI,high}$ level, SO is set high again. This feature can be used as early warning function to notice the μ-controller about a battery voltage drop and a possible reset in a short time. Of cause also any other voltage can be observed by this feature.

The user defines the threshold by the resistor-values $R_{SI1}$ and $R_{SI2}$.

For the exact timing and calculation of the reset and sense timing and thresholds, please refer to the application section.
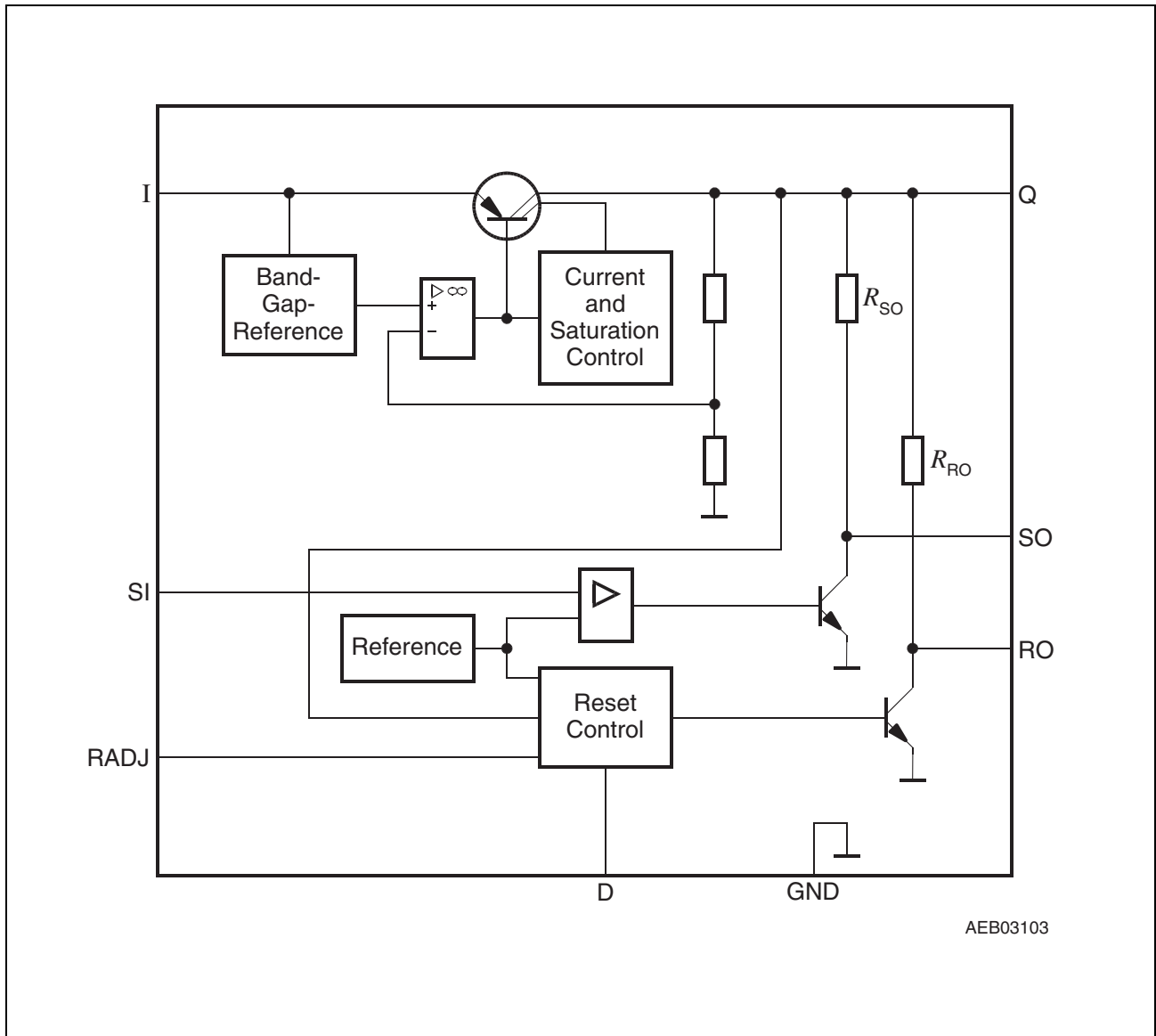
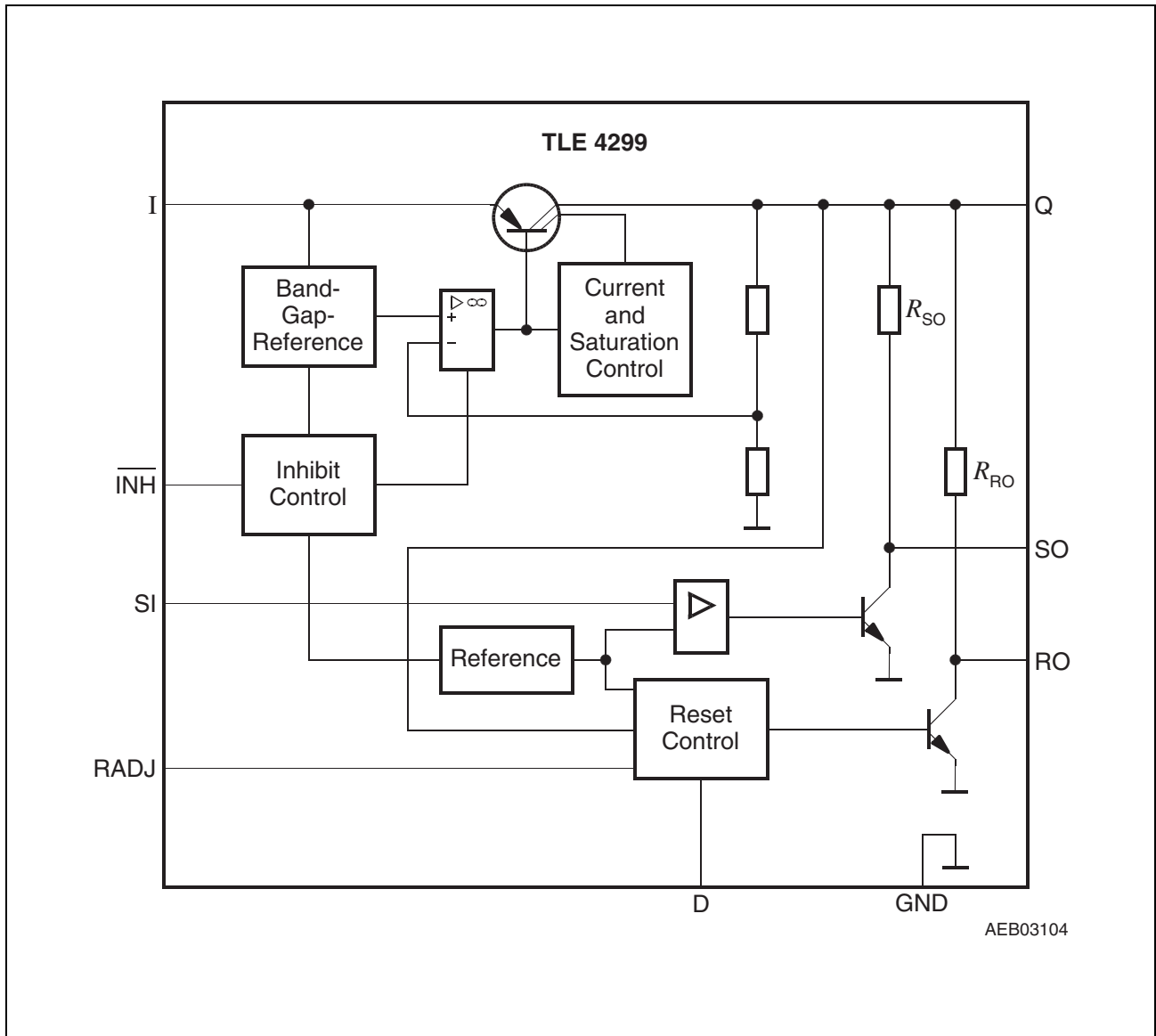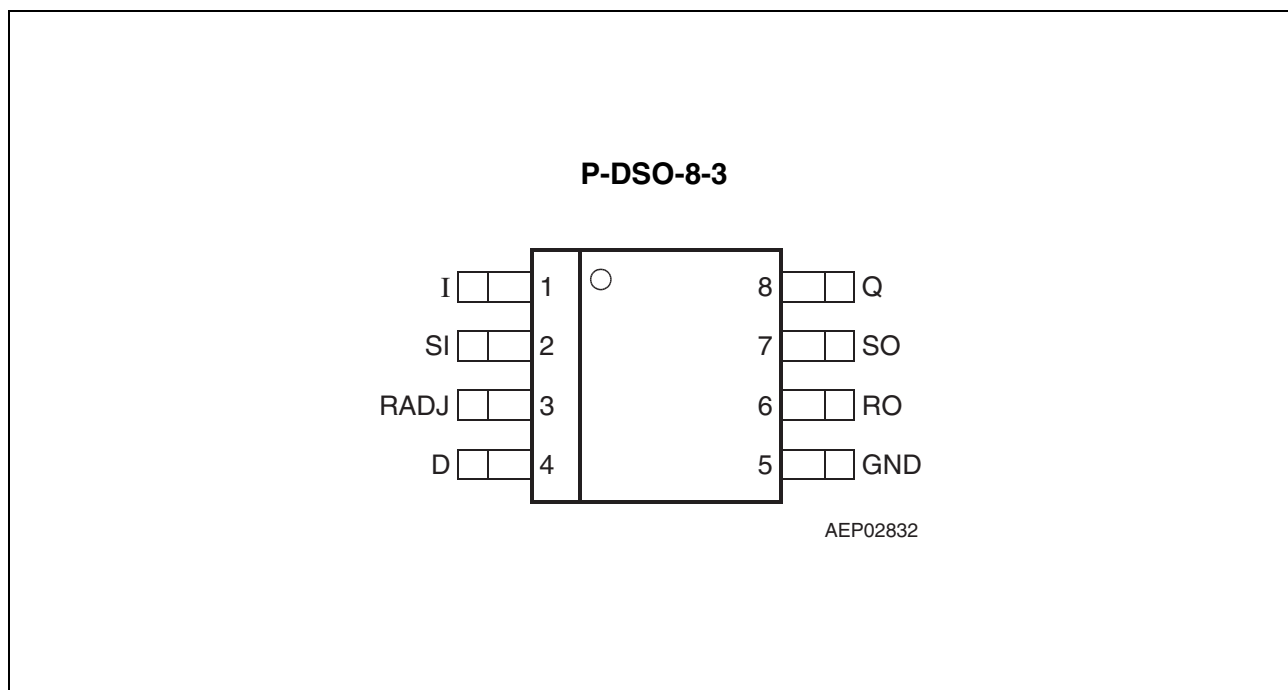**Figure 1     Block Diagram TLE 4299 G**

**Figure 2      Block Diagram TLE 4299 GM**

**P-DSO-8-3**



AEP02832

**Figure 3        Pin Configuration** (top view)

**Table 1        Pin Definitions and Functions (TLE 4299 G)**

| Pin No. | Symbol | Function |
|---|---|---|
| 1 | I | **Input;** block directly to GND on the IC with a ceramic capacitor. |
| 2 | SI | **Sense Input;** if not needed connect to Q. |
| 3 | RADJ | **Reset Threshold;** if not needed connect to GND. |
| 4 | D | **Reset Delay;** to select delay time, connect to GND via external capacitor. |
| 5 | GND | **Ground** |
| 6 | RO | **Reset Output;** the open-collector output is internally linked to Q via a 20 k$\Omega$ pull-up resistor. Keep open, if the pin is not needed. |
| 7 | SO | **Sense Output;** the open-collector output is internally linked to the output via a 20 k$\Omega$ pull-up resistor. Keep open, if the pin is not needed. |
| 8 | Q | **5-V Output;** connect to GND with a 22 $\mu$F capacitor, ESR < 5 $\Omega$. |

**P-DSO-14-8**



**Figure 4**    **Pin Configuration** (top view)

**Table 2**    **Pin Definitions and Functions (TLE 4299 GM)**

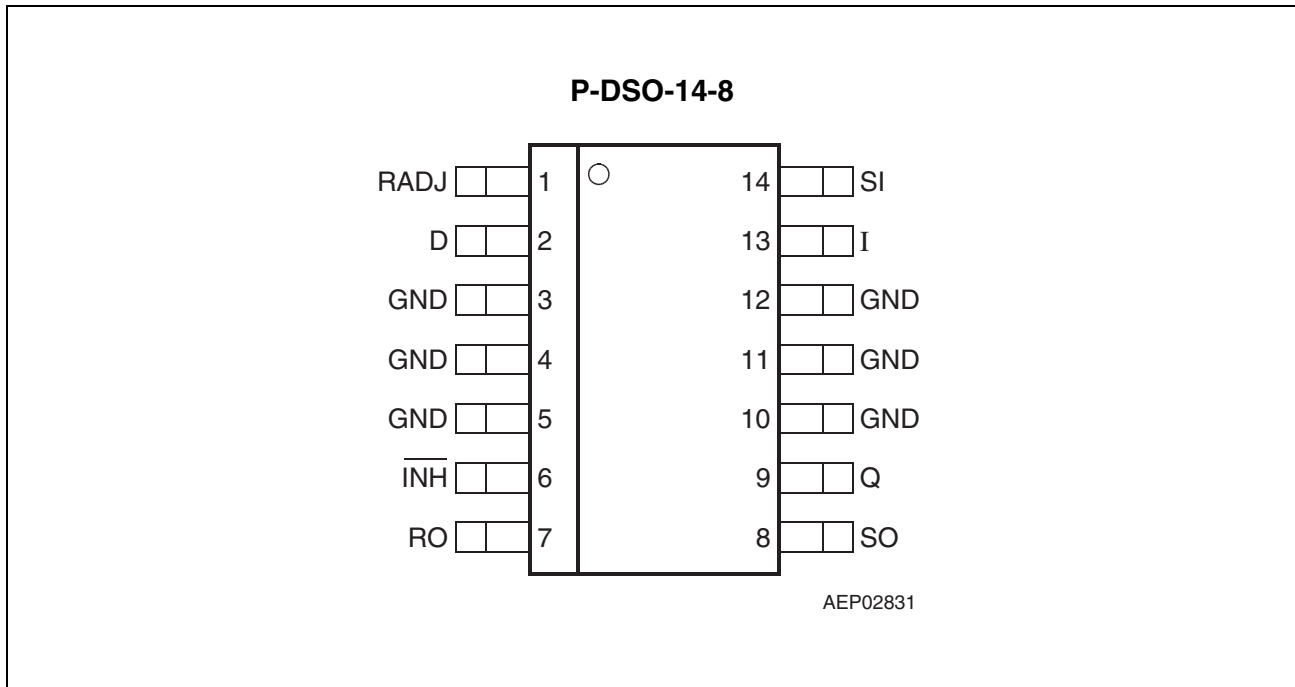| Pin No. | Symbol | Function |
|---------|--------|----------|
| 1 | RADJ | **Reset Threshold;** if not needed connect to GND. |
| 2 | D | **Reset Delay;** connect to GND via external delay capacitor for setting delay time. |
| 3, 4, 5 | GND | **Ground** |
| 6 | $\overline{\text{INH}}$ | **Inhibit;** If not needed connect to input pin I; a high signal switches the regulator ON. |
| 7 | RO | **Reset Output;** open-collector output, internally connected to Q via a pull-up resistor of 20 kΩ. Keep open, if the pin is not needed. |
| 8 | SO | **Sense Output;** open-collector output, internally connected to Q via a 20 kΩ pull-up resistor. Keep open, if the pin is not needed. |
| 9 | Q | **5-V Output;** connect to GND with a 22 µF capacitor, ESR < 5 Ω. |
| 10, 11, 12 | GND | **Ground** |
| 13 | I | **Input;** block to GND directly at the IC by a ceramic capacitor. |
| 14 | SI | **Sense Input;** if not needed connect to Q. |

**Table 3      Absolute Maximum Ratings**

$T_j$ = -40 to 150 °C

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| **Input I** | | | | | |
| Input voltage | $V_I$ | -40 | 45 | V | – |
| **Inhibit Input $\overline{\text{INH}}$** | | | | | |
| Input voltage | $V_{\overline{\text{INH}}}$ | -40 | 45 | V | – |
| **Sense Input SI** | | | | | |
| Input voltage | $V_{SI}$ | -0.3 | 45 | V | – |
| Input current | $I_{SI}$ | 1 | 1 | mA | – |
| **Reset Threshold RADJ** | | | | | |
| Voltage | $V_{RE}$ | -0.3 | 7 | V | – |
| Current | $I_{RE}$ | -10 | 10 | mA | – |
| **Reset Delay D** | | | | | |
| Voltage | $V_D$ | -0.3 | 7 | V | – |
| **Reset Output RO** | | | | | |
| Voltage | $V_R$ | -0.3 | 7 | V | – |
| **Sense Output SO** | | | | | |
| Voltage | $V_{SO}$ | -0.3 | 7 | V | – |
| **5-V Output Q** | | | | | |
| Output voltage | $V_Q$ | -0.3 | 7 | V | – |
| Output current | $I_Q$ | -5 | – | mA | – |
| **Temperature** | | | | | |
| Junction temperature | $T_j$ | – | 150 | °C | – |
| Storage temperature | $T_{Stg}$ | -50 | 150 | °C | – |
| **Operating Range** | | | | | |
| Input voltage | $V_I$ | 4.5 | 45 | V | – |
| Junction temperature | $T_j$ | -40 | 150 | °C | – |

**Table 3    Absolute Maximum Ratings** (cont'd)

$T_j$ = -40 to 150 °C

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | **Min.** | **Max.** | | |
| **Thermal Data** | | | | | |
| Junction-ambient | $R_{thja}$ | – | 200 | K/W | P-DSO-8-3 |
| | | – | 70 | K/W | P-DSO-14-8 |
| Junction-pin | $R_{thjp}$ | – | 60 | K/W | P-DSO-8-3 |
| | | – | 30 | K/W | P-DSO-14-8[1] |

1) Measured to pin 4.

*Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
*In the operating range, the functions given in the circuit description are fulfilled.*

## Table 4    Characteristics

$V_I$ = 13.5 V; $T_j$ = -40 °C < $T_j$ < 150 °C

| Parameter | Symbol | Limit Values | | | Unit | Measuring Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output voltage | $V_Q$ | 4.90 | 5.00 | 5.10 | V | 1 mA $\leq I_Q \leq$ 100 mA; 6 V $\leq V_I \leq$ 16 V |
| Output voltage | $V_Q$ | 4.85 | 5.00 | 5.15 | V | $I_Q \leq$ 150 mA; 6 V $\leq V_I \leq$ 16 V |
| Current limit | $I_Q$ | 250 | 400 | 500 | mA | – |
| Current consumption; $I_q = I_I - I_Q$ | $I_q$ | – | 65 | 105 | µA | Inhibit ON; $I_Q \leq$ 1 mA, $T_j$ < 85 °C |
| Current consumption; $I_q = I_I - I_Q$ | $I_q$ | – | 65 | 100 | µA | Inhibit ON; $I_Q \leq$ 1 mA, $T_j$ = 25 °C |
| Current consumption; $I_q = I_I - I_Q$ | $I_q$ | – | 170 | 500 | µA | Inhibit ON; $I_Q$ = 10 mA |
| Current consumption; $I_q = I_I - I_Q$ | $I_q$ | – | 0.7 | 2 | mA | Inhibit ON; $I_Q$ = 50 mA |
| Current consumption; $I_q = I_I - I_Q$ | $I_q$ | – | – | 1 | µA | $V_{\overline{INH}}$ = 0 V; $T_j$ = 25 °C |
| Drop voltage | $V_{dr}$ | – | 0.22 | 0.5 | V | $I_Q$ = 100 mA[1] |
| Load regulation | $\Delta V_Q$ | – | 5 | 30 | mV | $I_Q$ = 1 mA to 100 mA |
| Line regulation | $\Delta V_Q$ | – | 10 | 25 | mV | $V_I$ = 6 V to 28 V; $I_Q$ = 1 mA |
| Power Supply Ripple Rejection | $PSRR$ | – | 66 | – | dB | $f_r$ = 100 Hz; $V_r$ = 1 Vpp; $I_Q$ = 100 mA |
| **Inhibit (TLE 4299 GM only)** | | | | | | |
| Inhibit OFF voltage range | $V_{\overline{INH}\,OFF}$ | – | – | 0.8 | V | TLE 4299 GM; $V_Q$ off |
| Inhibit ON voltage range | $V_{\overline{INH}\,ON}$ | 3.5 | – | – | V | TLE 4299 GM; $V_Q$ on |
| High input current | $I_{\overline{INH}\,ON}$ | – | 3 | 5 | µA | TLE 4299 GM; $V_{\overline{INH}}$ = 5 V |
| Low input current | $I_{\overline{INH}\,OFF}$ | – | 0.5 | 2 | µA | TLE 4299 GM; $V_{\overline{INH}}$ = 0 V |

## Table 4 Characteristics (cont'd)

$V_I = 13.5$ V; $T_j = -40\ °C < T_j < 150\ °C$

| Parameter | Symbol | Limit Values | | | Unit | Measuring Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **Reset Generator** | | | | | | |
| Switching threshold | $V_{rt}$ | 4.50 | 4.60 | 4.80 | V | – |
| Reset pull-up | $R_{RO}$ | 10 | 20 | 40 | kΩ | – |
| Reset low voltage | $V_R$ | – | 0.17 | 0.40 | V | $V_Q < 4.5$ V; internal $R_{RO}$; $I_R = 1$ mA |
| External reset pull-up | $V_{R\ ext}$ | 5.6 | – | – | kΩ | Pull-up resistor to Q |
| Delay switching threshold | $V_{DT}$ | 1.5 | 1.85 | 2.2 | V | – |
| Switching threshold | $V_{ST}$ | 0.35 | 0.50 | 0.60 | V | – |
| Reset delay low voltage | $V_D$ | – | – | 0.1 | V | $V_Q < V_{RT}$ |
| Charge current | $I_{ch}$ | 4.0 | 8.0 | 12.0 | µA | $V_D = 1$ V |
| Reset delay time | $t_d$ | 17 | 28 | 35 | ms | $C_D = 100$ nF |
| Reset reaction time | $t_{rr}$ | 0.5 | 1.2 | 3.0 | µs | $C_D = 100$ nF |
| Reset adjust switching threshold | $V_{RADJ\ TH}$ | 1.26 | 1.36 | 1.44 | V | $V_Q > 3.5$ V |
| **Input Voltage Sense** | | | | | | |
| Sense threshold high | $V_{SI\ high}$ | 1.34 | 1.45 | 1.54 | V | – |
| Sense threshold low | $V_{SI\ low}$ | 1.26 | 1.36 | 1.44 | V | – |
| Sense input switching hysteresis | $V_{SI\ HYST}$ | 50 | 90 | 130 | mV | $V_{SI\ HYST} = V_{SI\ high} - V_{SI\ low}$ |
| Sense output low voltage | $V_{SO\ low}$ | – | 0.1 | 0.4 | V | $V_{SI} < 1.20$ V; $V_i > 4.2$ V; $I_{SO} = 0$ |
| External SO pull-up resistor | $R_{SO\ ext}$ | 5.6 | – | – | kΩ | – |
| Sense pull-up | $R_{SO}$ | 10 | 20 | 40 | kΩ | – |
| Sense input current | $I_{SI}$ | -1 | 0.1 | 1 | µA | – |
| Sense high reaction time | $t_{pd\ SO\ LH}$ | – | 2.4 | 2.9 | µs | – |
| Sense low reaction time | $t_{pd\ SO\ HL}$ | – | 1.7 | 2.1 | µs | – |

1) Drop voltage = $V_I$ - $V_Q$ (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input.)

Note: *The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25\,°C$ and the given supply voltage.*



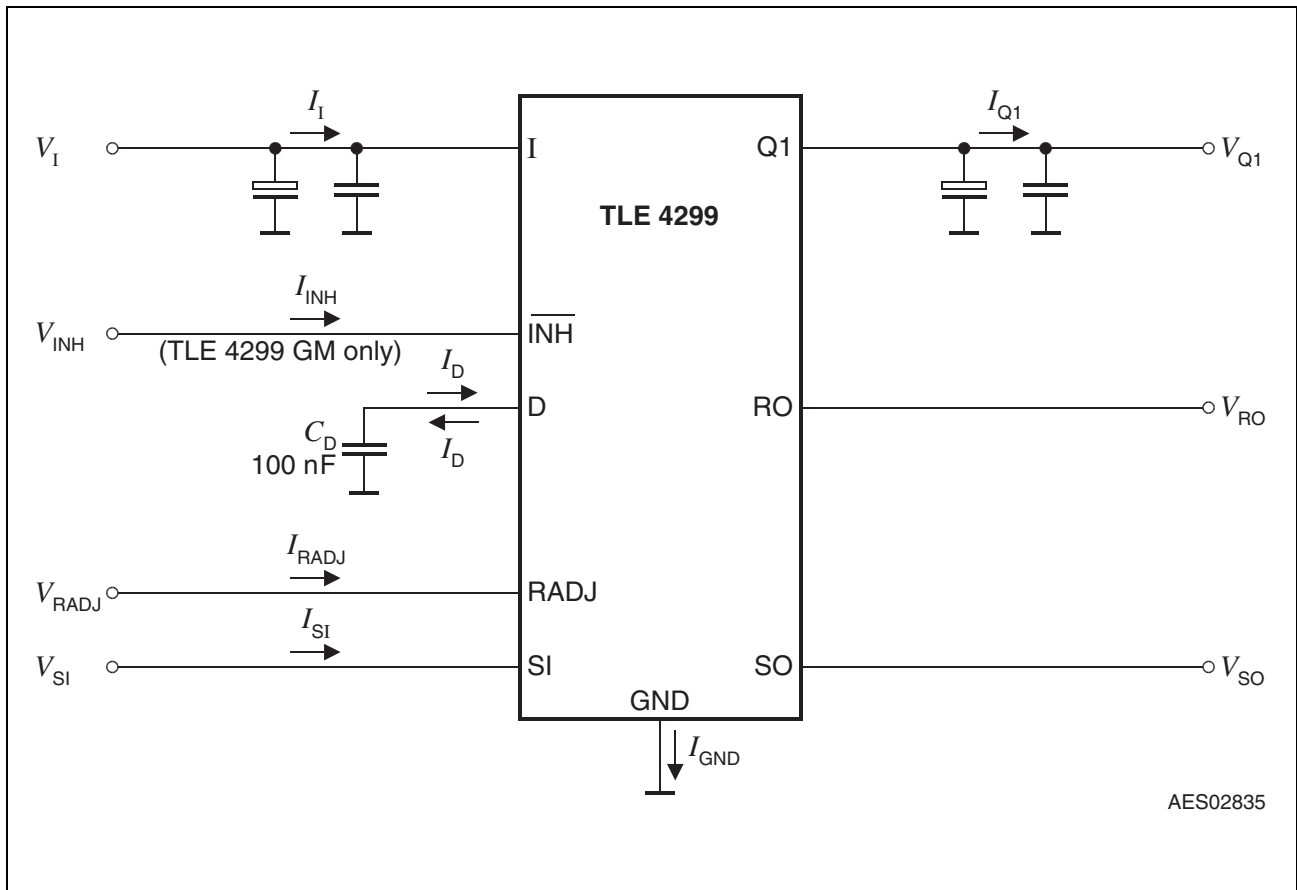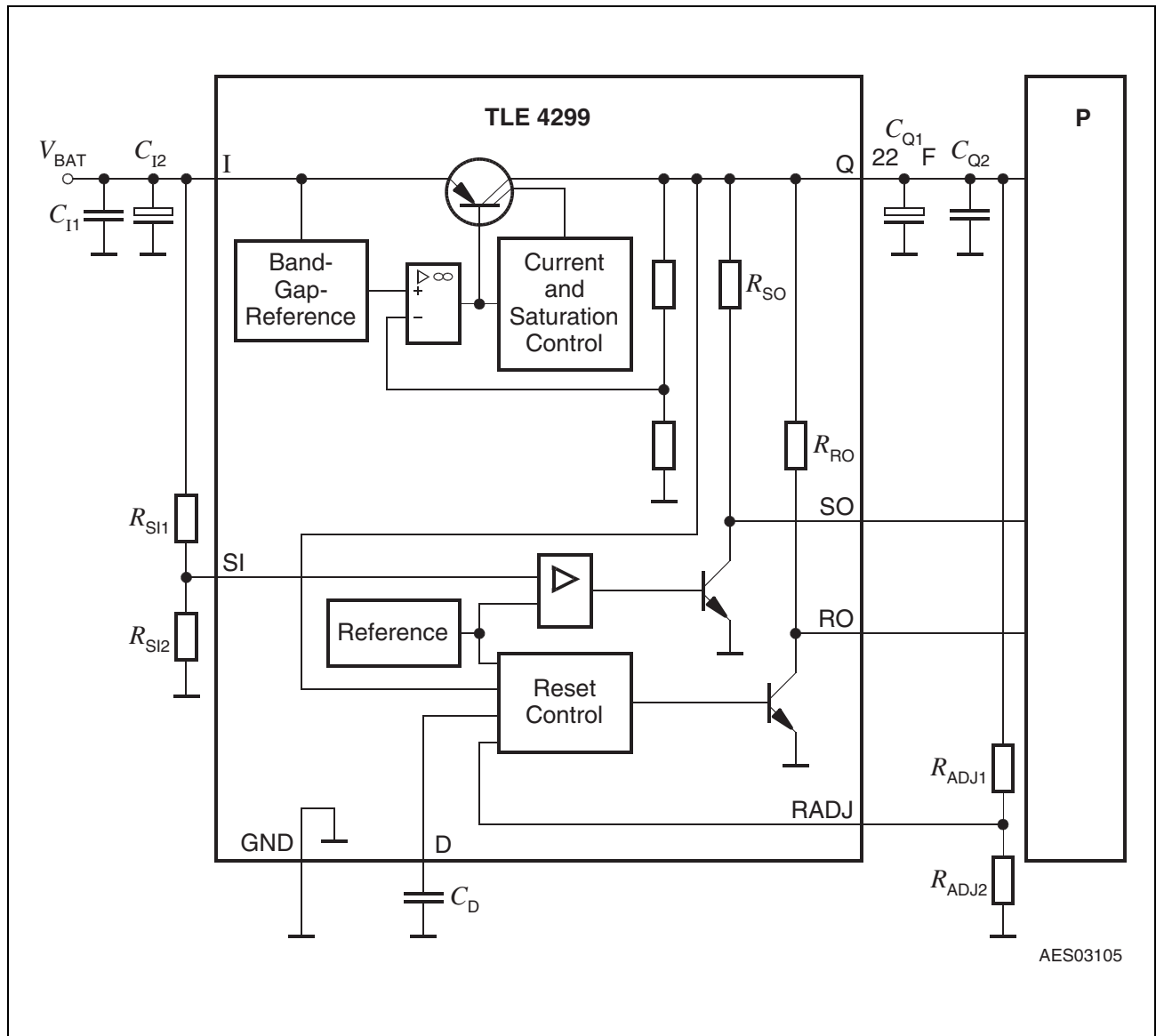**Figure 5      Measurement Circuit**

## Application Information

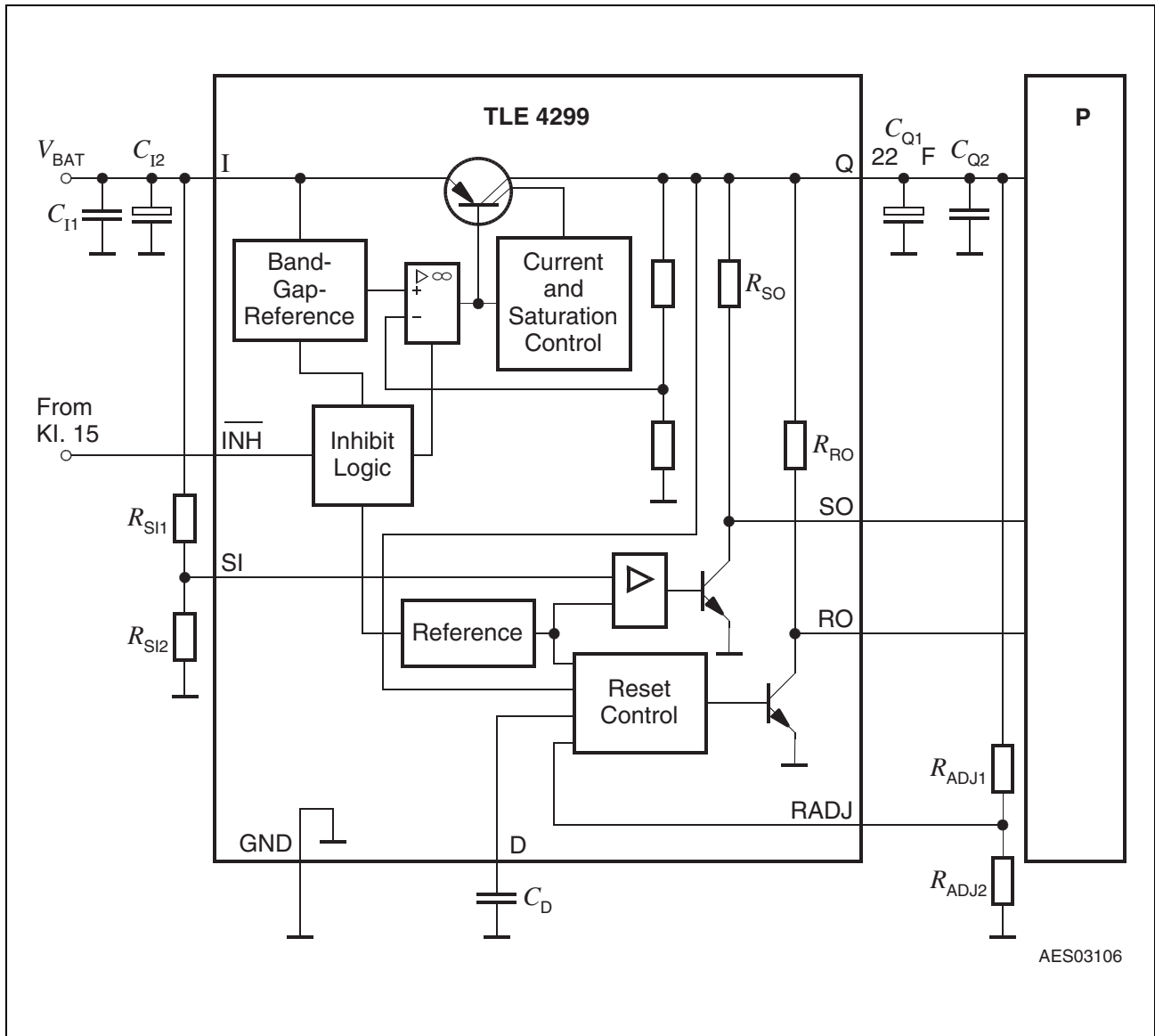

**Figure 6    Application Diagram TLE 4299 G**

**Figure 7    Application Diagram with Inhibit Function**

The TLE 4299 supplies a regulated 5 V output voltage with an accuracy of 2% from an input voltage between 5.5 V and 45 V in the temperature range of $T_j$ = -40 to 150 °C.

The device is capable to supply 150 mA. For protection at high input voltage above 25 V, the output current is reduced (SOA protection).

An input capacitor is necessary for compensating line influences and to limit steep input edges. A resistor of approx. 1 Ω in series with $C_I$, can damp the LC of the input inductivity and the input capacitor.

The voltage regulator requires for stability an output capacitor $C_Q$ of at least 22 µF with an ESR below 5 Ω.

## Reset

The power on reset feature is necessary for a defined start of the microprocessor when switching on the application. For the reset delay time after the output voltage of the regulator is above the reset threshold, the reset signal is set High again. The reset delay time is defined by the reset delay capacitor $C_D$ at pin D.

The under-voltage reset circuitry supervises the output voltage. In case $V_Q$ decreases below the reset threshold the reset output is set LOW after the reset reaction time. The reset LOW signal is generated down to an output voltage $V_Q$ to 1 V. Both the reset reaction time and the reset delay time is defined by the capacitor value.

The power on reset delay time is defined by the charging time of an external delay capacitor $C_D$.

$$C_D = (t_d \times I_D) \,/\, \Delta V \tag{1}$$

Definitions:

- $C_D$ = reset delay capacitor
- $t_d$ = reset delay time
- $\Delta V = V_{UD}$, typical 1.8 V for power up reset
- $\Delta V = V_{UD} - V_{LD}$, typical 1.35 V for undervoltage reset
- $I_D$ = charge current, typical 6.5 µA

For a delay capacitor $C_D$ = 100 nF the typical power on reset delay time is 28 ms.

The reset reaction time $t_{RR}$ is the time it takes the voltage regulator to set reset output LOW after the output voltage has dropped below the reset threshold. It is typically 1 µs for delay capacitor of 100 nF. For other values for $C_D$ the reaction time can be estimated using the following equation:

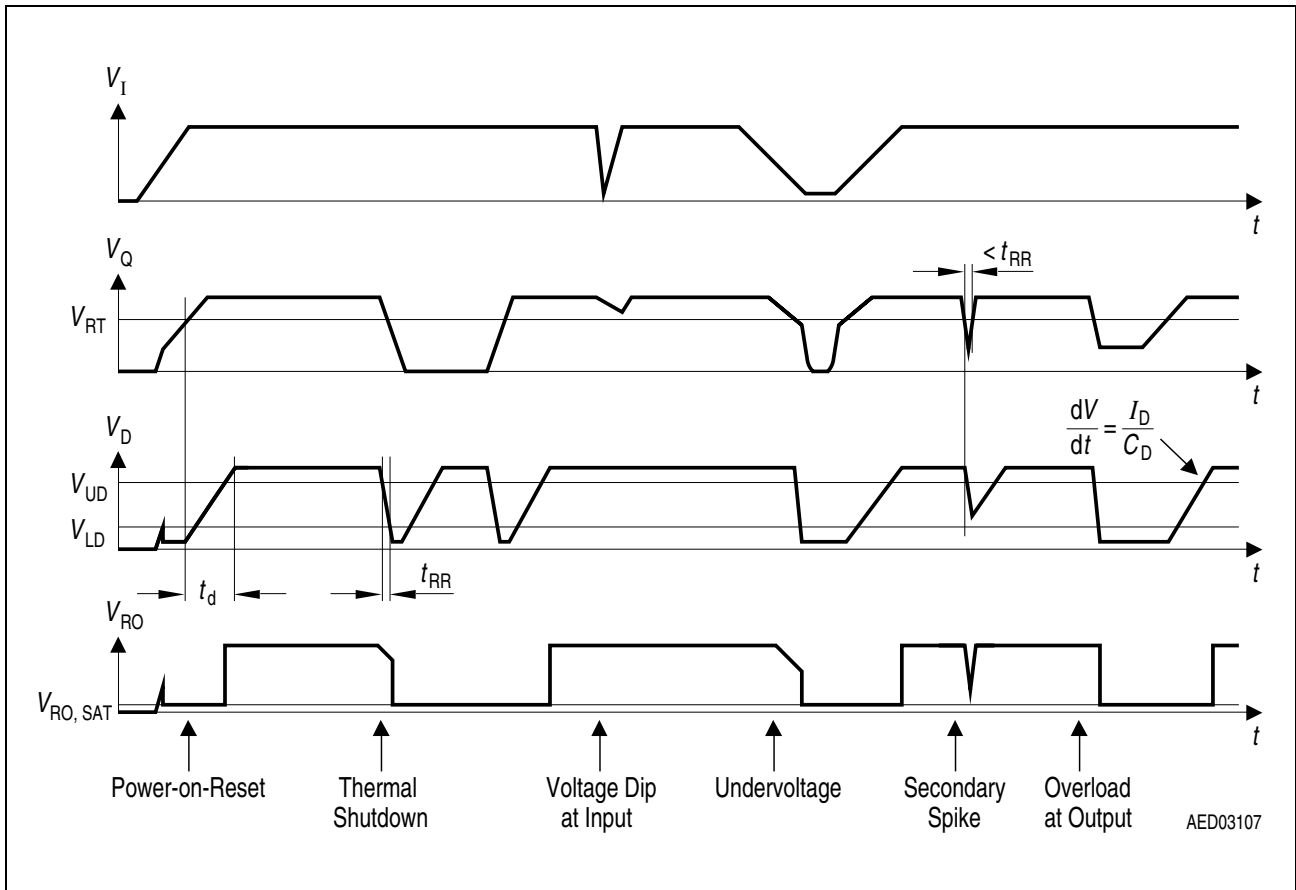$$t_{RR} = 10 \text{ ns} \,/\, \text{nF} \times C_D \tag{2}$$

**Figure 8    Reset Timing Diagram**

The reset output is an open collector output with a pull-up resistor of typical 20 kΩ to Q. An external pull-up can be added with a resistor value of at least 5.6 kΩ.

In addition the reset switching threshold can be adjusted by an external voltage divider. The feature is useful for microprocessors which guarantee safe operation down to voltages below the internally set reset threshold of 4.65 V typical.

If the internal used reset threshold of typical 4.65 V is used, the pin RADJ has to be connected to GND.

If a lower reset threshold is required by the system, a voltage divider defines the reset threshold $V_{Rth}$ between 3.5 V and 4.60 V:

$$V_{Rth} = V_{RADJ\ TH} \times (R_{ADJ1} + R_{ADJ2}) / R_{ADJ2} \tag{3}$$

$V_{RADJ\ TH}$ is typical 1.36 V.

**Early Warning**

The early warning function compares a voltage defined by the user to an internal reference voltage. Therefore the supervised voltage has to be scaled down by an

external voltage divider in order to compare it to the internal sense threshold of typical 1.35 V. The sense output pin is set low, when the voltage at SI falls below this threshold.

A typical example where the circuit can be used is to supervise the input voltage $V_I$ to give the microcontroller a prewarning of low battery condition.

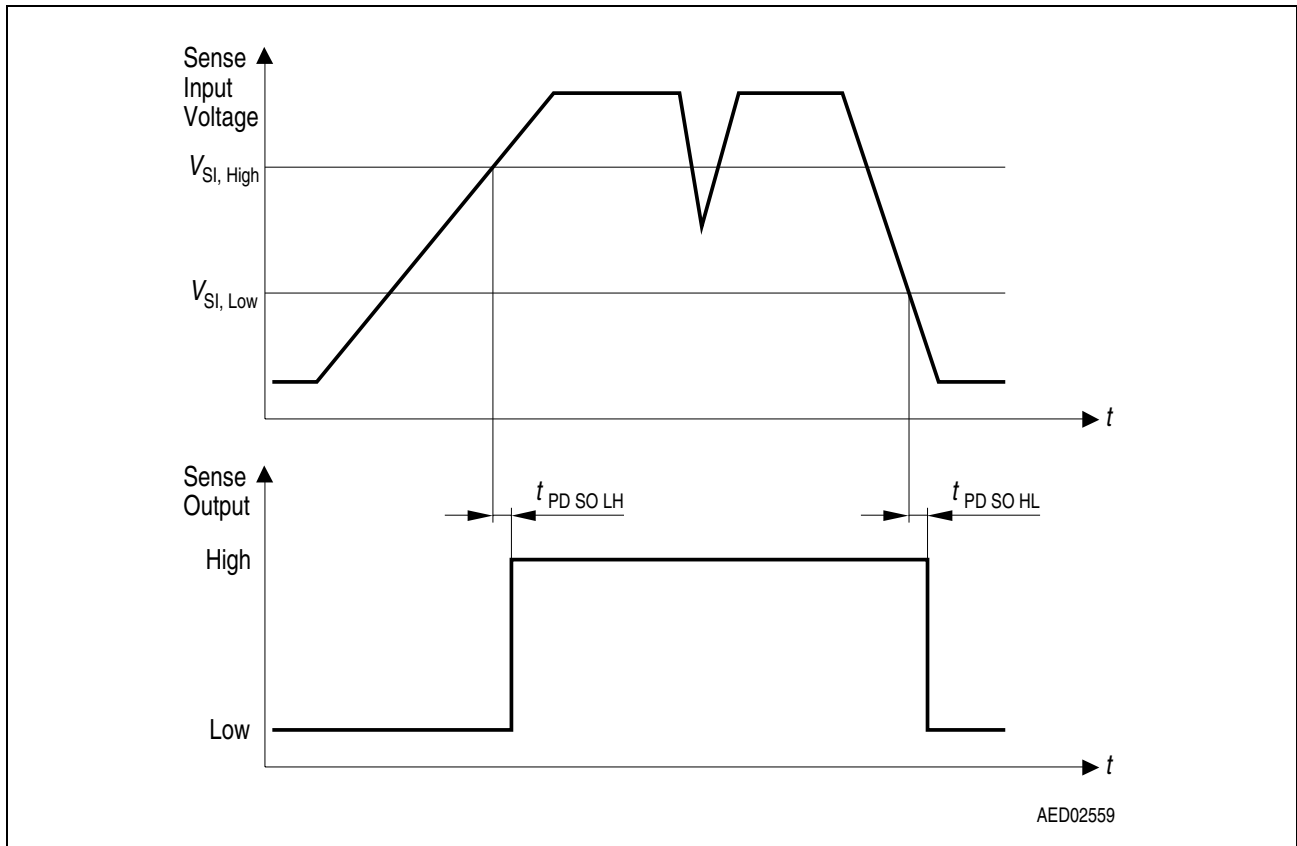Calculation to the voltage divider can be easily done since the sense input current can be neglected.



**Figure 9    Sense Timing Diagram**

$$V_{thHL} = (R_{SI1} + R_{SI2})/R_{SI2} \times V_{SI\,low} \tag{4}$$

$$V_{thLH} = (R_{SI1} + R_{SI2})/R_{SI2} \times V_{SI\,high} \tag{5}$$

The sense in comparator uses a hysteresis of typical 100 mV. This hysteresis of the supervised threshold is multiplied by the resistor dividers amplification $(R_{SI1} + R_{SI2})/R_{SI1}$.

The sense in comparator can also be used for receiving data with a threshold of typical 1.35 V and a hysteresis of 100 mV. Of course also the data signal can be scaled down with a resistive divider as shown above. With a typical delay time of 2.4 µs for positive transitions and 1.7 µs for negative transitions receiving data of up to 100 kBaud are possible.
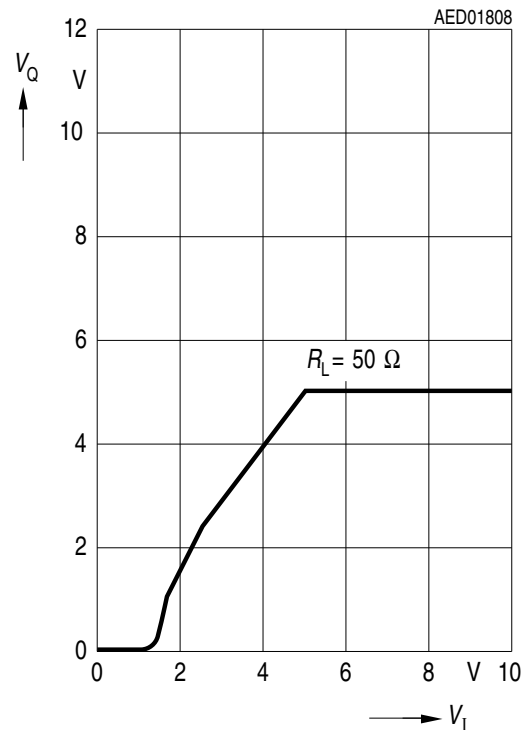
The sense output is an open collector output with a pull-up resistor of typical 20 kΩ to Q. An external pull-up can be added with a resistor value of at least 5.6 kΩ.
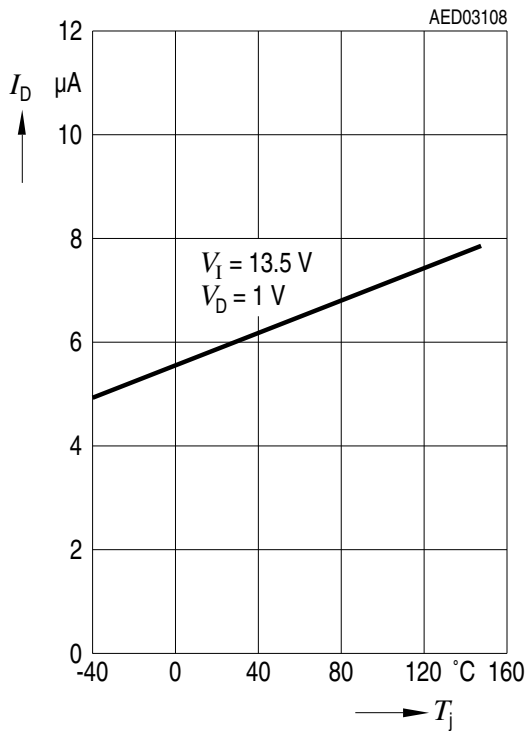
## Typical Performance Characteristics
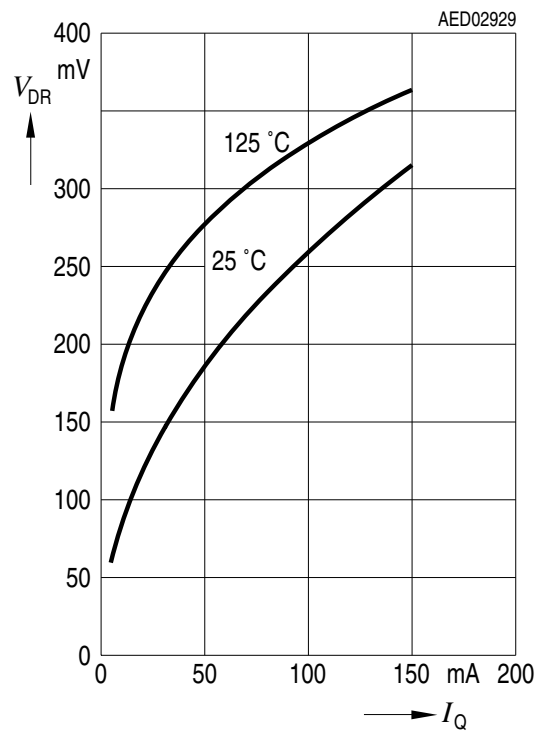
### Output Voltage $V_Q$ versus Temperature $T_j$
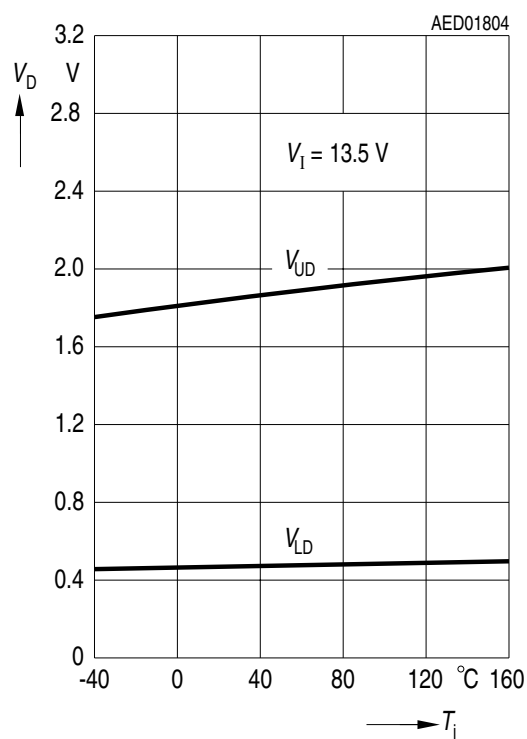


### Output Voltage $V_Q$ versus Input Voltage $V_I$
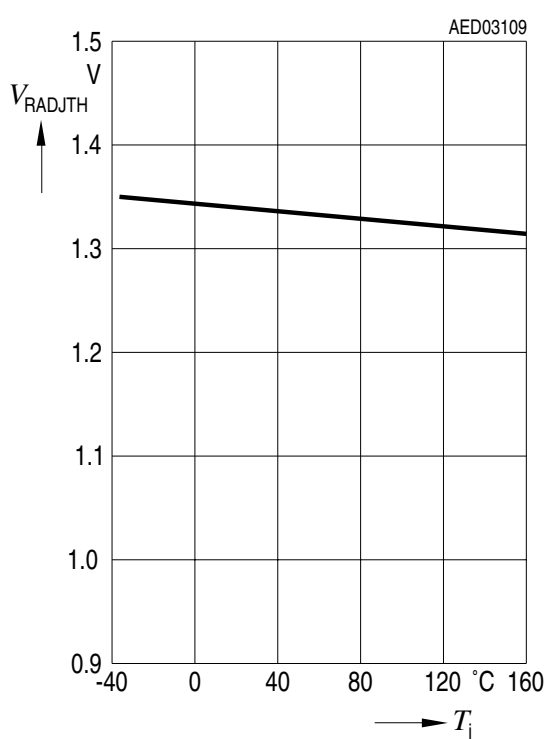
## Charge Current $I_{ch}$ versus Temperature $T_i$

AED03108



## Drop Voltage $V_{dr}$ versus Output Current $I_Q$

AED02929



## Switching Voltage $V_{dt}$ and $V_{st}$ versus Temperature $T_i$

AED01804



## Reset Adjust Switching Threshold $V_{RADJTH}$ versus Temperature $T_i$

AED03109

## Sense Threshold $V_{si}$ versus Temperature $T_i$

AED02933

Sense Output High

Sense Output Low

$V_{Si}$ V

$T_j$

## Output Current Limit $I_Q$ versus Input Voltage $V_I$

AED03110

$I_Q$ mA

$T_j = 25\,^{\circ}C$

$T_j = 125\,^{\circ}C$

$V_I$

## Current Consumption $I_q$ versus Output Current $I_Q$

AED02931

$I_q$ mA

$I_Q$

## Current Consumption $I_q$ versus Output Current $I_Q$

AED02932

$I_q$ mA

$I_Q$

## Package Outlines



$0.33 \pm 0.08$ x 45°

$4_{-0.2}^{1)}$

0.1 MIN.

(1.5)

1.75 MAX.

$0.2_{-0.01}^{+0.05}$

8° MAX.

1.27

0.1

C

$0.41_{-0.05}^{+0.1}$

$\oplus$ 0.2 Ⓜ A C x8

$0.64 \pm 0.25$

$6 \pm 0.2$

8  5

Index Marking

1  4

A

$5_{-0.2}^{1)}$

Index Marking (Chamfer)

1) Does not include plastic or metal protrusion of 0.15 max. per side
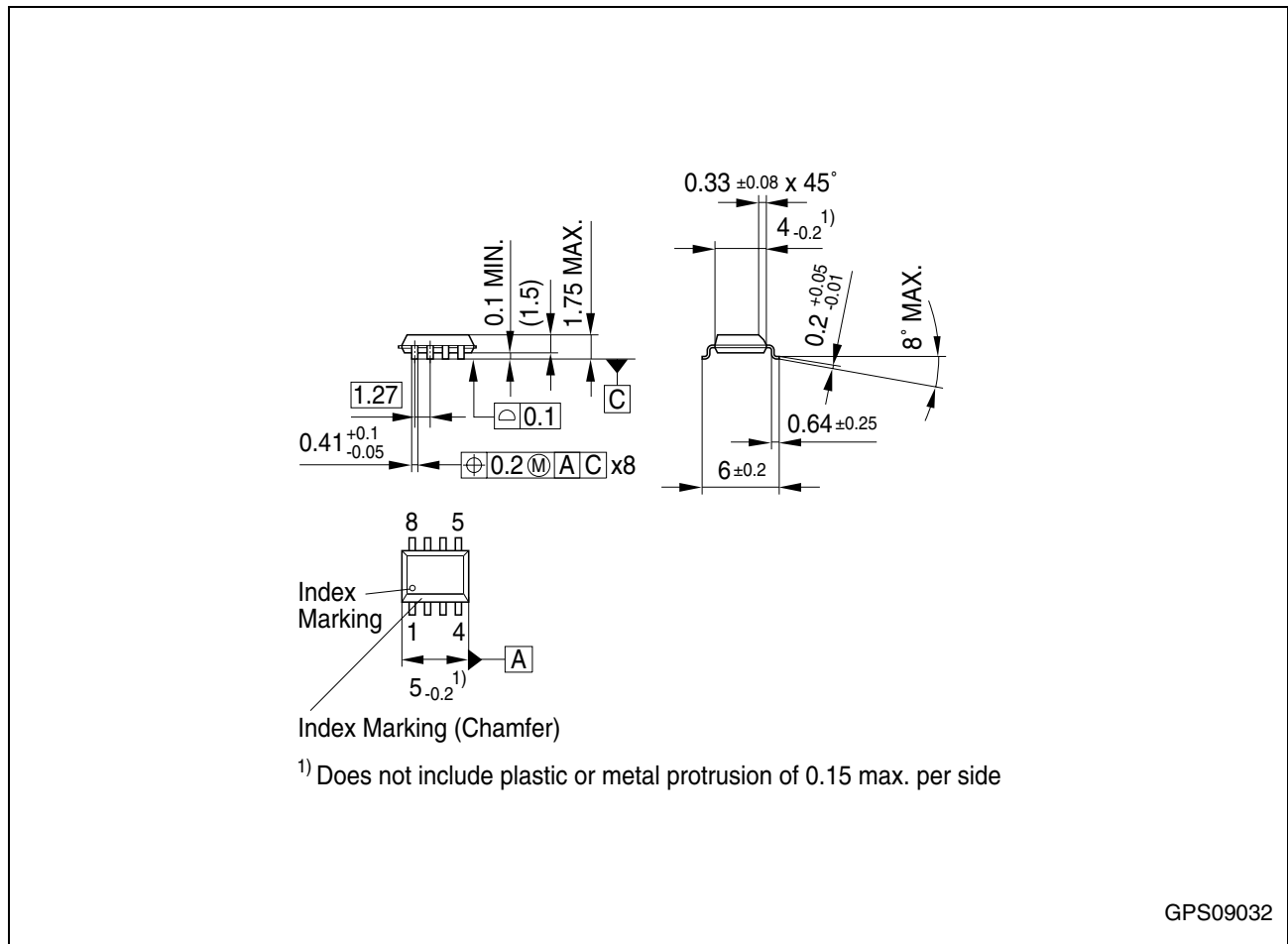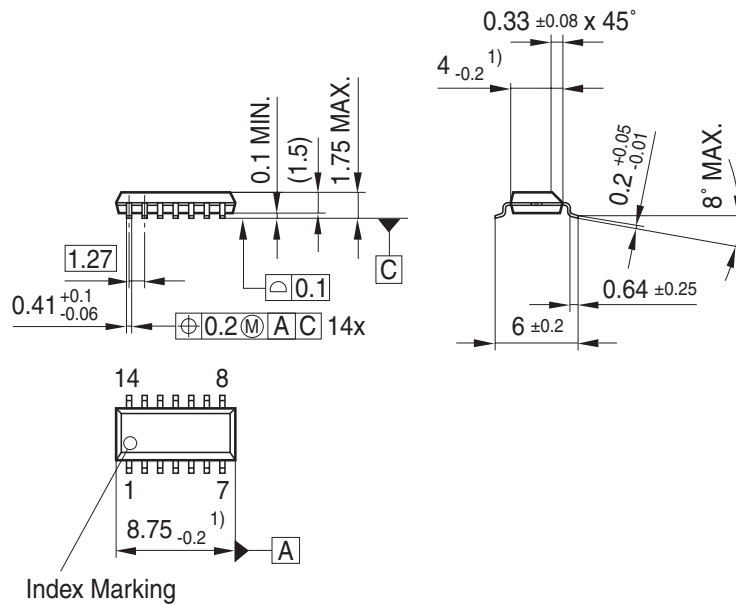
GPS09032

**Figure 10      P-DSO-8-3** (Plastic Dual Small Outline)

You can find all of our packages, sorts of packing and others in our
Infineon Internet Page "Products": **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

**Figure 11    P-DSO-14-8** (Plastic Dual Small Outline)

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Dimensions in mm

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