BU-65552, BU-65551 and BU-65550

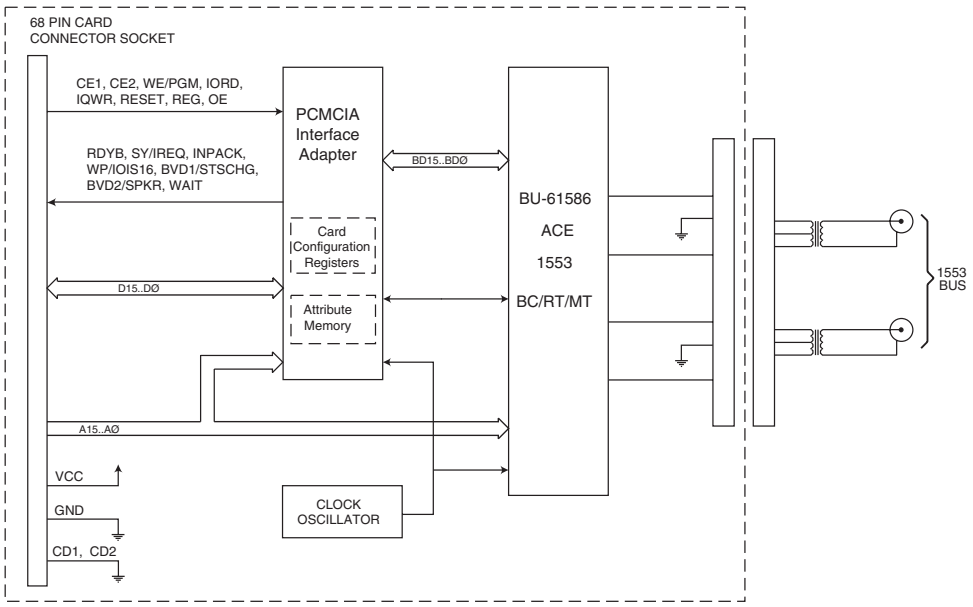
MIL-STD-1553 BC/RT/MT INTERFACE CARD

DESCRIPTION

The BU-65552, BU-65551 and BU-65550 provide full, intelligent interfacing between a dual redundant MIL-STD-1553 Data Bus and a PCMCIA socket. Software controls these cards operation as either a 1553 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT). The BU-65552, BU-65551 and BU-65550 are packaged in a Type II PCMCIA PC Card. The BU-65552 is designed around the Mini-ACE Plus, which has backward compatability to the BU-61586 and provides 64k x 16 on-board shared RAM. Using the supplied drivers and libraries, this card will require only 32k bytes of PC memory. The The BU-65552, BU-65551 and BU-65550 feature DDC's BU-61586 Advanced Communication Engine (ACE). As such, it includes dual transceiver and encoder/decoder, complete 1553 protocol, shared RAM and memory management logic for all three modes. On-board Interrupt Mask and Interrupt Status Registers support flexible operation for both interrupt and polling applications. The memory management scheme for RT mode provides an option for separation of broadcast data plus a circular buffer option for individual RT subaddresses to offload the host CPU.The PCMCIA interface includes 256 bytes of attribute memory as well as the four standard PCMCIA card configuration registers. Additional features include a wrap-around Built-In-Test, and software programmable RT address selection. Free C Runtime Library and comprehensive Menu Applications for DOS, Windows 95/98 and Windows NT. These cards support all dual redundant mode codes and message formats. Additionally, these cards allow the use of commercial off-the-shelf or ruggedized laptop and notebook computers in applications requiring a MIL-STD-1553 interface. Full compliance with both MIL-STD-1553 and PCMCIA 2.10 make the BU-65552, BU-65551 and BU-65550 an excellent choice for real-time simulation, test, and system integration applications.

FEATURES

- ***Type II PCMCIA 2.10 Compatible PC Card***
- ***MIL-STD-1553 Dual Redundant BC\RT\MT with Simultaneous RT/Monitor***
- ***Multiprotocol Support of MIL-STD-1553A and B Notice 2***
- ***Flexible RT Data Buffering***
- ***Selective Message Monitor***
- ***64K x 16 Shared RAM (BU-65552)***
- ***4K x 16 Shared RAM (BU-65551)***
- ***12K x 16 Shared RAM (BU-65550)***
- ***Runtime Libraries for Windows 3.1, Windows 95/98 and Windows NT***
- ***Menu Software for Windows 3.1, Windows 95/98 and Windows NT***



BU-65552 supplied with DDC-70093-1 Interface Cable

BU-65551 supplied with DDC-57613-1 Interface Cable

BU-65550 supplied with DDC-57612-1 Interface Cable

FIGURE 1. BU-65552, BU-65551 AND BU-65550 BLOCK DIAGRAM

TABLE 1. BU-65552, BU-65551 AND BU-65550 SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATINGS				
+5 V Supply Voltage	-0.3		7.0	V
RECEIVER				
Threshold Voltage, Transformer Coupled, Measured on Stub	0.200		0.860	V_{P-P}
Common Mode Voltage			10	V_{PEAK}
TRANSMITTER				
Differential Output Voltage				
■ Direct Coupled Across 35 ohms, Measured on Bus	6	7	9	V_{P-P}
■ Transformer Coupled, Measured on Stub	18	20	27	V_{P-P}
Output Noise, Differential (Direct Coupled)			10	mV_{P-P}, diff
Output Offset Voltage, Direct Coupled Across 35 ohms	-90		90	mV
Rise/Fall Time	100		300	nsec
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances				
■ + 5 V	4.5		5.5	V
Current Drain @ + 5.0 V				
■ Idle		80	110	mA
■ 25% Transmitter Duty Cycle		225	300	mA
■ 50% Duty Cycle		385	490	mA
■ 100% Duty Cycle		700	860	mA
POWER DISSIPATION				
Total PC Card (V_{CC} = +5.0 V)				W
■ Idle		0.4	0.55	
■ 25% Duty Cycle		0.98	1.18	W
■ 50% Duty Cycle		1.16	1.81	W
■ 100% Duty Cycle		1.47	3.07	W
1553 MESSAGE TIMING				
RT Response Time	4		7	µsec
Completion of CPU Write (BC Start-to Start of FIRST BC Message)		2.5		µsec
BC Intermessage Gap (See Note 1)		9.5		µsec
BC/RT/MT Response Timeout (See Note 2)				
■ 18.5 nominal	17.5	18.5	19.5	µsec
■ 22.5 nominal	21.5	22.5	23.5	µsec
■ 50.5 nominal	49.5	50.5	51.5	µsec
■ 128.0 nominal	127	128	129	µsec
Transmitter Watchdog Timeout		668		µsec
THERMAL				
BU-65552				
Operating Temperature	0		55	°C
Storage Temperature	-20		65	°C
BU-65551				
Operating Temperature	-25		70	°C
Storage Temperature	-55		80	°C
BU-65550				
Operating Temperature	0		55	°C
Storage Temperature	-20		65	°C
Vibration	Random vibration, 0.1 g^2/ Hz from 20 Hz to 2000 Hz			
Shock	40g, 11ms, half sine			
Operating Humidity	0 to 95% non-condensing			
Non-operating Humidity	100% condensing			

TABLE 1. BU-65552, BU-65551 AND BU-65550 SPECIFICATIONS (continued)

PARAMETER	MIN	TYP	MAX	UNITS
PHYSICAL CHARACTERISTICS				
Size		3.370 x 2.126 x 0.197 (85.6 x 54.0 x 5.0)		in (mm)
Weight		2.8 (80)		oz (gm)

Notes:
(1) Typical value for minimum intermessage gap time. Under software control, may be lengthened to (65,535 ms minus message time), in increments of 1 µs.
(2) Software programmable (4 options). Includes RT-to-RT Timeout (Mid-Parity of Transmit Command to Mid-Sync of Transmitting RT Status).

TABLE 2. HOST SYSTEM REQUIREMENTS

HARDWARE REQUIREMENTS
■ Socket Interface Compliant with PCMCIA Release 2.10 or higher
SOFTWARE REQUIREMENTS
■ Card Services Driver Compliant to PCMCIA Release 2.10 or higher

FUNCTIONAL OVERVIEW

GENERAL

The BU-65552, BU-65551 and BU-65550 (See FIGURE 1) provides a user-friendly interface between the serial MIL-STD-1553 Bus and a PCMCIA interface socket. The operating modes of these cards are controlled through the use of 24 on-board registers. 1553 message traffic is stored and retrieved using the dedicated, memory mapped, on-board 12K words of RAM. The various registers control and operate the BU-65552, BU-65551 and BU-65550. They include the five Configuration Registers, Start/Reset Register, Time Tag Register, Interrupt Mask Register, and Interrupt Status Register. The Configuration Registers define the operating mode and memory management features. The Start/Reset Register provides various reset and BC/MT start functions. The Interrupt Mask Register enables desired interrupts, with the interrupt priority level being jumper programmable by the user. The cause of interrupts may be determined by a single READ operation, by means of the Interrupt Status Register. The Time Tag Register features programmable resolution and is used to time tag messages in BC, RT, or MT modes.

The BU-65552 64K x16 of static RAM is shared by the PC host and the 1553 Bus with memory arbitration handled automatically by the BU-65552.

The BU-65551 4K x16 of static RAM is shared by the PC host and the 1553 Bus with memory arbitration handled automatically by the BU-65551.

The BU-65550 12K x16 of static RAM is shared by the PC host and the 1553 Bus with memory arbitration handled automatically by the BU-65550.

The BU-65552, BU-65551 and BU-65550 will withhold the WAIT signal (assert to logic "0") to the PCMCIA socket interface while a word is being transferred to or from the 1553 Bus. Since the memory arbitration is handled by simply stretching the handshake cycle, the wait state is transparent to the PC host processor's software. A maximum wait of 2.6 µs can occur

In addition to storing the 1553 message data, the RAM implements the Stacks and Look-Up Tables required for the different modes of operation. A global double buffering mechanism is available to prevent partially updated information from being transferred to or from the 1553 Bus. For RT mode, there is a programmable option to separate broadcast message data from non-broadcast data. This provides compliance to MIL-STD-1553. In addition, for RT mode, there is the choice of storing either a single message, a double buffer data structure, or a circular buffer data structure. The size of the circular buffer is programmable up to 8192 words, on a Tx/Rx/Bcst-subaddress basis.

The BU-65552, BU-65551 and BU-65550 support programmable command illegalization for RT mode. This allows individual Command Words to be illegalized as a function of $T/\overline{R}$ bit, subaddress, and word count/mode code. Since the illegalization scheme is RAM based, it is inherently self-testable.

A Descriptor Stack or Command Stack is maintained for BC, RT, and MT modes. This records the status of each message, the time the message was transmitted or received, and contains either the received 1553 command and Data Block Pointer (in RT or MT mode) or the actual address of the 1553 message block (in BC mode). In RT mode, a Lookup Table is provided to store the addresses of the data blocks to be used when receiving or transmitting messages for the individual subaddresses.

The PC Cards RT mode is multiprotocol, supporting MIL-STD-1553A, MIL-STD-1553B Notice 2, STANAG 3838 (including EFA bus), and the McAir A3818, A5232, and A5690 protocols.

The BU-65552, BU-65551 and BU-65550 implement three monitor modes: a word monitor, a selective message monitor, and a combined RT/selective message monitor.

PCMCIA INTERFACE

The BU-65552, BU-65551 and BU-65550 provide a Card Information Structure (CIS) within the attribute memory space of the PCMCIA interface. The CIS contains device configuration information structures called basic compatibility tuples. The format of these configuration tuples is defined within the PCMCIA interface standard. In addition to the CIS there are the four standard PCMCIA configuration registers (Configuration Option Register, Card Configuration and Status Register, Pin Replacement Register, and Socket and Copy Register).

The CIS, also referred to as the Metaformat, provides a level of device information which allows a card resource manager or an application program to identify and fully configure the card.

MEMORY MANAGEMENT

The BU-65552, BU-65551 and BU-65550 incorporate complete memory management and processor interface logic. The software interface to the host processor is implemented by means of 24 on-board registers plus up to 64K words of RAM. For all three modes, a stack area of RAM is maintained. In BC mode, the stack allows for the scheduling of multimessage frames. For all three modes, the stack provides a real-time chronology of all messages processed. In addition to the stack processing, the memory management logic performs storage, retrieval, and manipulation functions involving pointer and message data structures for all three modes.

The BU-65552, BU-65551 and BU-65550 provide a number of programm-able options for RT mode memory management. In compliance with MIL-STD-1553, received data from broadcast messages may be optionally separated from nonbroadcast received data. For each transmit, receive or broadcast subaddress, either a single-message data block or a variable-sized (128 to 8192 words) circular buffer may be allocated for data storage. In addition to helping ensure data consistency, the circular buffer feature provides a means of greatly reducing host processor overhead for bulk data transfer applications. End-of-message interrupts may be enabled either globally, following error messages, on a Tx/Rx/Bcst-subaddress basis, or when any particular Tx/Rx/Bcst-subaddress circular buffer reaches its lower boundary.

INTERRUPTS

The BU-65552, BU-65551 and BU-65550 provide many programmable options for interrupt generation and handling. The interrupt output pin ($\overline{INT}$) has three software programmable modes of operation: a pulse, a level output cleared under software control, or a level output automatically cleared following a read of the Interrupt Status Register.

Individual interrupts are enabled by the Interrupt Mask Register. The host processor may easily determine the cause of the interrupt by using the Interrupt Status Register. The Interrupt Status Register provides the current state of the interrupt conditions. The Interrupt Status Register may be updated in two ways. In the standard interrupt handling mode, a particular bit in the Interrupt Status Register will be updated only if the condition exists and the corresponding bit in the Interrupt Mask Register is enabled. In the enhanced interrupt handling mode, a particular bit in the Interrupt Status Register will be updated if the condition exists regardless of the contents of the corresponding Interrupt Mask Register bit. In any case, the respective Interrupt Mask Register bit enables an interrupt for a particular condition.

The BU-65552, BU-65551 and BU-65550 provide maskable interrupts and 15-bit Interrupt Status Register for end of message, end of BC message list, erroneous messages, Status Set (BC mode), Time Tag Register Rollover, RT Address Parity Error conditions, BC retry, data stack rollover, command stack rollover, transmitter watchdog timeout, or RAM parity error. The Interrupt Status Register allows the host processor to determine the cause of all interrupts by means of a single READ operation.

INTERNAL COMMAND ILLEGALIZATION

The BU-65552, BU-65551 and BU-65550 implemen internal command illegalization for RT mode. The illegalization architecture allows for any subset of the 4096 possible combinations of broadcast/own address, $T/\overline{R}$ bit, subaddress, and word count/mode code to be illegalized. The illegalization scheme is under software control of the host processor. As a result, it is inherently self-testable.

INTERNAL TIME TAG

The BU-65552, BU-65551 and BU-65550 include an internal read/writable Time Tag Register. This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 μs per LSB. Another option allows the Time Tag Register to be incremented under software control. This supports self-test for the Time Tag Register.

For each message processed, the value of the Time Tag register is loaded into the second location of the respective descriptor stack entry ("TIME TAG WORD") for both BC and RT modes.

Additional options are provided to clear the Time Tag Register following a Synchronize (without data) mode command or load the Time Tag Register following a Synchronize (with data) mode command. Another option enables an interrupt request and a bit in the Interrupt Status Register to be set when the Time Tag Register rolls over from FFFF to 0000 (hex). Assuming the Time Tag Register is not loaded or reset, this will occur at approximately 4-second time intervals, for 64 μs/LSB resolution, down to 131 ms intervals, for 2 μs/LSB resolution.

Another programmable option for RT mode is for the Service Request Status Word bit to be automatically cleared following the PC Cards response to a Transmit Vector Word mode command.

ADDRESSING, INTERNAL REGISTERS, MEMORY MANAGEMENT, AND INTERRUPTS

ADDRESSING THESE CARDS

All internal pointers used by these cards are assumed to be **word** addresses, however **byte** addressing is used by the PC to access memory and registers in the card. For example, to access the the Area A Stack Pointer at word offset address 0100 (hex), a byte address offset of 0200 (hex) must be used (i.e. the byte address is determined by multiplying the word address by two).

The shared RAM space starts at **byte** location 8000 if the memory allocation were contiguous. The registers are mapped into memory locations 0X0000 through 0X002F. The memory address space between 0X0030 and 0X7FFF is reserved. The 64K x 16 RAM uses page swapping, which is done in the device driver.

COMMON MEMORY ADDRESS MAP

The software interface of the BU-65552, BU-65551 and BU-65550 to the host processor consists of 17 internal operational registers for normal operation, an additional 8 test registers, plus shared memory (64K x 16 for BU-65552, 4K x 16 for BU-65551 and 12K x 16 for BU-65550). Both the registers and the shared memory reside in the PCMCIA common memory space. See TABLE 3. The BITMAPS of the 17 internal registers are shown in TABLES 4 through 21.

Definition of the address mapping and accessibility for the BU-65552, BU-65551 and BU-65550 17 nontest registers, and the test registers, is as follows:

TABLE 3. COMMON MEMORY ADDRESS MAPPING

HEX ADDRESS	DESCRIPTION/ACCESSIBILITY
0000, 0001	Interrupt Mask Register (RD/WR)
0002, 0003	Configuration Register # 1 (RD/WR)
0004, 0005	Configuration Register # 2 (RD/WR)
0004, 0005	Configuration Register # 2 (RD/WR)
0006, 0007	Start/Reset Register (WR)
0006, 0007	BC/RT Command Stack Pointer Register (RD)
0008, 0009	BC Control Word/RT Subaddress Control Word Register (RD/WR)
000A, 000B	Time Tag Register (RD/WR)
000C, 000D	Interrupt Status Register (RD)
000E, 000F	Configuration Register #3
0010, 0011	Configuration Register #4
0012, 0013	Configuration Register #5
0014, 0015	Data Stack Address Register (RD/WR)
0016, 0017	BC Frame Time Remaining Register (RD)*
0018, 0019	BC Time Remaining to Next Message Register (RD)*
001A,001B	BC Frame Time*/RT Last Command/MT Trigger Word* Register (RD/WR)
001C, 001D	RT Status Word Register (RD)
001E, 001F	RT BIT Word Register (RD)
0020, 0021 • • • 002E,002F	Test Mode Register 0 • • • Test Mode Register 7
0030, 0031 • • • 7FFE, 7FFF	reserved • • • reserved
8000, 8001 • • • DFFE, DFFF	12K x 16 Shared RAM (RD/WR) See NOTE below. • • • 12K x 16 Shared RAM (RD/WR)
E000, E001 • • • FFFE, FFFF	reserved • • • reserved

NOTES: 1. Normally RAM Addresses will be defined as an offset from the base address
2. BU-65551 shared RAM is 4K x 16

Interrupt Mask Register: Used to enable and disable interrupt requests for various conditions.

Configuration Registers #1 and #2: Used to select the PC Cards mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-on-Error, RT Memory Management mode selection, and control of the Time Tag operation.

Start/Reset Register: Used for "command" type functions, such as software reset, BC/MT Start, Interrupt Reset, Time Tag Reset, and Time Tag Register Test. The Start/Reset Register includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

BC/RT Command Stack Pointer Register: Allows the host CPU to determine the pointer location for the current or most recent message when the PC Card is in BC or RT mode.

BC Control Word/RT Subaddress Control Word Register: In BC mode, allows host access to the current or most recent BC Control Word. The BC Control Word contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. In RT mode, this register allows host access to the current or most recent Subaddress Control Word. The Subaddress Control Word is used to select the memory management scheme and enable interrupts for the current message. The read/write accessibility can be used as an aid for testing the ACE.

Time Tag Register: Maintains the value of a real-time clock. The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 μs/LSB. The TAG_CLK input signal also may cause an external oscillator to clock the Time Tag Register. Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of RAM.

Interrupt Status Register: Mirrors the Interrupt Mask Register and contains a Master Interrupt bit. It allows the host processor to determine the cause of an interrupt request by means of a single READ operation.

Configuration Registers #3, #4, and #5: Used to enable many of the BU-65552, BU-65551 and BU-65550 advanced features. These include all the enhanced mode features; that is, all the functionality beyond that of the previous generation product, the BUS-65529 that makes use of the Advanced Integrated Mux Hybrid with Enhanced RT Features (AIM-HY'er). For all three modes, use of the Enhanced Mode enables the various read-only bits in Configuration Register #1.

For BC mode, the enhanced mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message.

For RT mode, the enhanced mode features include the expanded RT Block Status Word, the combined RT/Selective Message Monitor mode, internal wrapping of the "$\overline{\text{RTFAIL}}$" output signal (from the J' chip)to the "$\overline{\text{RTFLAG}}$" RT Status Word bit, the double buffering scheme for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word.

For MT mode, use of the enhanced mode enables use of the Selective Message Monitor, the combined RT/Selective Monitor modes, and the monitor triggering capability.

Data Stack Address Register: Used to point to the current address location in shared RAM used for storing message words (second Command Words, Data Words, RT Status Words) in the Selective Word Monitor mode.

Frame Time Remaining Register: Provides a read only indication of the time remaining in the current BC frame. The resolution of this register is 100 μs/LSB.

Message Time Remaining Register: Provides a read only indication of the time remaining before the start of the next message in a BC frame. The resolution of this register is 1 μs/LSB.

BC Frame/RT Last Command/MT Trigger Word Register: In BC mode, it programs the BC frame time for use in the frame auto-repeat mode. The resolution of this register is 100 μs/LSB, with a range of 6.55 seconds. In RT mode, this register stores the current (or most previous) 1553 Command Word processed by the ACE RT; in the Word Monitor mode, this register specifies a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

Status Word Register and BIT Word Registers: Provide read-only indications of the BU-65552, BU-65551 and BU-65550 RT Status and BIT Words.

Test Mode Registers 0-7: These registers may be used to facilitate built-in testing of the BU-65552, BU-65551 and BU-65550 .

ACE Software

The BU-65552/BU-65551/BU-65550 are supplied with software Runtime Libraries for DOS, Windows 3.1, Windows 95/98 and Windows NT, and Menu programs for Windows 3.1, Windows 95/98 and Windows NT. This software is provided with the card at no extra cost.

ACE MENU OVERVIEW

The ACE Menu provides an interface for all ACE BC/RT/MT cards. For detailed information about the ACE Menu, please refer to the ACE Menu User's Guide.

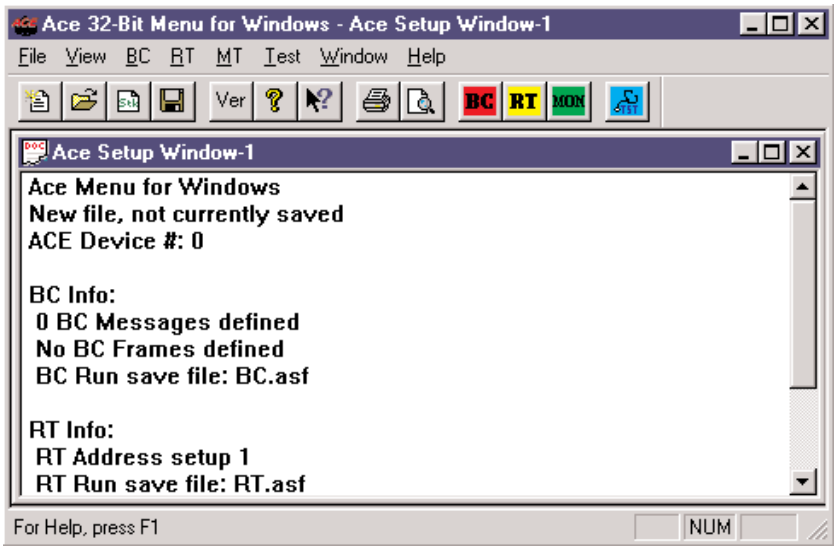


FIGURE 2. ACE SETUP WINDOW

Each of the operating modes, Bus Controller (BC), Remote Terminal (RT), and Monitor Terminal (MT) can be setup independently with all parameters being saved to an ACE setup file (*.ace). The card is only capable of running in one mode at a time. Each mode has its own run screen.

The ACE Menu is provides the necessary functionality for creating messages and assembling the messages into a frame for use by the BC function. The parameters for each message, including the command word, data words, and Bus selection are modifiable from the ACE Menu . Setup screens are available for setting other operational parameters such as Response Timeout, Retries and Stop-On criteria. Adding these messages to a frame structure creates a BC frame. The ACE Menu allows a frame to be a composition of many minor frames, where each minor frame will represent the same amount of time, but is not restricted to the same number of messages. The minor frame time is operator programmable. The number of minor frames times the minor frame time represents the Major Frame time. Once the frame is complete, the BC Run screen can be used to control the processing of the BC Frame. This screen displays operational status and provides controls for setting the minor frame time, the number of frames to send, and communication stack setup. The Stack setup allows the user to set the name and size of the stack. The Stack file where the 1553 bus traffic will be stored, and may be viewed at a later time.

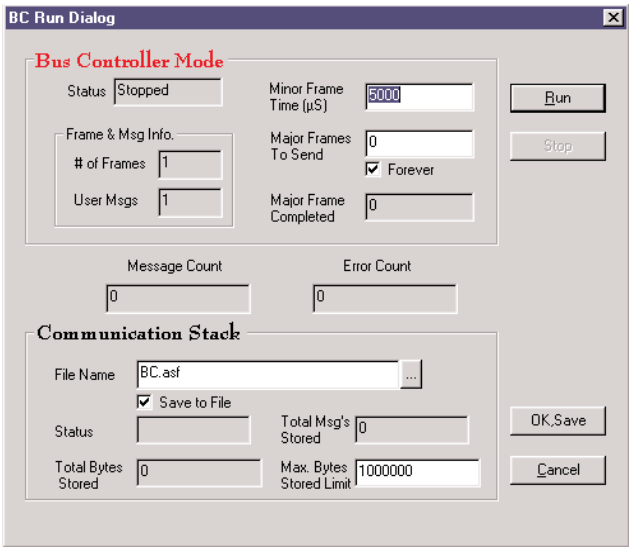


FIGURE 3. BC RUN DIALOG WINDOW

Communication information is saved in stack files (*.asf). The run screens allow configuration of the stack file location and size. All run modes provide the stack view capability. After running the card, the generated stack file can be viewed by opening the stack viewer. Within each of the operating mode tool bars and menus, there is an open stack button that allows quick access to the stack file open dialog. Once opened, the stack file can be searched for any type of message or error. These stack files are compatible with the previous version stack files for both the Windows 95 and Windows 3.xx ACE Menu programs.

The Remote Terminal mode operation allows setting the hardware to respond to a specified RT address. The setup for a RT is much simpler than that of a BC. The bulk of the setup is used to specify the data that should be returned based on the sub-address set in the message command word. The data edit screen provides controls to select the sub-address and enter the data. Once all of the sub-address responses have been determined, the operation of the RT is controlled in the Setup screen. The controls available here are the RT Address, Remote Terminal to Remote Terminal timeout, and status word bits set. Finally, the RT Run screen will provide options for setting the Remote Terminal Address, and the Stack File.

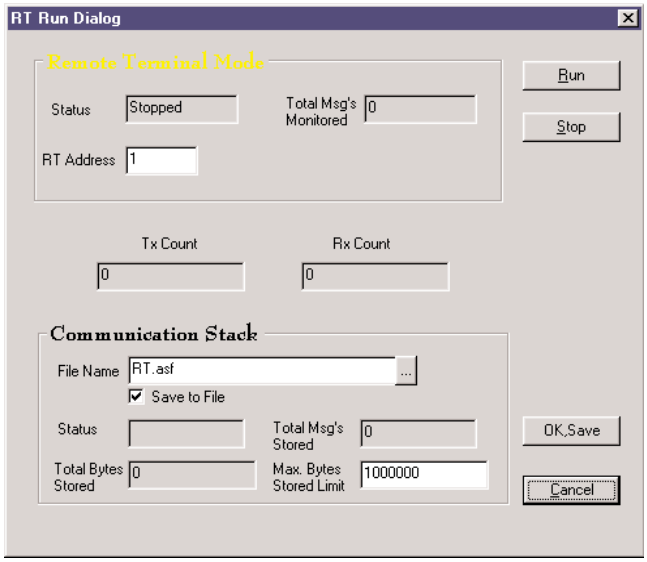


FIGURE 4. RT RUN DIALOG WINDOW

Monitor operation is also provided. The ACE Menu monitor is a full message monitor that will monitor the 1553 bus traffic, decode the messages (command and data) and save the information to a Stack File. The monitor is capable of filtering the message information based on Remote Terminal address, Sub-address, and Transmit/Receive for each message. When all of the appropriate filtering has been established, the Response Timeout option may be set. The timeout option instructs the Monitor as to how long it must wait before declaring a no response message. The Run Monitor screen has controls that allow setting the Stack File requirements, and to provide access to the Monitor Trigger capabilities. The monitor is capable of triggering its capture based on any combination of the command word bits, or based on any of the error bits in the RT Status Word.

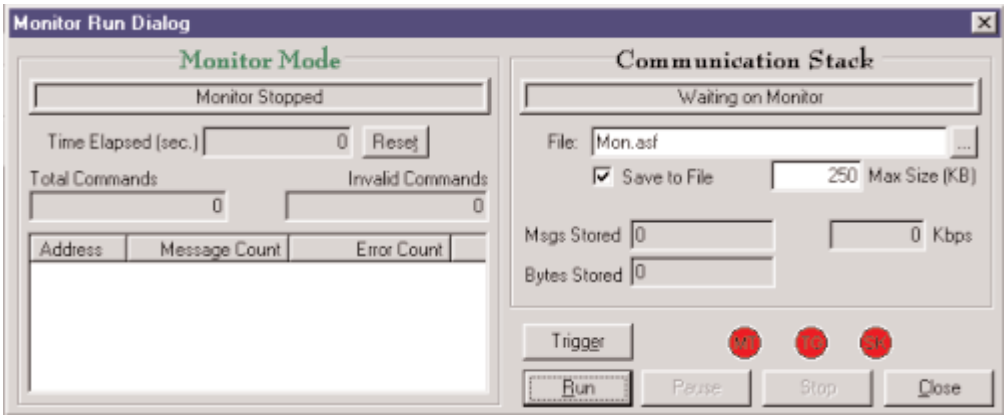


FIGURE 5. MONITOR MODE WINDOW

Finally, a Stack View capability is provided for each of the modes (BC, RT, and MT). From the Stack Button, a stack file can be selected, and viewed on the screen. Once the stack file is displayed, there is a capability of 'Finding' any message that was captured. The stack file contains information pertaining to the Storage Date, time and number of messages. It also contains the data portion of the messages, all pertinent status information, and text describing the error type.

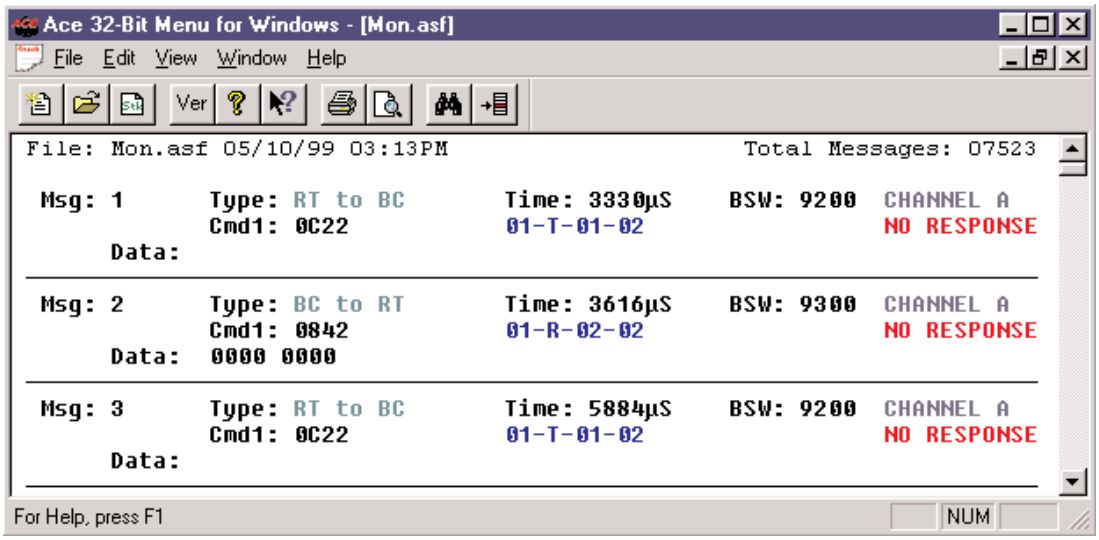


FIGURE 6. MONITOR MODE - STACK VIEW

The stack file can be searched by message command word, any data word, or any MIL-STD-1553 error. Each of the search criteria may be combined with a mask to allow searching for a family of command or data words. The search direction is selectable between up and down.

ACE RUNTIME LIBRARIES

The Runtime Libraries come in both 16-bit and 32-bit versions to support 16 and 32 bit DOS and Windows. Using the Runtime Library, applications may be created that are capable of controlling the PCMCIA card in either the BC, RT or MT mode. The newest version of this Runtime Library supports C and Visual Basic programming. Included with the ACE Runtime Library are sample applications for Bus Controller, Remote Terminal, and Monitor mode control. There are also sample programs for self-test and loop back tests. The self-test program tests and reports any errors found with the major portions of the hardware including registers, RAM, interrupt generation, and the protocol unit. The loop back tests force the BU-65552I/BU-65551I/BU-65550 card to communicate with itself. This test verifies the protocol unit and the transceivers to a greater degree than is performed by the Selftst2 program. The source for all of the test and sample programs is provided free of charge. These source programs may be used as a starting point for custom applications.

The following source code represents the simplicity of writing code for the BU-6555X PCMCIA cards. This program sends 10 words of data to RT 1 sub-address 5 on channel A, followed by a 32 word transmit to RT 6 sub-address 1 on channel 'A'. It then receives 5

words from RT 8 sub-address 4 on channel 'A', followed by a 32 word receive from RT 7 sub-address 2 on channel 'A'. Note that the creation of a 32 word message requires only that the data be defined in a buffer, and then a single function call to BuSendData(…) be made. Similarly, to receive data from a RT, a buffer must be defined, and a call to BuGetData(…) will be made. This encapsulated functionality relieves the application developer from having to know the dirty details of the 1553 protocol hardware and registers.

The following code is from the BCDEMO1.C sample program supplied with the BU-6555X hardware.

```
#include <stdio.h>
#include <stdlib.h>
#include <stdace.h>

void main ()
{
  BuConf_t  Conf; /* ACE library configuration type */
  BuError_t Err;  /* ACE library error status type  */

  U16BIT data[ 32]={  0X0000,0x1111,0x2222,0x3333,0x4444,0x5555,0x6666,0x7777,
0x8888,0x9999,0xAAAA,0xBBBB,0xCCCC,0xDDDD,0xEEEE,0xFFFF,
0x0001,0x0002,0x0004,0x0008,0x0010,0x0020,0x0040,0x0080,
0x0100,0x0200,0x0400,0x0800,0x1000,0x2000,0x4000,0x8000};

  /* display revision info */
  printf("%s\n\n",BuRev());
  printf("\nThis BC Demo sets the Ace card in BC mode and sends a few messages.\n\n");

  /* setup configuration for device X and open ACE library */
  printf("Choose the logical device # of your BC:> ");
  scanf("%d",&Conf.ConfDev);

  Err=BuOpen32(&Conf);
  if(Err) {
          printf("BuError %d %s\n",Err,BuErrorStr(Err));
          return;
  }

  /* opens bus controller mode */
  BuBCOpen();

  /* send 10 words to rt 5 sa 1 on channel A */
  Err=BuBCSendData(CW_CHANNELA,5,1,data,10);
  printf("%s\n",BuErrorStr(Err));

  /* send 32 words to rt 6 sa 1 on channel A
     added this [ 01-SEP-1995] to test 32 word case */
  Err=BuBCSendData(CW_CHANNELA,6,1,data,32);
  printf("%s\n",BuErrorStr(Err));

  /* receive 5 words from rt 8 sa 4 on channel A */
  Err=BuBCGetData(CW_CHANNELA,8,4,data,5);
  printf("%s\n",BuErrorStr(Err));

  /* display data */
  if(!Err){int x;for(x=0;x<5;x++)printf("%04x ",data[ x] );printf("\n");}

  /* receive 32 words from rt 7 sa 2 on channel A
     added this [ 01-SEP-1995] to test 32 word case */
  Err=BuBCGetData(CW_CHANNELA,7,2,data,32);
  printf("%s\n",BuErrorStr(Err));

  /* display data */
  if(!Err){int x;for(x=0;x<32;x++)printf("%04x ",data[ x] );}

  /* closes bus controller mode */
  BuBCClose();

  /* must call at end of ACE library use */
  BuClose();

}
```

TABLE 4. INTERRUPT MASK REGISTER (READ/WRITE 00H)	
BIT	**DESCRIPTION**
15 (MSB)	RESERVED
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	RT MODE CODE/MT PATTERN TRIGGER
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	STATUS SET
0 (LSB)	END OF MESSAGE

TABLE 5. CONFIGURATION REGISTER #1 (READ/WRITE 02H)				
BIT	**BC FUNCTION (Enhanced Mode Only Bits 11-0)**	**RT WITHOUT ALTERNATE STATUS**	**RT WITH ALTERNATE STATUS (Enhanced Only)**	**MONITOR FUNCTION (Enhanced mode only bits 12-0)**
15 (MSB)	RT/$\overline{\text{BC-MT}}$ (logic 0)	(logic 1)	(logic 1)	(logic o)
14	MT/$\overline{\text{BC-RT}}$ (logic 0)	(logic 0)	(logic 0)	(logic 1)
13	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\overline{\text{A}}$	CURRENT AREA B/$\overline{\text{A}}$
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)
11	FRAME STOP-ON-ERROR	$\overline{\text{DYNAMIC BUS CONTROL ACCEPTANCE}}$	S10	TRIGGER ENABLED WORD
10	STATUS SET STOP-ON-MESSAGE	$\overline{\text{BUSY}}$	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	$\overline{\text{SERVICE REQUEST}}$	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	$\overline{\text{SUBSYSTEM FLAG}}$	S07	NOT USED
7	EXTERNAL TRIGGER ENABLED	$\overline{\text{RTFLAG}}$ (Enhanced Mode Only)	S06	EXTERNAL TRIGGER ENABLED
6	INTERNAL TRIGGER ENABLED	NOT USED	S05	NOT USED
5	INTERMESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	DOUBLED/$\overline{\text{SINGLE}}$ RETRY	NOT USED	S02	NOT USED
2	BC ENABLED	NOT USED	S01	MONITOR ENABLED(Read Only)
1	BC FRAME IN PROGRESS (Read Only)	NOT USED	S00	MONITOR TRIGGERED (Read Only)
0 (LSB)	BC MESSAGE IN PROGRESS (Read Only)	RT MESSAGE IN PROGRESS (Enhanced mode only, Read Only)	RT MESSAGE IN PROGRESS (Read Only)	MONITOR ACTIVE (Read Only)

TABLE 6. CONFIGURATION REGISTER #2 (READ/WRITE 04H)	
BIT	**DESCRIPTION**
15 (MSB)	ENHANCED INTERRUPTS
14	LOGIC “0”
13	BUSY LOOKUP TABLE ENABLE
12	RX SA DOUBLE BUFFER ENABLE
11	OVERWRITE INVALID DATA
10	256-WORD BOUNDARY DISABLE
9	TIME TAG RESOLUTION 2(TTR2)
8	TIME TAG RESOLUTION 1 (TTR1)
7	TIME TAG RESOLUTION 0 (TTR0)
6	CLEAR TIME TAG ON SYNCHRONIZE
5	LOAD TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/PULSE* INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST
1	ENHANCED RT MEMORY MANAGEMENT
0 (LSB)	SEPARATE BROADCAST DATA

TABLE 7. START/RESET REGISTER (WRITE 06H)	
BIT	**DESCRIPTION**
15 (MSB)	RESERVED
•	•
•	•
•	•
7	RESERVED
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0 (LSB)	RESET

TABLE 8. BC/RT COMMAND STACK POINTER REG. (READ 06H)	
BIT	**DESCRIPTION**
15 (MSB)	COMMAND STACK POINTER 15
•	•
•	•
•	•
0 (LSB)	COMMAND STACK POINTER 0

TABLE 9. BC CONTROL WORD REGISTER (READ/WRITE 08H)	
BIT	**DESCRIPTION**
15 (MSB)	RESERVED
14	M.E. MASK
13	SERVICE REQUEST BIT MASK
12	SUBSYS BUSY BIT MASK
11	SUBSYS FLAG BIT MASK
10	TERMINAL FLAG BIT MASK
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/$\overline{B}$
6	OFF LINE SELF TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0 (LSB)	RT-RT FORMAT

TABLE 10. RT SUBADDRESS CONTROL WORD REGISTER (READ/WRITE 08H)	
BIT	**DESCRIPTION**
15 (MSB)	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)
5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST:MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0 (LSB)	BCST: MEMORY MANAGEMENT 0 (MM0)

TABLE 11. TIME TAG REGISTER (READ/WRITE 0AH)	
BIT	**DESCRIPTION**
15 (MSB)	TIME TAG 15
•	•
•	•
•	•
0 (LSB)	TIME TAG 0

TABLE 12. INTERRUPT STATUS REGISTER (READ/WRITE 0CH)	
BIT	**DESCRIPTION**
15 (MSB)	MASTER INTERRUPT
14	RAM PARITY ERROR
13	TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	RT MODE/MT PATTERN TRIGGER
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	RT SUBADDRESS CONTROL WORD EOM
3	BC END OF FRAME
2	FORMAT ERROR
1	STATUS SET
0 (LSB)	END OF MESSAGE

TABLE 13. CONFIGURATION REGISTER #3 (READ/WRITE 0EH)	
BIT	**DESCRIPTION**
15 (MSB)	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACk SIZE 2
9	MT DATA STACk SIZE 1
8	MT DATA STACk SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE T/$\overline{R}$ ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	BUSY RX TRANSFER DISABLE
2	RAFT-FLAG WRAP ENABLE
1	1553A MODE CODES ENABLE
0 (LSB)	ENHANCED MODE CODE HANDLING

TABLE 14. CONFIGURATION REGISTER #4 (READ/WRITE1 0H)	
BIT	**DESCRIPTION**
15 (MSB)	EXTERNAL BIT WORD ENABLE
14	INHIBIT BIT WORD IF BUSY
13	MODE COMMAND OVERRIDE BUSY
12	EXPANDED BC CONTROL WORD ENABLE
11	BROADCAST MASK ENABLE/$\overline{XOR}$
10	RETRY IF -A AND M.E.
9	RETRY IF STATUS SET
8	1ST RETRY ALT/$\overline{SAME}$ BUS
7	2ND RETRY ALT/$\overline{SAME}$ BUS
6	VALID M.E./NO DATA
5	VALID BUSY/NO DATA
4	MT TAG GAP OPTION
3	LATCH RT ADDRESS WITH CONFIG #5
2	TEST MODE 2
1	TEST MODE 1
0 (LSB)	TEST MODE 0

TABLE 15. CONFIGURATION REGISTER #5 (READ/WRITE 12H)	
BIT	**DESCRIPTION**
15 (MSB)	12MHZ CLOCK SELECT
14	LOGIC “0”
13	EXTERNAL TX INHIBIT A, read only BU-65170/61580X6
12	EXTERNAL TX INHIBIT B, read only BU-65170/61580X6
11	EXPANDED CROSSING ENABLED
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	LOGIC “1”
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0 (LSB)	RT ADDRESS PARITY

TABLE 16. MONITOR DATA STACK ADDRESS REGISTER (READ/WRITE 14H)	
BIT	**DESCRIPTION**
15 (MSB)	MONITOR DATA STACK ADDRESS 15
•	•
•	•
•	•
0 (LSB)	MONITOR DATA STACK ADDRESS 0

TABLE 17. BC FRAME TIME REMAINING REGISTER (READ/WRITE 16H)	
BIT	**DESCRIPTION**
15 (MSB)	BC FRAME TIME REMAINING 15
•	•
•	•
•	•
0 (LSB)	BC FRAME TIME REMAINING 0
Note: resolution = 100 µs per LSB	

TABLE 18. BC MESSAGE TIME REMAINING REGISTER (READ 18H)	
BIT	**DESCRIPTION**
15 (MSB)	BC MESSAGE TIME REMAINING 15
•	•
•	•
•	•
0 (LSB)	BC MESSAGE TIME REMAINING 0
Note: resolution = 1 µs per LSB	

TABLE 19. BC FRAME TIME/RT LAST COMMAND/MT TRIGGER REGISTER (READ/WRITE 1AH)	
BIT	**DESCRIPTION**
15 (MSB)	BIT 15
•	•
•	•
•	•
0 (LSB)	BIT 0

TABLE 20. RT STATUS REGISTER (READ 1CH)	
BIT	**DESCRIPTION**
15 (MSB)	RT ADDRESS 4
14	RT ADDRESS 3
13	RT ADDRESS 2
12	RT ADDRESS 1
11	RT ADDRESS 0
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPT
0 (LSB)	TERMINAL FLAG

TABLE 21. RT BIT WORD REGISTER (READ 1EH)	
BIT	**DESCRIPTION**
15 (MSB)	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	CHANNEL B/$\overline{A}$
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED
4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNCH/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0 (LSB)	COMMAND WORD CONTENTS ERROR

TABLES 22 TO 25 ARE NOT REGISTERS, BUT THEY ARE WORDS STORED IN RAM:

TABLE 22. BC MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15 (MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	STATUS SET
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	MASKED STATUS SET
6	RETRY COUNT 1
5	RETRY COUNT 0
4	GOOD DATA BLOCK TRANSFER
3	WRONG STATUS ADDRESS/NO GAP
2	WORD COUNT ERROR
1	INCORRECT SYNC TYPE
0 (LSB)	INVALID WORD

TABLE 23. RT MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15 (MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	RT-RT FORMAT
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0 (LSB)	COMMAND WORD CONTENTS ERROR

TABLE 24. WORD MONITOR IDENTIFICATION WORD	
BIT	**DESCRIPTION**
15 (MSB)	GAP TIME
•	•
•	•
•	•
8	GAP TIME
7	WORD FLAG
6	$\overline{\text{THIS RT}}$
5	$\overline{\text{BROADCAST}}$
4	ERROR
3	COMMAND/$\overline{\text{DATA}}$
2	CHANNEL B/$\overline{A}$
1	CONTIGUOUS DATA/$\overline{\text{GAP}}$
0 (LSB)	$\overline{\text{MODE CODE}}$

TABLE 25. MESSAGE MONITOR MODE BLOCK STATUS WORD	
BIT	**DESCRIPTION**
15 (MSB)	EOM
14	SOM
13	CHANNEL B/$\overline{A}$
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0 (LSB)	COMMAND WORD CONTENTS ERROR

BUS CONTROLLER (BC) ARCHITECTURE

The BC protocol of the BU-65552, BU-65551 and BU-65550 implement all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of bits in the BC Control Word and the T/$\overline{R}$ bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The BC response timeout value is programmable with choices of 18, 22, 50, and 130 μs. The longer response timeout values allow for operation over long buses and/or the use of repeaters.

FIGURE 7 illustrates BC intermessage gap and frame timing. The BU-65552, BU-65551 and BU-65550 may be programmed to process BC frames of up to 512 messages with no processor intervention. It is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either internally, using a programmable BC frame timer, or from an external trigger input. The internal BC frame time is programmable up to 6.55 seconds in increments of 100 μs. In addition to BC frame time, intermessage gap time, defined as the start of the current message to the start of the subsequent message, is programmable on an individual message basis. The time between individual successive messages is programmable up to 65.5 ms, in increments of 1 μs.

BC MEMORY ORGANIZATION

TABLE 26 illustrates a typical memory map for BC mode. It is important to note that the only fixed locations for the BU-65552, BU-65551 and BU-65550 in the Standard BC mode are for the two Stack Pointers (address locations 0100 [hex] and 0104) and for the two Message Count locations (0101 and 0105). Enabling the Frame Auto-Repeat mode will reserve four more memory locations for use in the Enhanced BC mode; these locations are for the two Initial Stack Pointers (address locations 102 [hex] and 106) and for the Initial Message Count locations (103 and 107). The user is free to locate the Stack and BC Message Blocks anywhere else within the shared RAM address space.

TABLE 26. TYPICAL BC MEMORY ORGANIZATION (SHOWN FOR 12K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0101	Message Count A (fixed location)
0102	Initial Stack Pointer A (see note) (Auto-Frame Repeat Mode)
0103	Initial Message Count A (see note) (Auto-Frame Repeat Mode)
0104	Stack Pointer B
0105	Message Count B
0106	Initial Stack Pointer B (see note) (Auto-Frame Repeat Mode)
0107	Initial Message Count B (see note) (Auto-Frame Repeat Mode)
0108-012D	Message Block 0
012E-0153	Message Block 1
0154-0179	Message Block 2
•	•
•	•
•	•
2EC0-2EE5	Message Block 308Message Block 8
2EE6-2EFF	Not Used
2F00-2FFF	Stack B

Notes:
1) Used only in the Enhanced BC mode with Frame Auto-Repeat enabled.
2) Address represents the word offset from the memory base address in the common memory address space.
3) For the 65552, the memory spans from 0000(hex) to FFFF(hex), providing a full 64K words of shared RAM.

For simplicity of illustration, assume the allocation of the maximum length of a BC message for each message block in the typical BC memory map of TABLE 26. The maximum size of a BC message block is 38 words, for an RT-to-RT transfer of 32 Data Words (Control + 2 Commands + Loopback + 2 Status Words + 32 Data Words). Note, however, that this example assumes the disabling of the 256-word boundaries.

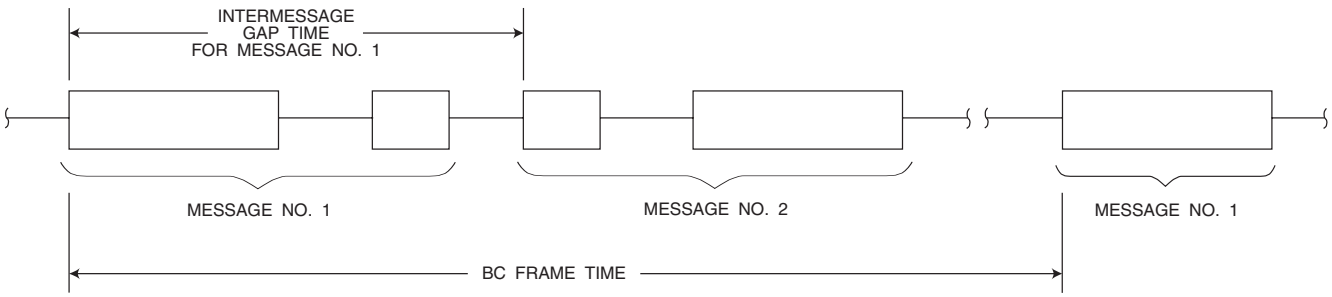


FIGURE 7. BC MESSAGE GAP AND FRAME TIMING

BC MEMORY MANAGEMENT

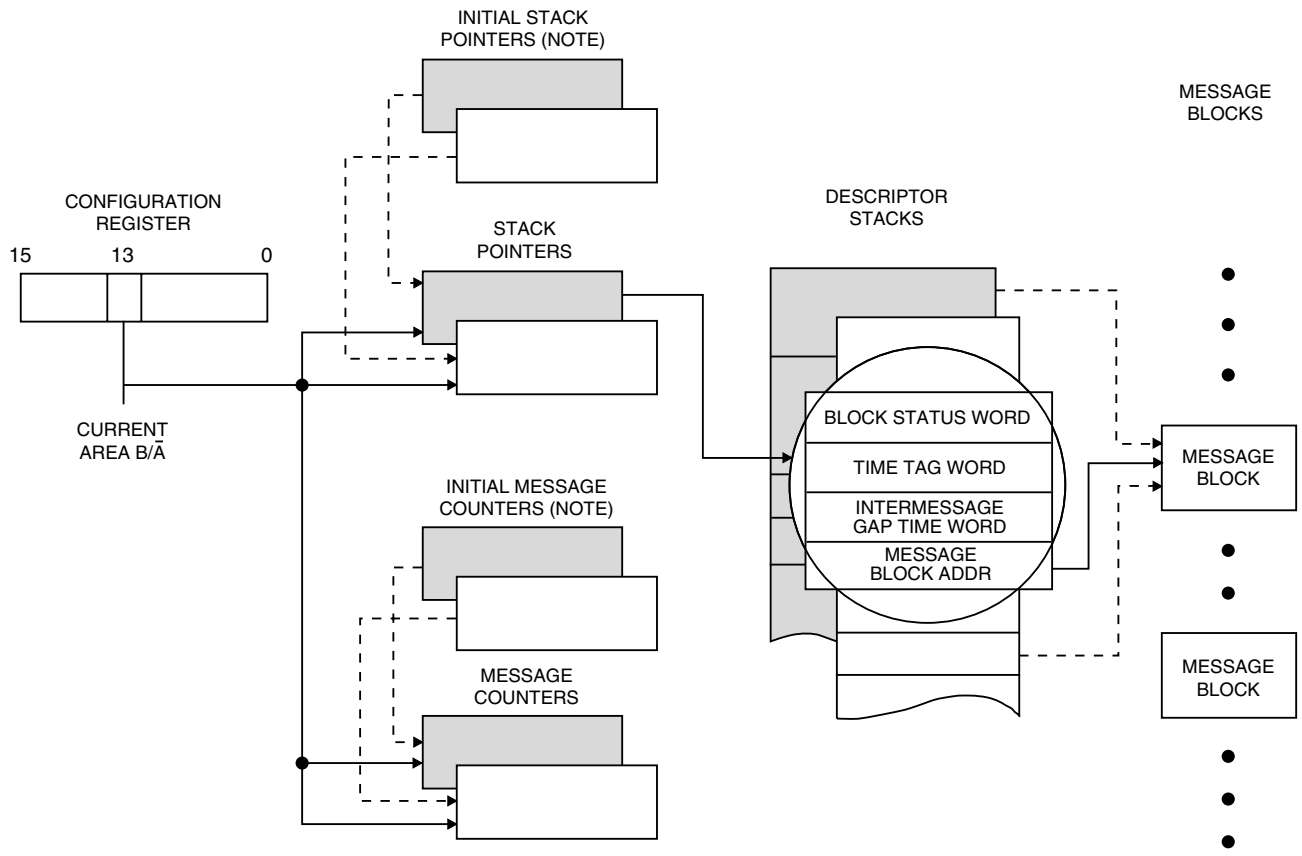
FIGURE 8 illustrates the BU-65552, BU-65551 and BU-65550 BC memory management scheme. One of the BC memory management features is the global double buffering mechanism. This provides for two sets of the various BC mode data structures: Stack Pointer and Message Counter locations, Descriptor Stack areas, and BC message blocks. Bit 13 of Configuration Register #1 selects the current active area. At any point in time, internal 1553 memory management logic may access only the various data structures within the "active" area. FIGURE 8 delineates the "active" and "inactive" areas by the non-shaded and shaded areas, respectively; however, **both the "active" and "nonactive" areas are always accessible by the host processor.** In most applications, the host processor will access the "nonactive" area, while the 1553 bus processes the "active" area messages.

The BC may be programmed to transmit multimessage frames of up to 512 messages. The number of messages to be processed is programmable by the Active Area Message Count location in the shared RAM, initialized by the host processor. In addition, the host processor must initialize another location, the Active Area Stack Pointer. The Stack Pointer references the four-word message block descriptor in the Stack area of shared RAM for each message to be processed. The BC Stack size is programmable with choices of 256, 512, 1024, and 2048 words.

In the BC Frame Auto-Repeat mode, the Initial Stack Pointer and Initial Message Counter locations must be loaded by the host prior to the processing of the first frame. The single frame mode does not use these two locations.

The third and fourth words of the BC block descriptor are the Intermessage Gap Time and the Message Block Address for the respective message. These two memory locations must be written by the host processor prior to the start of message processing. Use of the Intermessage Gap Time is optional. The Block Address pointer specifies the starting location for each message block. The first word of each BC message block is the BC Control Word.

At the start and end of each message, the Block Status and Time Tag Words write to the message block descriptor in the stack. The Block Status Word includes indications of message in process or message completion, bus channel, Status Set, response timeout, retry count, Status address mismatch, loop test (on-line self-test) failure, and other error conditions. TABLE 22 illustrates the bit mapping of the BC Block Status word. The 16-bit Time Tag Word will reflect the current contents of the internal Time Tag Register. This read/writable register, which operates for all three modes, has programmable resolution of from 2 to 64 μs/LSB. In addition, the Time Tag register may be clocked from an external source.



Note: Initial Stack Pointers and Initial Message Counters used only in BC Frame Auto-Repeat Mode.

FIGURE 18. BC MODE MEMORY MANAGEMENT

BC MESSAGE BLOCK FORMATS AND BC CONTROL WORD

In BC mode, the BU-65552, BU-65551 and BU-65550 support all MIL-STD-1553 message formats. For each 1553 message format, the BU-65552, BU-65551 and BU-65550 mandate a specific sequence of words within the BC Message Block. This includes locations for the Control, Command and (transmitted) Data Words that are to be read from RAM by the BC protocol logic. In addition, subsequent contiguous locations must be allocated for storage of received Loopback, RT Status and Data Words. FIGURE 9 illustrates the organization of the BC message blocks for the various MIL-STD-1553 message formats. Note that for all of the message formats, the BC Control Word is located in the first location of the message block.

For each of the BC Message Block formats, the first word in the block is the BC Control Word. The BC Control Word is **not** transmitted on the 1553 bus. Instead, it contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. The bit mapping and definitions of the BC Control Word are illustrated in TABLE 9.

The BC Control Word is followed by the Command Word to be transmitted, and subsequently by a second Command Word (for an RT-to-RT transfer), followed by Data Words to be transmitted (for Receive commands). The location after the last word to be transmitted is reserved for the Loopback Word. The Loopback Word is an on-line self-test feature. The subsequent locations after the Loopback Word are reserved for received Status Words and Data Words (for Transmit commands).

AUTOMATIC RETRIES

The BU-65552, BU-65551 and BU-65550 BC implements automatic message retries. When enabled, retries will occur, following response timeout or format error conditions. As additional options, retries may be enabled when the Message Error Status Word bit is set by a 1553A RT or following a "Status Set" condition. For a failed message, either one or two message retries will occur, the bus channel (same or alternate) is independently programmable for the first and second retry attempts. Retries may be enabled or disabled on an individual message basis.

BC INTERRUPTS

BC interrupts may be enabled by the Interrupt Mask Register for Stack Rollover, Retry, End-of-Message (global), End-of-Message (in conjunction with the BC Control Word for individual messages), response timeout, message error, end of BC frame, and Status Set conditions. The definition of "Status Set" is programmable on an individual message basis by means of the BC Control Word. This allows for masking ("care/don't care") for the individual RT Status Word bits.

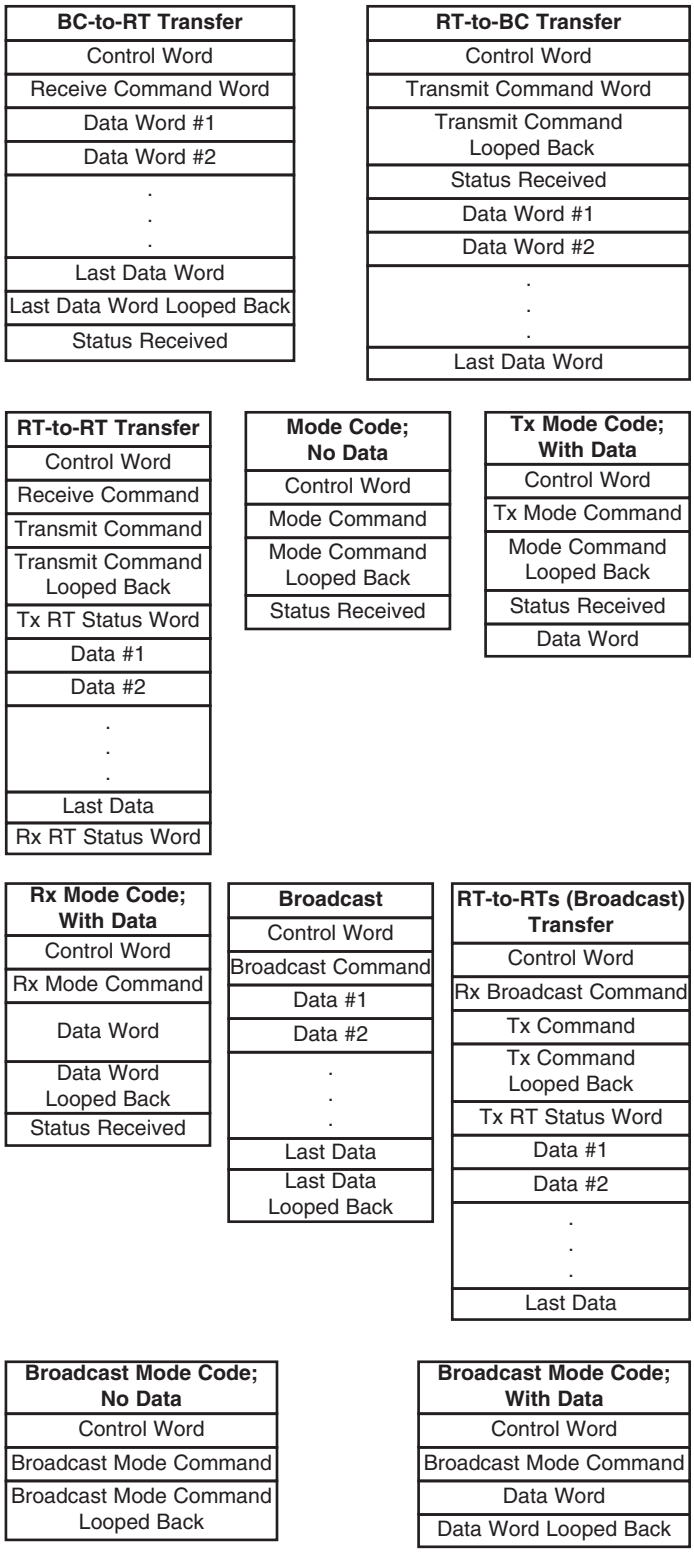


FIGURE 9. BC MESSAGE BLOCK FORMATS

REMOTE TERMINAL (RT) ARCHITECTURE

The RT protocol design of the BU-65552, BU-65551 and BU-65550 represent DDC's fifth generation implementation of a 1553 RT. One of the salient features of the ACE's RT architecture is its true multiprotocol functionality. This includes programmable options for support of MIL-STD-1553A, the various McAir protocols, and MIL-STD-1553B Notice 2. The BU-65552, BU-65551 and BU-65550 RT response time is 2 to 5 μs dead time (4 to 7 μs per 1553B), providing compliance to all the 1553 protocols. Additional multiprotocol features include options for full software control of RT Status and Built-in-Test (BIT) words. Alternatively, for 1553B applications, these words may be formulated in real-time by the BU-65552, BU-65551 and BU-65550 protocol logic. The BU-65552, BU-65551 and BU-65550 RT protocol design implements all the MIL-STD-1553B message formats and dual redundant mode codes. This design is based largely on previous generation products that have passed SEAFAC testing for MIL-STD-1553B compliance. The ACE RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. Other key features RT include a set of interrupt conditions, internal command illegalization, and programmable busy by subaddress.

RT MEMORY ORGANIZATION

TABLE 27 illustrates a typical memory map for the BU-65552, BU-65551 and BU-65550 in RT mode. As in BC mode, the two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100 (hex) for the Area A Stack Pointer and address 0104 for the Area B Stack Pointer. Besides the Stack Pointer, for RT mode there are several other areas of the ACE address space designated as fixed locations. All RT modes of operation require the Area A and Area B Lookup Tables. Also allocated, are several fixed locations for optional features: Command Illegalization Lookup Table, Mode Code Selective Interrupt Table, Mode Code Data Table, and Busy Bit Lookup Table. It should be noted that any unenabled optional fixed locations may be used for general purpose storage (data blocks).

The RT Lookup tables, which provide a mechanism for mapping data blocks for individual Tx/Rx/Bcst-subaddresses to areas in the RAM, occupy address range locations are 0140 to 01BF for Area A and 01C0 to 023F for Area B. The RT lookup tables include Subaddress Control Words and the individual Data Block Pointers. If used, address range 0300-03FF will be dedicated as the illegalizing section of RAM. The actual Stack RAM area and the individual data blocks may be located in any of the nonfixed areas in the shared RAM address space.

RT MEMORY MANAGEMENT

Another salient feature of the ACE series products is the flexibility of its RT memory management architecture. The RT architecture allows the memory management scheme for each transmit, receive, or broadcast subaddress to be programmable on a subaddress basis. Also, in compliance with MIL-STD-1553B Notice 2, the BU-65552, BU-65551 and BU-65550 provide an option to separate data received from broadcast messages from nonbroadcast received data.Besides supporting a global double buffering scheme (as in BC mode), the ACE RT provides a pair of 128-word Lookup Tables for memory management control,

TABLE 27. TYPICAL RT MEMORY MAP (SHOWN FOR 12K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0101-0103	RESERVED
0104	Stack Pointer B (fixed location)
0105-0107	RESERVED
0108-010F	Mode Code Selective Interrupt Table (fixed area)
0110-013F	Mode Code Data (fixed area)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
0240-0247	Busy Bit Lookup Table (fixed area)
0248-025F	(not used)
0260-027F	Data Block 0
0280-02FF	Data Block 1-4
0300-03FF	Command Illegalizing Table (fixed area)
0400-041F	Data Block 5
0420-043F	Data Block 6
•	•
•	•
•	•
2FE0-2FFF	Data Block 356

Notes:
1) Address represents the word offset from the memory base address in the common memory address space.
3) For the 65552, the memory spans from 0000(hex) to FFFF(hex), providing a full 64K words of shared RAM.

programmable on a subaddress basis (refer to TABLE 28). The 128-word tables include 32-word tables for transmit message pointers and receive message pointers. There is also a third, optional Lookup Table for broadcast message pointers, providing Notice 2 compliance, if necessary.

The fourth section of each of the RT Lookup Tables stores the 32 Subaddress Control Words (refer to TABLE 10 and 28). The individual Subaddress Control Words may be used to select the RT memory management option and interrupt scheme for each transmit, receive, and (optionally) broadcast subaddress.

For each transmit subaddress, there are two possible memory management schemes: (1) single message; and (2) circular buffer. For each receive (and optionally broadcast) subaddress, there are three possible memory management schemes: (1) single message; (2) double buffered; and (3) circular buffer. For each transmit, receive and broadcast subaddress, there are two interrupt conditions programmable by the respective Subaddress Control Word: (1) after every message to the subaddress; (2) after a circular buffer rollover. An additional table in RAM may be used to enable interrupts following selected mode code messages.

When using the circular buffer scheme for a given subaddress, the size of the circular buffer is programmable by three bits of the

TABLE 28. RT LOOK-UP TABLES			
AREA A	**AREA B**	**DESCRIPTION**	**COMMENT**
0140 . . . 015F	01C0 . . . 01DF	Rx(/Bcst)_SA0 . . . Rx(/Bcst)_SA31	Receive (/Broadcast) Lookup Table
0160 . . . 017F	01E0 . . . 01FF	Tx_SA0 . . . Tx_SA31	Transmit Lookup Table
0180 . . . 019F	0200 . . . 021F	Bcst_SA0 . . . Bcst_SA31	Broadcast Lookup Table (Optional)
01A0 . . . 01BF	0220 . . . 023F	SACW_SA0 . . . SACW_SA31	Subaddress Control Word Lookup Table (Optional)

Note: Address represents the word offset from the memory base address in the common memory address space.

TABLE 29. SUBADDRESS CONTROL WORD Memory Management Subaddress Buffer Scheme				
MM2	**MM1**	**MM0**	**DESCRIPTION**	**COMMENT**
0	0	0	Single Message or Double Buffered	
0	0	1	128-Word	Circular Buffer of Specified Size
0	1	0	256-Word	
0	1	1	512-Word	
1	0	0	1024-Word	
1	0	1	2048-Word	
1	1	0	4096-Word	
1	1	1	8192-Word	

Subaddress Control Word (see TABLE 29). The options for circular buffer size are 128, 256, 512, 1024, 2048, 4096, and 8192 Data Words.

SINGLE MESSAGE MODE

FIGURE 10 illustrates the RT Single Message memory management scheme. When operating in default mode, the Single Message scheme is implemented for all transmit, receive, and broadcast subaddresses. In the Single Message mode (also in the Double Buffer and Circular Buffer modes), there is a global double buffering scheme, controlled by bit 13 of Configuration Register #1. This selects from between the two sets of the various data structures shown in the figure: the Stack Pointers (fixed addresses), Descriptor Stacks (user defined addresses), RT Lookup Tables (fixed addresses), and RT Data Word blocks (user defined addresses). FIGURES 27, 28, and 29 delineate the "active" and "nonactive" areas by the non-shaded and shaded areas, respectively.

As shown, the ACE stores the Command Word from each message received, in the fourth location within the message descriptor (in the stack) for the respective message. The $T/\overline{R}$ bit, subaddress field, and (optionally) broadcast/own address, index into the active area Lookup Table, to locate the data block pointer for the current message. RT memory management logic then accesses the data block pointer to locate the starting address for the Data Word block for the current message. The maximum size for an RT Data Word block is 32 words.

For a particular subaddress in the Single Message mode, there is overwriting of the contents of the data blocks for receive/broadcast subaddresses – or overreading, for transmit subaddresses. In the single message mode, it is possible to access multiple data blocks for the same subaddress. This, however, requires the intervention of the host processor to update the respective Lookup Table pointer.

To implement a data wraparound subaddress, as required by Notice 2 of MIL-STD-1553B, the Single Message scheme should be used for the wrap-around subaddress. Notice 2 recommends subaddress 30 as the wraparound subaddress.

CIRCULAR BUFFER MODE

FIGURE 11 illustrates the RT circular buffer memory management scheme. The circular buffer mode facilitates bulk data transfers. The size of the RT circular buffer, shown on the right side of the figure, is programmable from 128 to 8192 words (in even powers of 2) by the respective Subaddress Control Word. As in the single message mode, the host processor initially loads the individual Lookup Table entries. At the start of each message, the ACE stores the Lookup Table entry in the third position of the respective message block descriptor in the stack area of RAM, as in the Single Message mode. The ACE transfers Receive or Transmit Data Words to (from) the circular buffer, starting at the location referenced by the Lookup Table pointer.

At the end of a valid (or, optionally, invalid) message, the value of the Lookup Table entry updates to the next location after the last address accessed for the current message. As a result, Data Words for the next message directed to the same Tx/RX(/Bcst) subaddress will be accessed from the next contiguous block of address locations within the circular buffer. As a recommended option, the Lookup Table pointers may be programmed to not update following an invalid receive (or broadcast) message. This allows the 1553 bus controller to retry the failed message, resulting in the valid (retried) data overwriting the invalid data. This eliminates overhead for the RT's host processor. When the pointer reaches the lower boundary of the circular buffer (located at 128-, 256-, . . . 8192-word boundaries in the address space), the pointer moves to the top boundary of the circular buffer, as FIGURE 11 shows.

Implementing Bulk Data Transfers

The use of the Circular Buffer scheme is ideal for bulk data transfers; that is, multiple messages to/from the same subaddress. The recommendation for such applications is to enable the circular buffer interrupt request. By so doing, the routine transfer of multiple messages to the selected subaddress, **including errors and retries**, is transparent to the RT's host processor. By strategically initializing the subaddresses' Lookup Table pointer

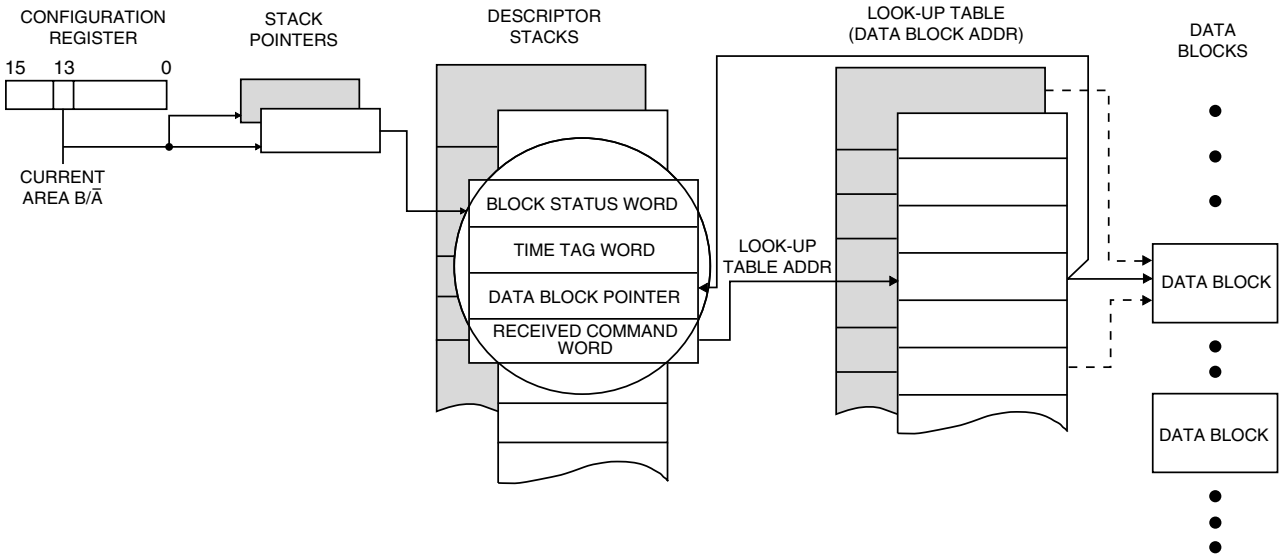


FIGURE 10. RT MEMORY MANAGEMENT: SINGLE MESSAGE MODE

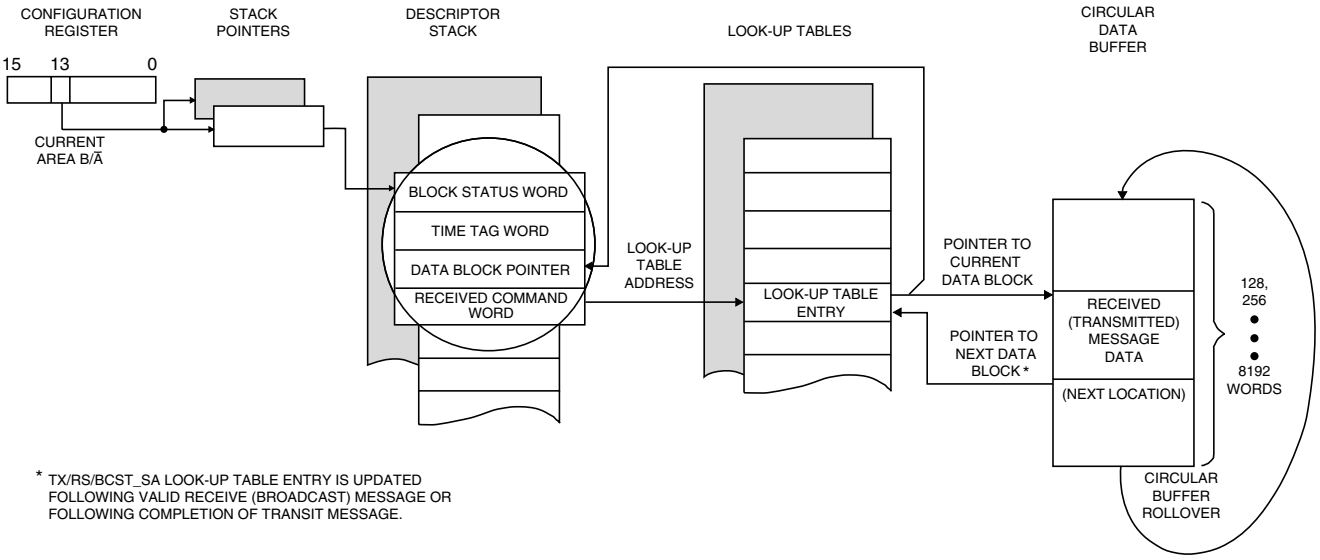


FIGURE 11. RT MEMORY MANAGEMENT: CIRCULAR BUFFER MODE

prior to the start of the bulk transfer, the BU-65550 and BU-65551 may be configured to issue an interrupt request only after it has received the anticipated number of valid Data Words to the designated subaddress.

SUBADDRESS DOUBLE BUFFERING MODE

For receive (and broadcast) subaddresses, the BU-65552, BU-65551 and BU-65550 RT offer a third memory management option, Subaddress Double Buffering. Subaddress double buffering provides a means of ensuring data consistency. FIGURE 12 illustrates the RT Subaddress Double Buffering scheme. Like the Single Message and Circular Buffer modes, the Double Buffering mode may be selected on a subaddress basis by means of the Subaddress Control Word. The purpose of the Double Buffering mode is to provide the host processor a convenient means of accessing the most recent, valid data received to a given subaddress. This serves to ensure the highest possible degree of data consistency by allocating **two** 32-bit Data Word blocks for each individual receive (and/or broadcast) subaddress.

At a given point in time, one of the two blocks will be designated as the "active" 1553 data block while the other will be designated as the "inactive" block. The Data Words from the next receive message to that subaddress will be stored in the "active" block. Upon completion of the message, provided that the message was valid and Subaddress Double Buffering is enabled, the BU-65552, BU-65551 and BU-65550 will automatically switch the "active" and "inactive" blocks for the respective subaddress. The ACE accomplishes this by toggling bit 5 of the subaddresses' Lookup Table Pointer and rewriting the pointer. As a result, the most recent valid block of received Data Words will always be readily accessible to the host processor.As a means of ensuring data consistency, the host processor is able to reliably access the most recent valid, received Data Word block by performing the following sequence:

(1) Disable the double buffering for the respective subaddress by the Subaddress Control Word. That is, temporarily switch the subaddresses' memory management scheme to the Single Message mode.

(2) Read the current value of the receive (or broadcast) subaddress's Lookup Table pointer. This points to the current "active" Data Word block. By inverting bit 5 of this pointer value, it is possible to locate the start of the "inactive" Data Word block. This block will contain the Data Words received during the most recent valid message to the subaddress.

(3) Read out the words from the "inactive" (most recent) Data Word Block.

(4) Re-enable the Double Buffering mode for the respective subaddress by the Subaddress Control Word.

RT INTERRUPTS

As in BC mode, the BU-65552, BU-65551 and BU-65550 RT provide many maskable interrupts. RT interrupt conditions include End of (every) Message, Message Error, Selected Subaddress (Subaddress Control Word) Interrupt, Circular Buffer Rollover, Selected Mode Code Interrupt, and Stack Rollover.

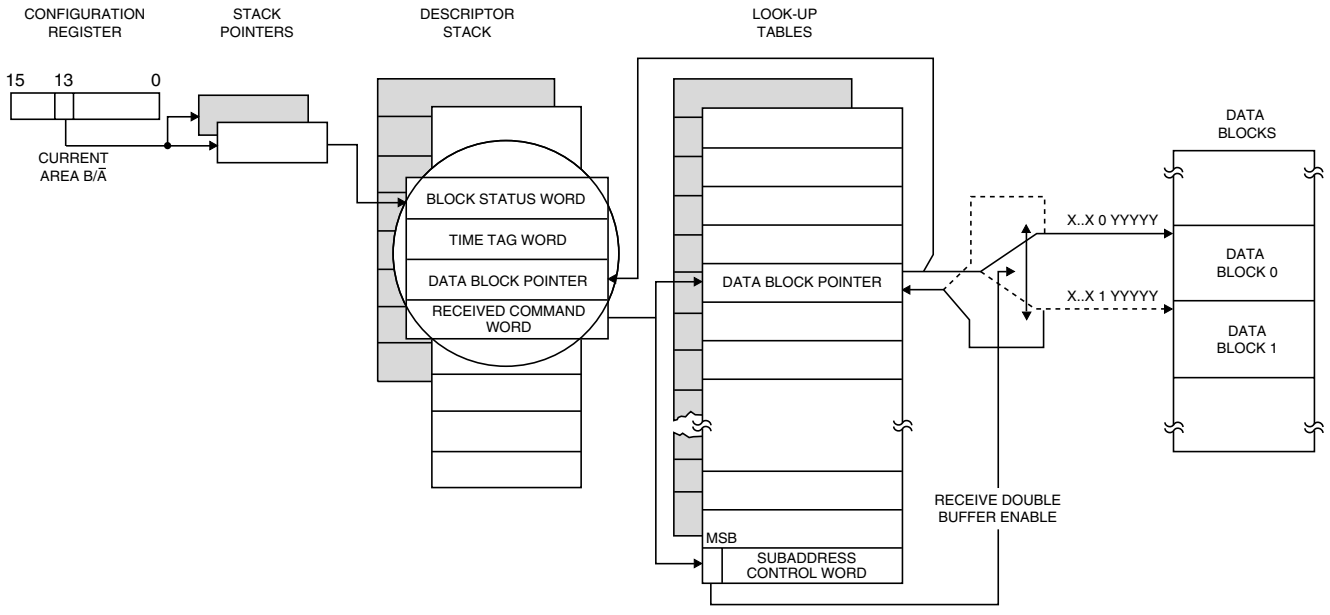


FIGURE 12. RT MEMORY MANAGEMENT: SUBADDRESS DOUBLE BUFFERING MODE

DESCRIPTOR STACK

At the beginning and end of each message, the BU-65552, BU-65551 and BU-65550 RT stores a four-word message descriptor in the active area stack. The RT stack size is programmable, with choices of 256, 512, 1024, and 2048 words. FIGURES 5, 6 and 7 show the four words: Block Status Word, Time Tag Word, Data Block Pointer, and the 1553 received Command Word. The RT Block Status Word includes indications of message in-progress or message complete, bus channel, RT-to-RT transfer and RT-to-RT transfer errors, message format error, loop test (self-test) failure, circular buffer rollover, illegal command, and other error conditions. TABLE 23 shows the bit mapping of the RT Block Status Word.

As in BC mode, the Time Tag Word stores the current contents of the BU-65552, BU-65551 and BU-65550 read/writable Time Tag Register. The resolution of the Time Tag Register is programmable from among 2, 4, 8, 16, 32, and 64 μs/LSB. Also, incrementing of the Time Tag counter may be from an external clock source or via software command.

The ACE stores the contents of the accessed Lookup Table location for the current message, indicating the starting location of the Data Word block, as the Data Block Pointer. This serves as a convenience in locating stored message data blocks. The ACE stores the full 16-bit 1553 Command Word in the fourth location of the RT message descriptor.

RT COMMAND ILLEGALIZATION

The BU-65552, BU-65551 and BU-65550 provide an internal mechanism for RT command illegalization. In addition, there is a means for allowing the setting of the Busy Status Word bit to be only for a programmed subset of the transmit/receive/broadcast subaddresses.

The illegalization scheme uses a 256-word area in the shared RAM address space. A benefit of this feature is the reduction of printed circuit board requirements, by eliminating the need for ~~an~~ external PROM, PLD, or RAM device that does the illegalizing function. The BU-65552, BU-65551 and BU-65550 illegalization scheme provides maximum flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/$\overline{R}$ bit, subaddress, and word count/mode code to be illegalized. Another advantage of the RAM-based illegalization technique is that it provides for a high degree of self-test ability.

Addressing The Illegalization Table

TABLE 30 illustrates the addressing scheme of the illegalization RAM . As shown, the base address of the illegalizing RAM is word address 0300 (hex) in the shared RAM. The ACE formulates the index into the Illegalizing Table based on the values of BROADCAST/OWN ADDRESS, T/$\overline{R}$ bit, Subaddress, and the MSB of the Word Count/Mode Code field (WC/MC4) of the current Command Word.

The internal RAM has 256 words reserved for command illegalization. Broadcast commands may be illegalized separately from non-broadcast receive commands and mode commands.

Commands may be illegalized down to the word count level. For example, a one-word receive command to subaddress 1 may be legal, while a two-word receive command to subaddress 1 may be illegalized.

The first 64 words of the Illegalization Table refer to broadcast receive commands (two words per subaddress). The next 64 words refer to broadcast transmit commands. Since nonmode code broadcast transmit commands are by definition invalid, this section of the table (except for subaddresses 0 and 31) does not need to be initialized by the user. The next 64 words correspond to nonbroadcast receive commands. The final 64 words refer to nonbroadcast transmit commands. Messages with Word Count/Mode Code (WC/MC) fields between 0 and 15 may be illegalized by setting the corresponding data bits for the respective even-numbered address locations in the illegalization table. Likewise, messages with WC/MC fields between 16 and 31 may be illegalized by setting the corresponding data bits for the respective odd-numbered address locations in the illegalization table.

The following should be noted with regards to command illegalization:

(1)To illegalize a particular word count for a given broadcast/own address-T/$\overline{R}$ subaddress, the appropriate bit position in the respective illegalization word should be set to logic 1. A bit value of logic 0 designates the respective Command Word as a egal command. The BU-65552, BU-65551 and BU-65550 will respond to an illegalized non-broadcast command with the Message Error bit set in its RT Status Word.

(2)For subaddresses 00001 through 11110, the "WC/MC" field specifies the Word Count field of the respective Command Word. For subaddresses 00000 and 11111, the

TABLE 30. ILLEGALIZATION RAM ADDRESS DEFINITION

BIT	DESCRIPTION
15 (MSB)	0
14	0
13	0
12	0
11	0
10	0
9	1
8	1
7	$\overline{\text{BROADCAST}}$/OWNADDRESS
6	T/$\overline{R}$
5	SA4
4	SA3
3	SA2
2	SA1
1	SA0
0 (LSB)	WC4/MC4

"WC/MC" field specifies the Mode Code field of the respective Command Word.

(3)Since nonmode code broadcast transmit messages are not defined by MIL-STD-1553B, the 60 words in the illegalization RAM, addresses 0342 through 037D, corresponding to these commands do not need to be initialized. They **will not respond** to a non-mode code broadcast transmit command, but will automatically set the Message Error bit in its internal Status Register, regardless of whether or not corresponding bit in the illegalization RAM has been set. If the next message is a Transmit Status or Transmit Last Command mode code, they will respond with its Message Error bit set.

PROGRAMMABLE BUSY

As a means of providing compliance with Notice 2 of MIL-STD-1553B, the BU-65552, BU-65551 and BU-65550 RT provide a software controllable means for setting the Busy Status Word bit as a function of subaddress. By a Busy Lookup Table in the shared RAM space, it is possible to set the Busy bit based on command broadcast/own address, $T/\overline{R}$ bit, and subaddress. Another programmable option, allows received Data Words to be either stored or not stored for messages, when the Busy bit is set.

OTHER RT FUNCTIONS

The BU-65552, BU-65551 and BU-65550 allow the hardwired RT Address to be read by the host processor. Also, there are options for the RT FLAG Status Word bit to be set under software control and/or automatically following a failure of the loopback self-test. Other software controllable RT options include software programmable RT Status and RT BIT words, automatic clearing of the Service Request Status Word bit following a Transmit Vector Word mode command, capabilities to clear and/or load the Time Tag Register following receipt of Synchronize mode commands, options regarding Data Word transfers for the Busy and/or Message Error (Illegal) Status Word bits, and for handling of 1553A and reserved mode codes.

MONITOR (MT) ARCHITECTURE

The BU-65552, BU-65551 and BU-65550 provide three bus monitor (MT) modes:

(1) The "AIM-HY" (default) or "AIM-HY'er" Word Monitor mode.

(2) A Selective Message Monitor mode.

(3) A Simultaneous Remote Terminal/Selective Message Monitor mode.

The strong recommendation for new applications is the use of the Selective Message Monitor, rather than the Word Monitor. Besides providing monitor filtering based on RT Address, $T/\overline{R}$ bit, and Subaddress, the Message Monitor eliminates the need to determine the start and end of messages by software. The development of such software tends to be a tedious task. Moreover, at run time, it tends to entail a high degree of CPU overhead.

WORD MONITOR

In the Word Monitor mode, the BU-65552, BU-65551 and BU-65550 monitor both 1553 buses. After initializing the Word Monitor and putting it on-line the BU-65552, BU-65551 and BU-65550 store all Command, Status, and Data Words received from both buses. For each word received from either bus, a pair of words are stored in shared RAM. The first word is the 16 bits of data from the received word. The second word is the Monitor Identification (ID), or "Tag" word. The ID Word contains information relating to bus channel, sync type, word validity, and interword time gaps. The BU-65552, BU-65551 and BU-65550 store data and ID words in a circular buffer in the shared RAM address space. TABLE 24 shows the bit mapping for the Monitor ID word.

MONITOR TRIGGER WORD

There is a Trigger Word Register that provides additional flexibility for the Word Monitor mode. The BU-65552, BU-65551 and BU-65550 store the value of the 16-bit Trigger Word in the MT Trigger Word Register. The contents of this register represent the value of the Trigger Command Word. There are programmable options to start or stop the Word Monitor, and/or to issue an interrupt request following receipt of the Trigger Command Word from the 1553 bus.

SELECTIVE MESSAGE MONITOR MODE

The BU-65552, BU-65551 and BU-65550 Selective Message Monitor provide features to greatly reduce the software and processing burden of the host CPU. The Selective Message Monitor implements selective monitoring of messages from a dual 1553 bus, with the monitor filtering based on the RT Address, $T/\overline{R}$ bit, and Subaddress fields of received 1553 Command Words. The Selective Message Monitor mode greatly simplifies the host processor software by distinguishing between Command and Status Words. The Selective Message Monitor maintains two stacks in RAM: a Command Stack and a Data Stack.

SIMULTANEOUS RT/MESSAGE MONITOR MODE

The Selective Message Monitor may function as a purely passive monitor or may be programmed to function as a simultaneous RT/Monitor. The RT/Monitor mode provides complete Remote Terminal (RT) operation for the BU-65552, BU-65551 and BU-65550 strapped RT address and bus monitor capability for the other 30 nonbroadcast RT addresses. This allows it to simultaneously operate as a full function RT and "snoop" on all or a subset of the bus activity involving the other RTs on a bus. This type of operation is sometimes needed to implement a backup bus controller. The combined RT/Selective Monitor maintains three stack areas in the address space: an RT Command Stack, a Monitor Command Stack, and a Monitor Data Stack. The pointers for the various stacks have fixed locations in the shared RAM address space.

SELECTIVE MESSAGE MONITOR MEMORY ORGANIZATION

TABLE 31 illustrates a typical memory map for the ACE in the Selective Message Monitor mode. This mode of operation defines several fixed locations in the RAM. These locations allocate in a manner that is compatible with the combined RT/Selective Message Monitor mode. Refer to FIGURE 13 for an example of a typical Selective Message Monitor Memory Map.

The fixed memory map consists of two Monitor Command Stack Pointers (location 102h and 106h), two Monitor Data Stack Pointers (locations 103h and 107h), and a Selective Message Monitor Lookup Table (0280-02FFh) based on RT Address, T/$\overline{R}$, and subaddress. Assume a Monitor Command Stack size of 1K words, and a Monitor Data Stack size of 2K words

Refer to FIGURE 13 for an illustration of the Selective Message Monitor operation. Upon receipt of a valid Command Word, the BU-65552, BU-65551 and BU-65550 will reference the Selective Monitor Lookup Table (a fixed block of addresses) to check for the condition (disabled/enabled) of the current command. If disabled, it will ignore (and not store) the current message; if enabled, it will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer.

Similar to RT mode, The ACE stores a Block Status Word, 16-bit Time Tag Word, and Data Block Pointer in the Message Descriptor, along with the received 1553 Command Word following reception of the Command Word. The ACE writes the Block Status and Time Tag Words at both the start and end of the message. The Monitor Block Status Word contains indications of message in-progress or message complete, bus channel, Monitor Data Stack Rollover, RT-to-RT transfer and RT-to-RT transfer errors, message format error, and other error conditions.

TABLE 31. TYPICAL SELECTIVE MESSAGE MONITOR MEMORY MAP (SHOWN FOR 12K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-0101	Not Used
0102	Monitor Command Stack Pointer A (fixed location)
0103	Monitor Data Stack Pointer A (fixed location)
0104-0105	Not Used
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0260-027F	Registers
0280-02FF	Selective Monitor Lookup Table (fixed area)
0300-03FF	Not Used
0400-07FF	Monitor Command Stack A
0800-0BFF	Monitor Command Stack B
0C00-0FFF	Not Used
1000-1FFF	Monitor Data Stack A
2000-2FFF	Monitor Data Stack B

Notes:
1) Address represents the word offset from the memory base address in the common memory address space.
3) For the 65552, the memory spans from 0000(hex) to FFFF(hex), providing a full 64K words of shared RAM.

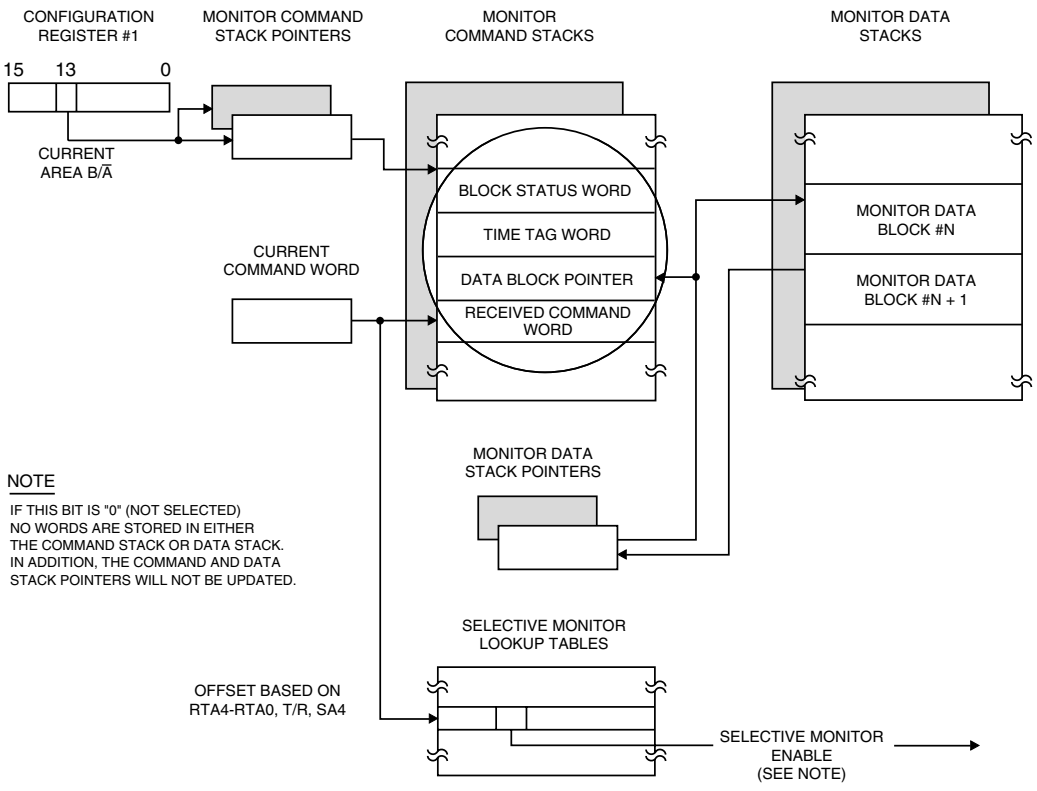


FIGURE 13. SELECTIVE MESSAGE MONITOR MEMORY MANAGEMENT

TABLE 25 shows the Message Monitor Block Status Word. The Data Block Pointer references the first word stored in the Monitor Data Stack (the first word following the Command Word) for the current message. The will then proceed to store the subsequent words from the message (possible second Command Word, Data Word(s), Status Word(s) into consecutive locations in the Monitor Data Stack.

The size of the Monitor Command Stack is programmable to 256, 1K, 4K, or 16K words. The Monitor Data Stack size is programmable to 512, 1K, 2K, 4K, 8K, 16K, 32K, or 64K words.

Monitor interrupts may be enabled for Monitor Command Stack Rollover, Monitor Data Stack Rollover, and/or End-of-Message conditions. In addition, in the Word Monitor mode there may be an interrupt enabled for a Monitor Trigger condition.

INTERFACE TO MIL-STD-1553 BUS

FIGURES 9 through 14 illustrates the interface from the BU-65552, BU-65551 and BU-65550 to a 1553 bus for either transformer (long stub) or direct (short stub) coupling, plus the peak-to-peak voltage levels that appear at various points (when transmitting). Both coupling configurations require the use of an included cable assembly that interfaces directly to the PC Card. For the transformer (long stub) coupling configuration, a second transformer, referred to as a coupling transfer is required. In accordance with MIL-STD-1553B, the turns ratio of the coupling transformer is 1.0 to 1.4.

Both transformer and direct coupling configurations require an isolation resistor to be placed in series with each leg of the transformer connecting to the 1553 bus; this protects the bus against short circuit conditions in the transformers, stubs, or terminal components.

The standard cable provided with the BU-65552 (part number DDC-70093-1), BU-65551 (part number DDC-58708-1) and BU-65550 (part number DDC-57612) provide for a transformer coupled connection. The mating connector required on the stub cable is a Trompeter PL75 or equivalent connector. Direct coupling requires the use of a optional cable assembly (DDC-70093-1 for BU-65552, DDC-57613 for BU-65550, contact factory for BU-65551 cable assembly availability).

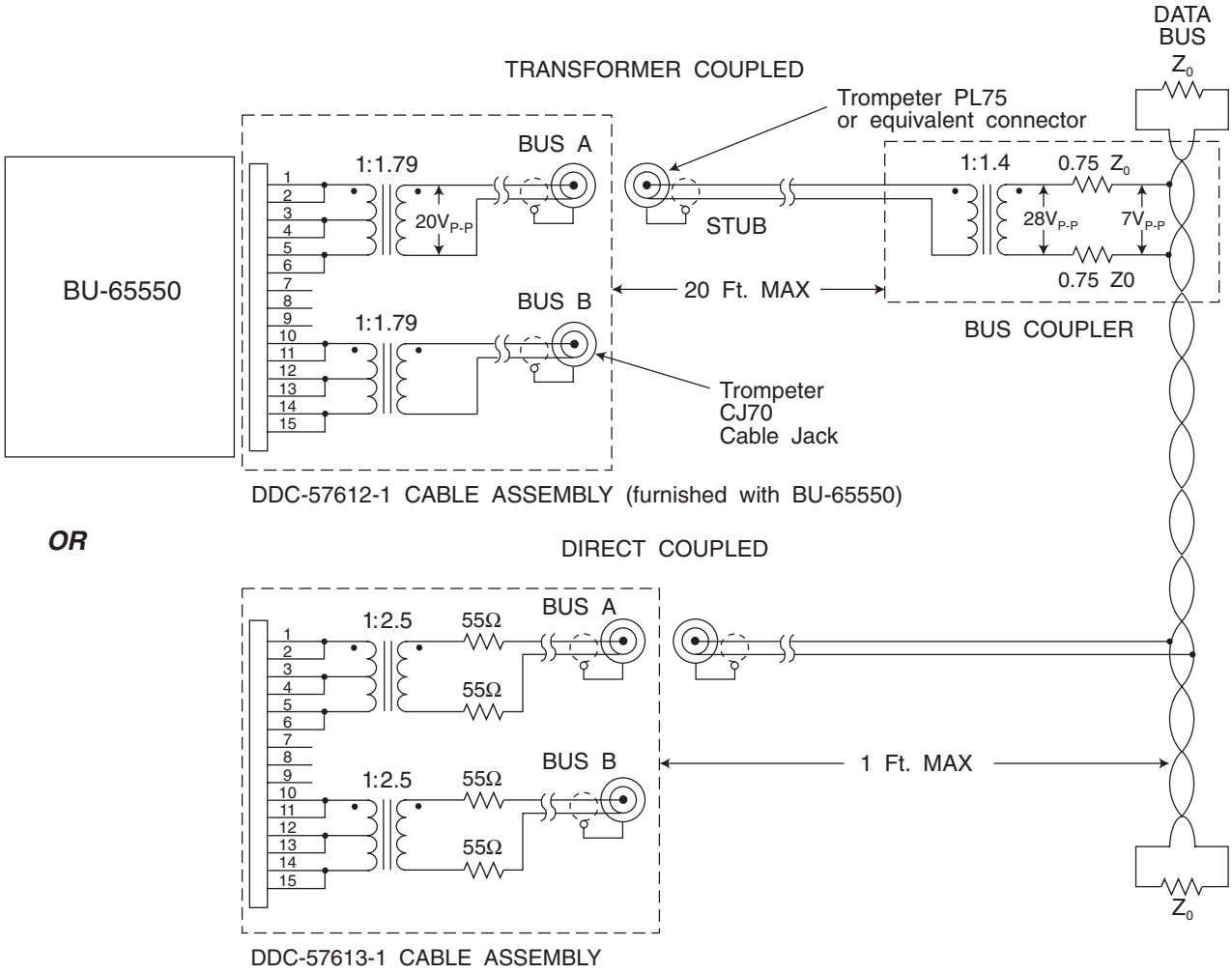
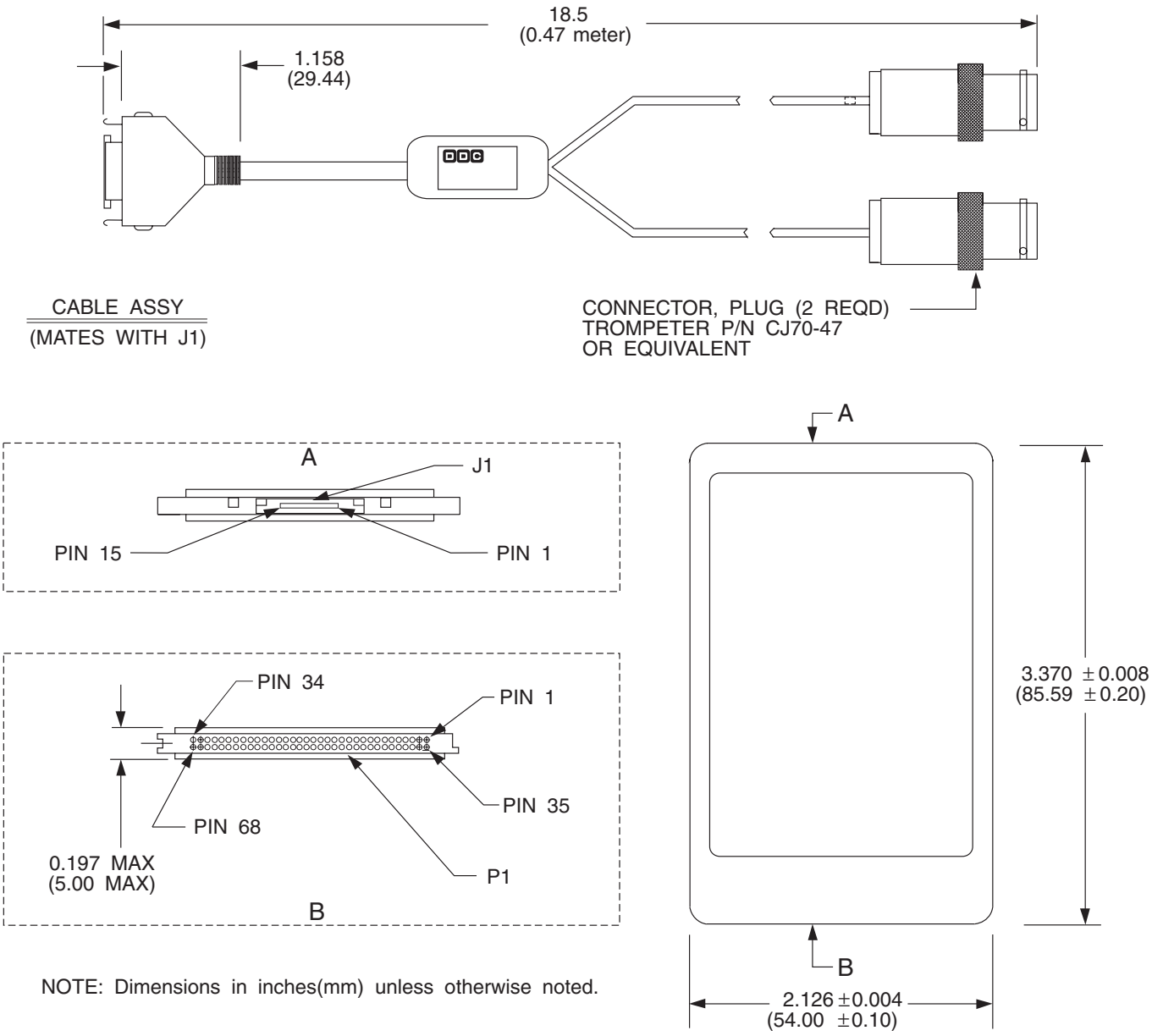


FIGURE 14. BU-65550 INTERFACE TO A MIL-STD-1553 BUS



NOTE: Dimensions in inches(mm) unless otherwise noted.

FIGURE 15. BU-65550 MECHANICAL OUTLINE, SHOWN WITH STANDARD DDC-57612-1 INTERFACE CABLE ASSEMLY

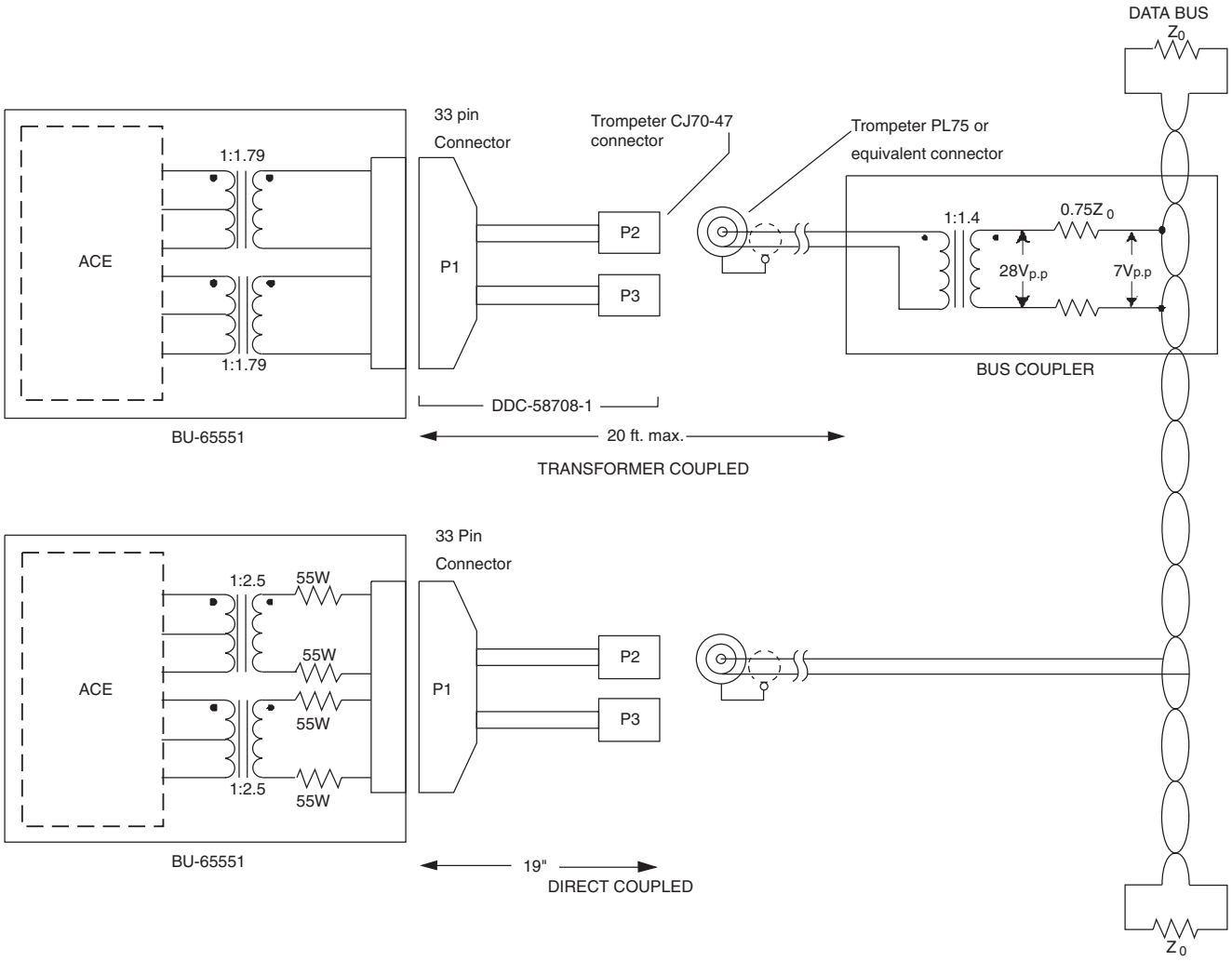
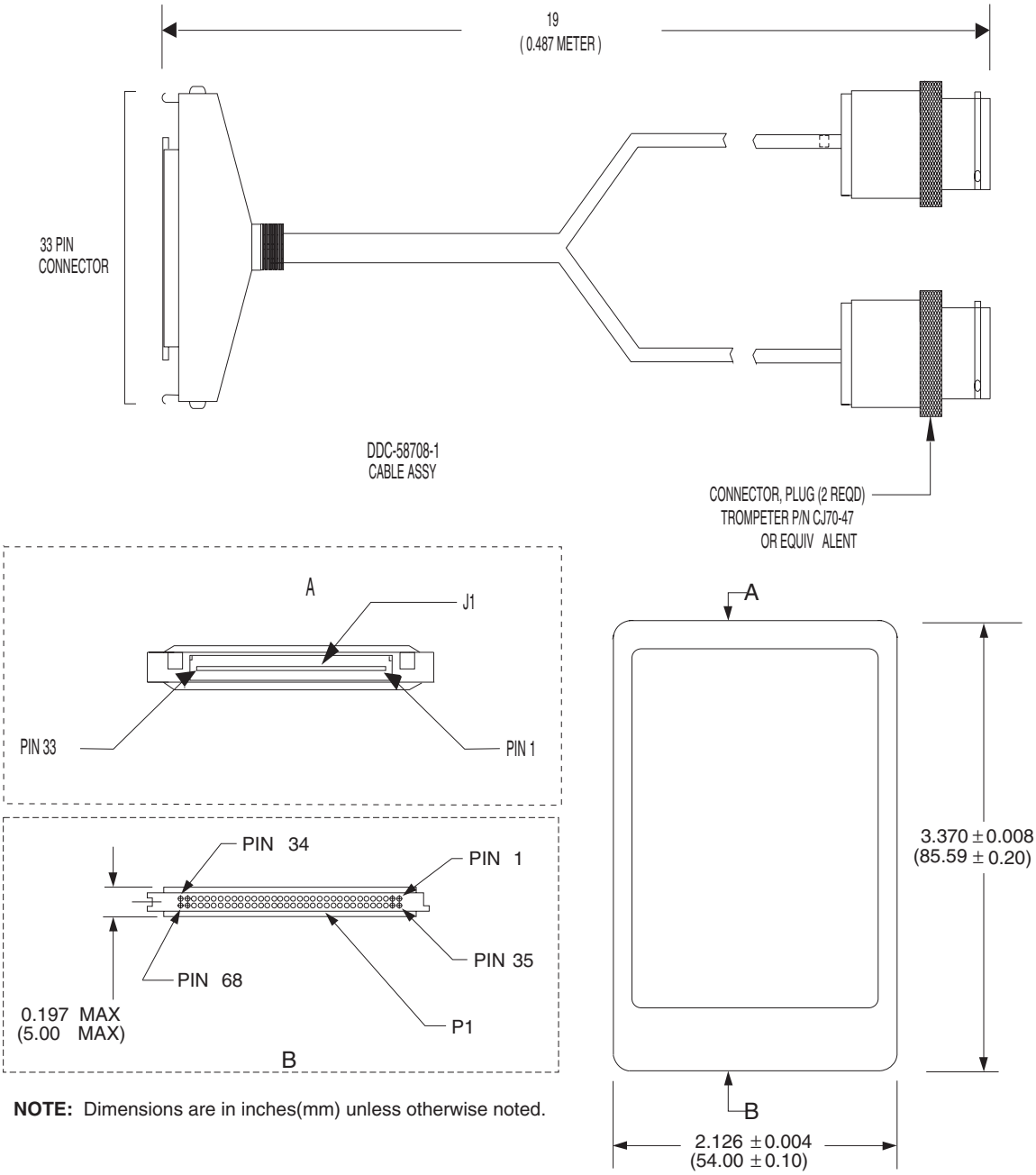
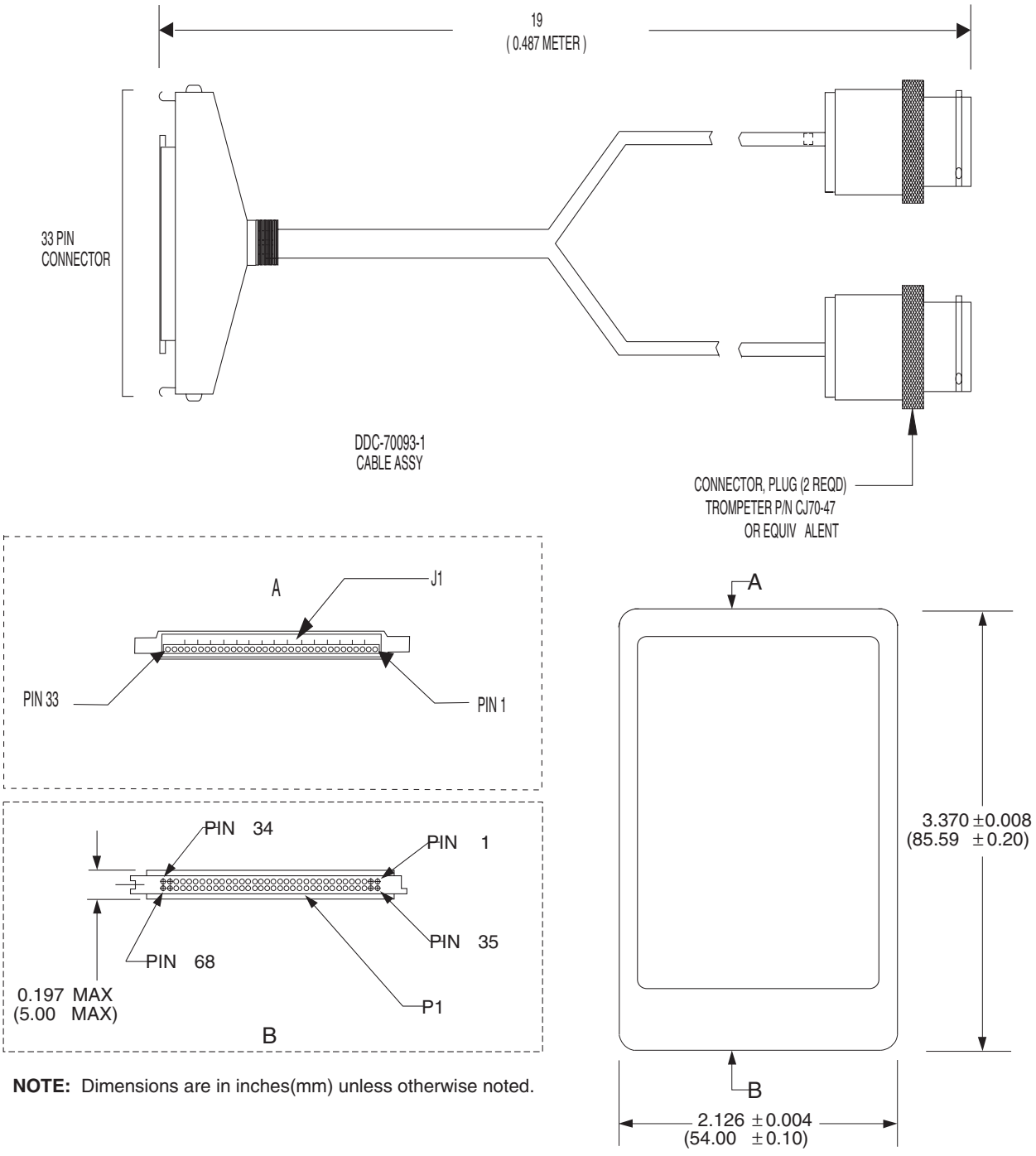


FIGURE 16. BU-65551 INTERFACE TO A MIL-STD-1553 BUS



NOTE: Dimensions are in inches(mm) unless otherwise noted.

FIGURE 17. BU-65551 MECHANICAL OUTLINE, SHOWN WITH STANDARD DDC-58708-1 INTERFACE CABLE ASSEMLY



NOTE: Dimensions are in inches(mm) unless otherwise noted.

FIGURE 18. BU-65552 MECHANICAL OUTLINE, SHOWN WITH STANDARD DDC-70093-1 INTERFACE CABLE ASSEMLY

CE MARK CERTIFICATION

The BU-65551M2-300 and the BU-65552M2-300 carry the CE MARK signifying conformance to the requirements of COUNCIL DIRECTIVE 89/336 EEC. The supporting test (reports) are on file at DDC, New York, USA and are available for on-site review.

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DECLARATION OF CONFORMITY

We Data Device Corporation
105 Wilbur Place
Bohemia, NY 11716-2482

declare under our sole responsibility that the product(s)
BU-65551M2-300
to which this declaration relates is in conformity with the following standard(s) or other normative document(s):

EN 55022-1: 1998 CLASS B; Conducted Emissions (150kHz to 30MHz)
CLASS B; Radiated Emissions (30MHz to 1GHz)

EN 50082-1: 1997 EN 61000-4-2:1995; Electrostatic Discharge
EN 61000-4-3:1997; Radiation Immunity
ENV 50204:1994; Radiated Immunity, Pulsed
EN 61000-4-4:1995; EFT/Burst, Power and I/O Leads
EN 61000-4-5:1995; Surge Immunity, Power Leads
EN 61000-4-6:1996; Conducted Immunity, Power and I/O Leads
EN 61000-4-11:1994; Voltage Dips and Interrupts

following the provisions of COUNCIL DIRECTIVE 89/336 EEC

Place Bohemia, NY USA
(Signature)

Date May 2, 2000
Joseph Saber
(Full Name)

Director, Product Assurance
(Position)

DDC-PAF-636A
04/05/2000

105 Wilbur Place • Bohemia • New York • 11716-2482
Tel: (631) 567-5600 • Fax: (631) 244-8252
www.ddc-web.com

DECLARATION OF CONFORMITY

We Data Device Corporation
105 Wilbur Place
Bohemia, NY 11716-2482

declare under our sole responsibility that the product(s)
BU-65552M2-300
to which this declaration relates is in conformity with the following standard(s) or other normative document(s):

EN 55022-1: 1998 CLASS B; Conducted Emissions (150kHz to 30MHz)
CLASS B; Radiated Emissions (30MHz to 1GHz)

EN 50082-1: 1997 EN 61000-4-2:1995; Electrostatic Discharge
EN 61000-4-3:1997; Radiation Immunity
ENV 50204:1994; Radiated Immunity, Pulsed
EN 61000-4-4:1995; EFT/Burst, Power and I/O Leads
EN 61000-4-5:1995; Surge Immunity, Power Leads
EN 61000-4-6:1996; Conducted Immunity, Power and I/O Leads
EN 61000-4-11:1994; Voltage Dips and Interrupts

following the provisions of COUNCIL DIRECTIVE 89/336 EEC

Place Bohemia, NY USA
(Signature)

Date May 2, 2000
Joseph Saber
(Full Name)

Director, Product Assurance
(Position)

DDC-PAF-637A
04/05/2000

ORDERING INFORMATION

BU-XXXXXMX-300

Test Criteria:
0 = None

Screening:
0 = Standard DDC Procedures

Temperature Range:
BU-65552 Series = 0 to +55°C
BU-65550 Series = 0 to +55°C
BU-65551 Series = -25 to +70°C

Cable Type:
0 = Without Cable
1 = Direct Coupled*
2 = Transformer Coupled**

Package:
M = Module

Product Type:
65552 = BC/RT/MT with 64K RAM, Isolation transformer inside interface card assembly.
65551 = BC/RT/MT with 4K RAM, Isolation transformer inside interface card assembly.
65550 = BC/RT/MT with 12K RAM, Isolation transformers part of cable assembly.

* Contact factory for Direct Coupled Cable Assembly for BU-65552 Series
** Includes DDC-70093-1, Transformer Coupled Cable Assembly for BU-65552 Series.

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* Contact Factory for Direct Coupled Cable Assembly for BU-65551 Series.
** Includes DDC-58708-1, Transformer Coupled Cable Assembly for BU-65551 Series.

* Includes DDC-57613-1, Direct Coupled Cable Assembly for BU-65550 Series.
** Includes DDC-57612-1, Transformer Coupled Cable Assembly for BU-65550 Series.

Standard Software:
BUS-69080 - 16-bit “C” Library
BUS-69081 - Windows 3.1 Menu
BUS-69082 - 32-bit Windows 95 DLL/Driver
BUS-69083 - 32-bit Windows 95 NT DLL/Driver
BUS-69084 - 32-bit Windows 95 Menu
BUS-69085 - 32-bit Windows 95 NT Menu

These products contain tin-lead solder.

The information in this data sheet is believed to be accurate; however, no responsibility is assumed by Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith.
Specifications are subject to change without notice.

Please visit our web site at **www.ddc-web.com** for the latest information.

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