



# FODM8071

## 3.3V/5V Logic Gate Output Optocoupler with High Noise Immunity

### Features

- High noise immunity characterized by common mode rejection
  - 20kV/μs minimum common mode rejection
- High speed
  - 20Mbit/sec date rate (NRZ)
  - 55ns max. propagation delay
  - 20ns max. pulse width distortion
  - 30ns max. propagation delay skew
- 3.3V and 5V CMOS compatibility
- Specifications guaranteed over 3V to 5.5V supply voltage and -40°C to +110°C temperature range
- Safety and regulatory approvals
  - UL1577, 3750 VAC<sub>RMS</sub> for 1 min.
  - IEC60747-5-2 (pending)

### Applications

- Microprocessor system interface
  - SPI, I<sup>2</sup>C
- Industrial fieldbus communications
  - DeviceNet, CAN, RS485
- Programmable logic control
- Isolated data acquisition system
- Voltage level translator

### Description

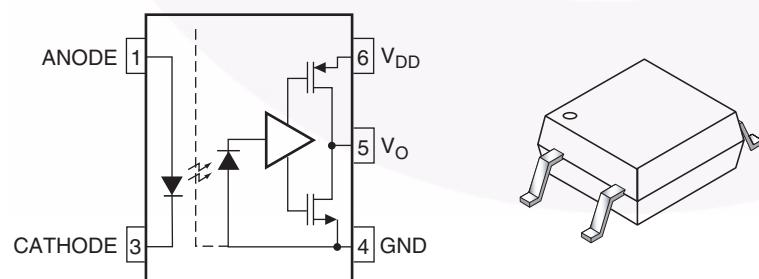
The FODM8071 is a 3.3V/5V high-speed logic gate output Optocoupler, which supports isolated communications allowing digital signals to communicate between systems without conducting ground loops or hazardous voltages. It utilizes Fairchild's patented coplanar packaging technology, Optoplanar®, and optimized IC design to achieve high noise immunity, characterized by high common mode rejection specifications.

This high-speed logic gate output optocoupler, housed in a compact 5-Pin Mini-Flat package, consists of a high-speed AlGaAs LED at the input coupled to a CMOS detector IC at the output. The detector IC comprises an integrated photodiode, a high-speed transimpedance amplifier and a voltage comparator with an output driver. The CMOS technology coupled with a high efficiency LED achieves low power consumption as well as very high speed (55ns propagation delay, 20ns pulse width distortion).

### Related Resources

- [www.fairchildsemi.com/products/opto/](http://www.fairchildsemi.com/products/opto/)
- [www.fairchildsemi.com/pf/FO/FOD8001.html](http://www.fairchildsemi.com/pf/FO/FOD8001.html)
- [www.fairchildsemi.com/pf/FO/FOD0721.html](http://www.fairchildsemi.com/pf/FO/FOD0721.html)

### Functional Schematic



### Truth Table

LED	Output
Off	High
On	Low

## Pin Definitions

Number	Name	Function Description
1	ANODE	Anode
3	CATHODE	Cathode
4	GND	Output Ground
5	$V_O$	Output Voltage
6	$V_{DD}$	Output Supply Voltage

## Safety and Insulation Ratings for Mini-Flat Package (SO5 Pin)

As per IEC60747-5-2 (Pending Certification). This optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For rated main voltage < 150Vrms		I-IV		
	For rated main voltage < 300Vrms		I-III		
	Climatic Classification		40/110/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
$V_{PR}$	Input to Output Test Voltage, Method b, $VIORM \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial Discharge < 5 pC	1060			V
$V_{PR}$	Input to Output Test Voltage, Method a, $VIORM \times 1.5 = V_{PR}$ , Type and Sample Test with $t_m = 60$ sec, Partial Discharge < 5 pC	848			V
$V_{IORM}$	Max Working Insulation Voltage	565			$V_{peak}$
$V_{IOTM}$	Highest Allowable Over Voltage	4000			$V_{peak}$
	External Creepage	5.0			mm
	External Clearance	5.0			mm
	Insulation Thickness	0.5			mm
$T_{Case}$	Safety Limit Values, Maximum Values allowed in the event of a failure, Case Temperature	150			°C
$R_{IO}$	Insulation Resistance at $T_{STG}, V_{IO} = 500V$	$10^9$			Ω

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. .

Symbol	Parameter	Value	Units
$T_{STG}$	Storage Temperature	-40 to +125	°C
$T_{OPR}$	Operating Temperature	-40 to +110	°C
$T_J$	Junction Temperature	-40 to +125	°C
$T_{SOL}$	Lead Solder Temperature (Refer to Reflow Temperature Profile)	260 for 10sec	°C
$I_F$	Forward Current	20	mA
$V_R$	Reverse Voltage	5	V
$V_{DD}$	Supply Voltage	0 to 6.0	V
$V_O$	Output Voltage	-0.5 to $V_{DD}+0.5$	V
$I_O$	Average Output Current	10	mA
$PD_I$	Input Power Dissipation <sup>(1)(3)</sup>	40	mW
$PD_O$	Output Power Dissipation <sup>(2)(3)</sup>	70	mW

### Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
$T_A$	Ambient Operating Temperature	-40	+110	°C
$V_{DD}$	Supply Voltages <sup>(4)</sup>	3.0	5.5	V
$V_{FL}$	Logic Low Input Voltage	0	0.8	V
$I_{FH}$	Logic High Input Current	5	16	mA
$I_{OL}$	Logic Low Output Current	0	7	mA

### Isolation Characteristics

(Apply over all recommended conditions, typical value is measured at  $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{ISO}$	Input-Output Isolation Voltage	freq = 60Hz, t = 1.0min, $I_{I-O} \leq 10\mu\text{A}$ <sup>(5)(6)</sup>	3750			V <sub>ACRMS</sub>
$R_{ISO}$	Isolation Resistance	$V_{I-O} = 500\text{V}$ <sup>(5)</sup>	$10^{11}$			Ω
$C_{ISO}$	Isolation Capacitance	$V_{I-O} = 0\text{V}$ , freq = 1.0MHz <sup>(5)</sup>		0.2		pF

#### Notes:

1. Derate linearly from 95°C at a rate of -1.4mW/°C
2. Derate linearly from 100°C at a rate of -3.47mW/°C.
3. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.
4. 0.1μF bypass capacitor must be connected between 4 and 6.
5. Device is considered a two terminal device: Pins 1, and 3 are shorted together and Pins 4, 5, and 6 are shorted together.
6. 3,750 VAC<sub>RMS</sub> for 1 minute duration is equivalent to 4,500 VAC<sub>RMS</sub> for 1 second duration.

**Electrical Characteristics** (Apply over all recommended conditions) $(T_A = -40^\circ\text{C} \text{ to } +110^\circ\text{C}, 3.0V \leq V_{DD} \leq 5.5V)$ , unless otherwise specified.Typical value is measured at  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3.3V$ .

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
<b>INPUT CHARACTERISTICS</b>						
$V_F$	Forward Voltage	$I_F = 10\text{mA}$ , Fig. 1	1.05	1.35	1.8	V
$BV_R$	Input Reverse Breakdown Voltage	$I_R = 10\mu\text{A}$	5	15		V
$I_{FHL}$	Threshold Input Current	Fig. 2		2.8	5	mA
<b>OUTPUT CHARACTERISTICS</b>						
$I_{DDL}$	Logic Low Output Supply Current	$V_{DD} = 3.3V, I_O = 10\mu\text{A}$ , Fig. 3, 5		3.3	4.8	mA
		$V_{DD} = 5.0V, I_O = 10\mu\text{A}$ , Fig. 3, 6		4.0	5.0	mA
$I_{DDH}$	Logic High Output Supply Current	$V_{DD} = 3.3V, I_O = 0\text{mA}$ , Fig. 4		3.3	4.8	mA
		$V_{DD} = 5.0V, I_O = 0\text{mA}$ , Fig. 4		4.0	5.0	mA
$V_{OH}$	Logic High Output Voltage	$V_{DD} = 3.3V, I_O = -20\mu\text{A}, I_F = 0\text{mA}$	$V_{DD} - 0.1V$	3.3		V
		$V_{DD} = 3.3V, I_O = -4\text{mA}, I_F = 0\text{mA}$	$V_{DD} - 0.5V$	3.1		V
		$V_{DD} = 5.0V, I_O = -20\mu\text{A}, I_F = 0\text{mA}$	$V_{DD} - 0.1V$	5.0		V
		$V_{DD} = 5.0V, I_O = -4\text{mA}, I_F = 0\text{mA}$	$V_{DD} - 0.5V$	4.9		V
$V_{OL}$	Logic Low Output Voltage	$I_O = 20\mu\text{A}, I_F = 10\text{mA}$		0.0027	0.01	V
		$I_O = 4\text{mA}, I_F = 10\text{mA}$		0.27	0.8	V

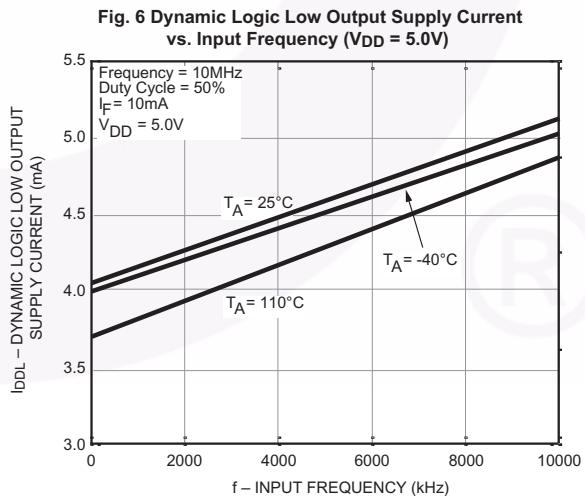
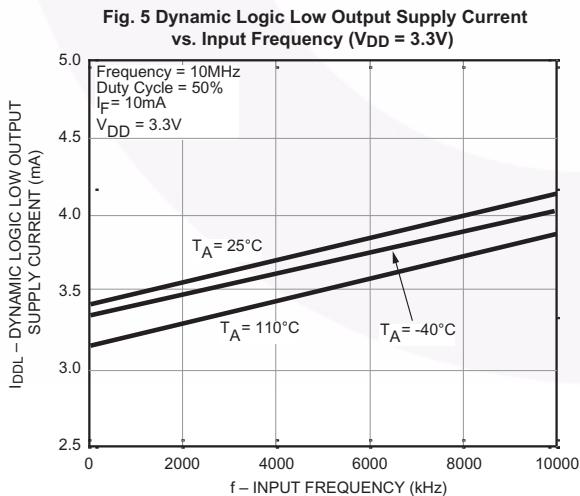
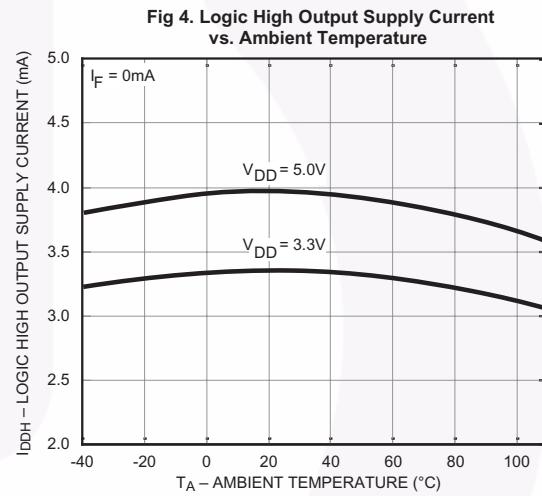
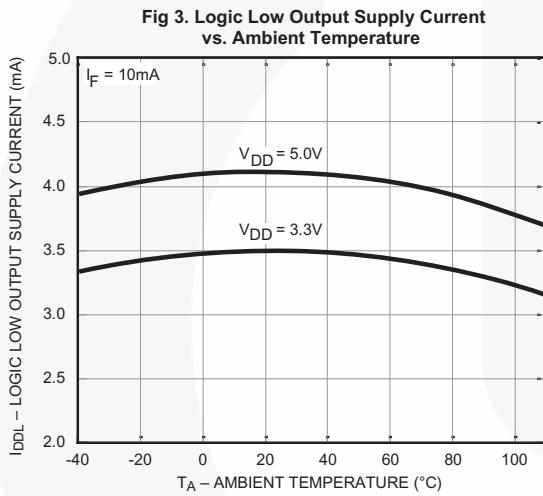
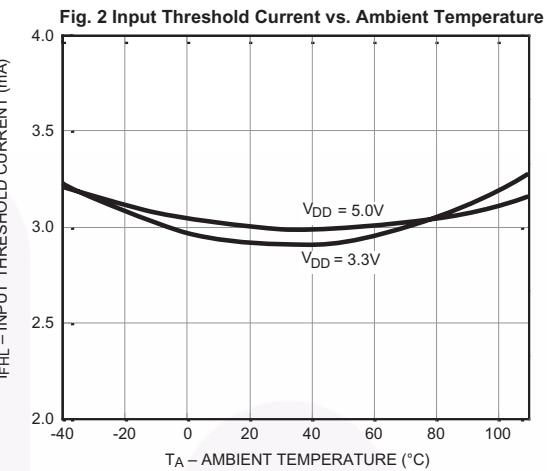
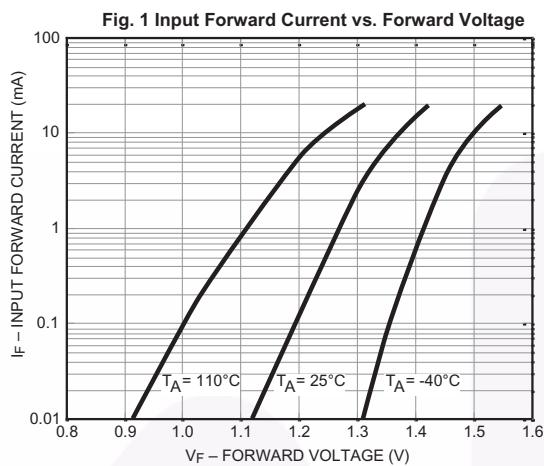
**Switching Characteristics** (Apply over all recommended conditions) $(T_A = -40^\circ\text{C} \text{ to } +110^\circ\text{C}, 3.0V \leq V_{DD} \leq 5.5V, I_F = 5\text{mA})$ , unless otherwise specified.Typical value is measured at  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3.3V$ 

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Date Rate <sup>(7)</sup>					20	Mbps
$t_{PW}$	Pulse Width		50			ns
$t_{PHL}$	Propagation Delay Time to Logic Low Output	$C_L = 15\text{pF}$ , Fig. 7, 8, 12		31	55	ns
$t_{PLH}$	Propagation Delay Time to Logic High Output	$C_L = 15\text{pF}$ , Fig. 7, 8, 12		25	55	ns
PWD	Pulse Width Distortion, $ t_{PHL} - t_{PLH} $	$C_L = 15\text{pF}$ , Fig. 9, 10		5.5	20	ns
$t_{PSK}$	Propagation Delay Skew	$C_L = 15\text{pF}$ <sup>(8)</sup>			30	ns
$t_R$	Output Rise Time (10% to 90%)	Fig. 11, 12		5.8		ns
$t_F$	Output Fall Time (90% to 10%)	Fig. 11, 12		5.3		ns
$ CM_H $	Common Mode Transient Immunity at Output High	$I_F = 0\text{mA}, V_O > 0.8V_{DD}, V_{CM} = 1000V, T_A = 25^\circ\text{C}$ , Fig. 13 <sup>(9)</sup>	20	40		kV/μs
$ CM_L $	Common Mode Transient Immunity at Output Low	$I_F = 5\text{mA}, V_O < 0.8V, V_{CM} = 1000V, T_A = 25^\circ\text{C}$ , Fig. 13 <sup>(9)</sup>	20	40		kV/μs
$C_{PD}$	Output Dynamic Power Dissipation Capacitance <sup>(10)</sup>			4		pF

**Notes:**

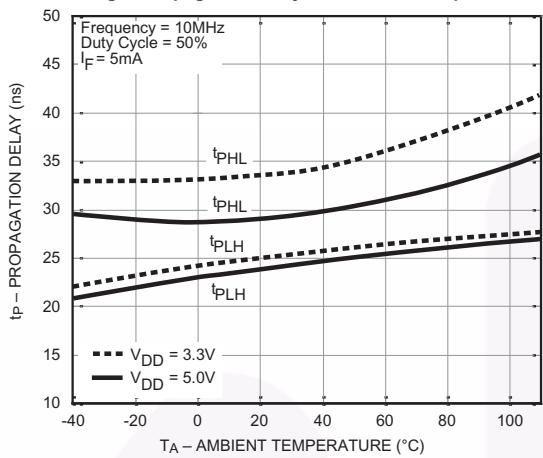
7. Data rate is based on 10MHz, 50% NRZ pattern with a 50nsec minimum bit time.
8.  $t_{PSK}$  is equal to the magnitude of the worst case difference in  $t_{PHL}$  and/or  $t_{PLH}$  that will be seen between any two units from the same manufacturing date code that are operated at same case temperature ( $\pm 5^\circ\text{C}$ ), at same operating conditions, with equal loads ( $R_L = 350\Omega$  and  $C_L = 15\text{pF}$ ), and with an input rise time less than 5ns.
9. Common mode transient immunity at output high is the maximum tolerable positive  $dV_{cm}/dt$  on the leading edge of the common mode impulse signal,  $V_{cm}$ , to assure that the output will remain high. Common mode transient immunity at output low is the maximum tolerable negative  $dV_{cm}/dt$  on the trailing edge of the common pulse signal,  $V_{cm}$ , to assure that the output will remain low.
10. Unloaded dynamic power dissipation is calculated as follows:  $C_{PD} \times V_{DD} \times f + I_{DD} + V_{PD}$  where  $f$  is switched time in MHz.

**Typical Performance Curves (Continued)**

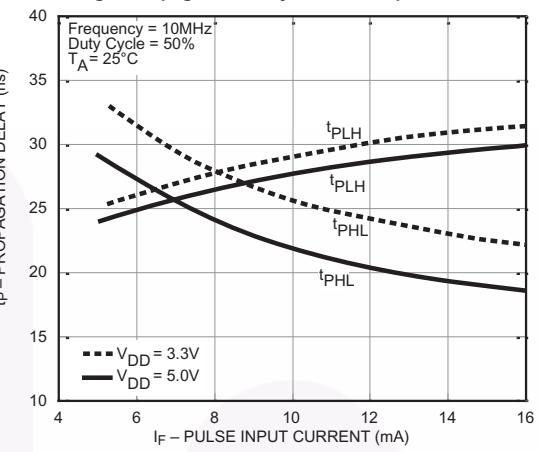


## Typical Performance Curves (Continued)

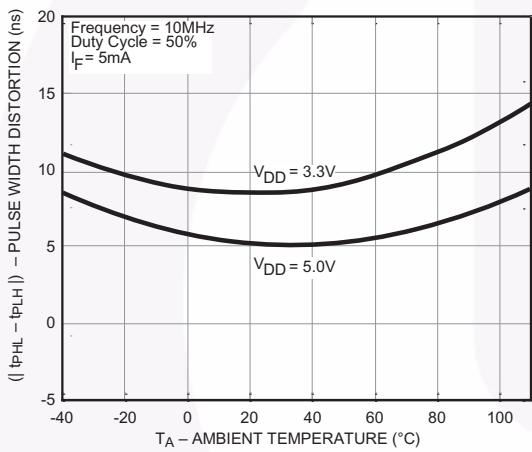
**Fig 7. Propagation Delay vs. Ambient Temperature**



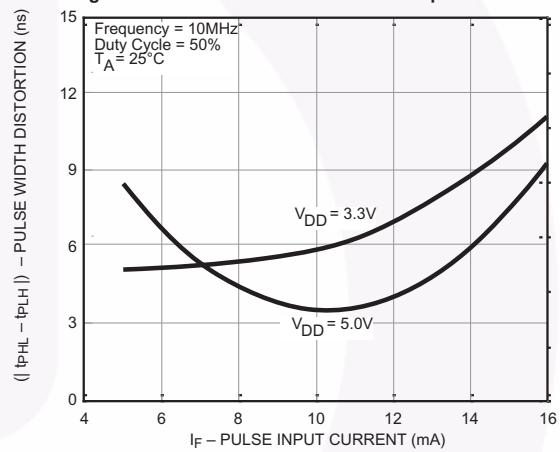
**Fig 8. Propagation Delay vs. Pulse Input Current**



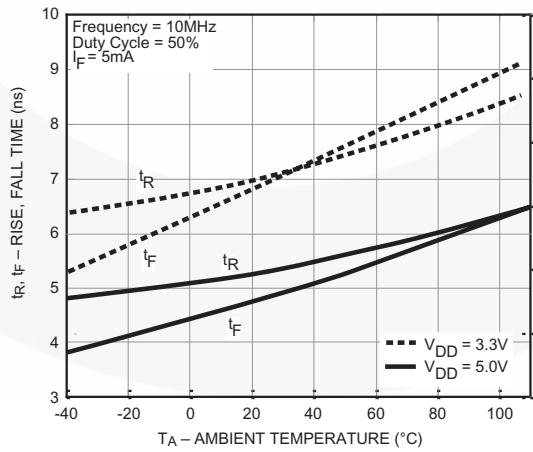
**Fig 9. Pulse Width Distortion vs. Ambient Temperature**



**Fig 10. Pulse Width Distortion vs Pulse Input Current**



**Fig 11. Rise and Fall Time vs. Ambient Temperature**



## Schematics

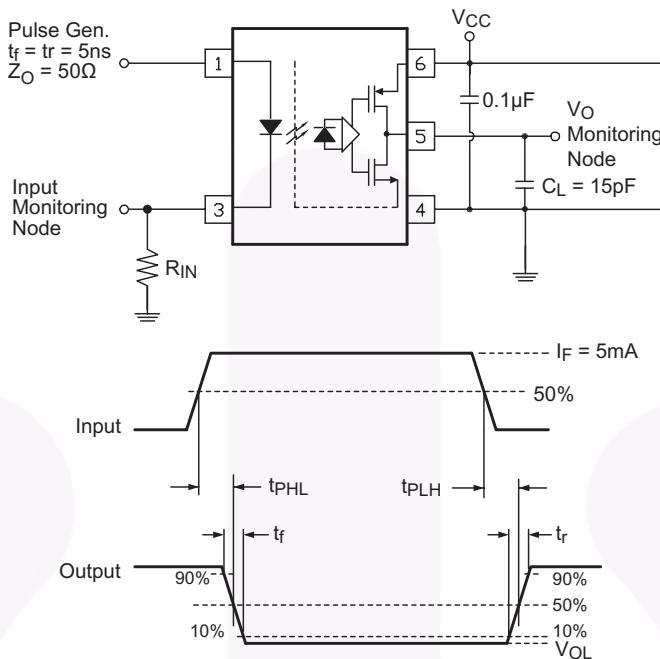


Figure 12. Test Circuit for Propagation Delay Time, Rise Time and Fall Time

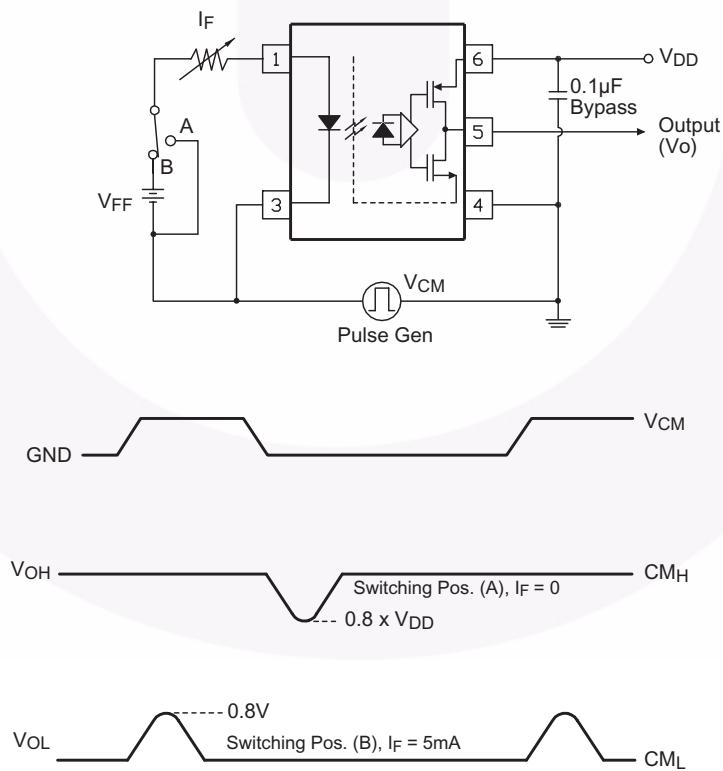
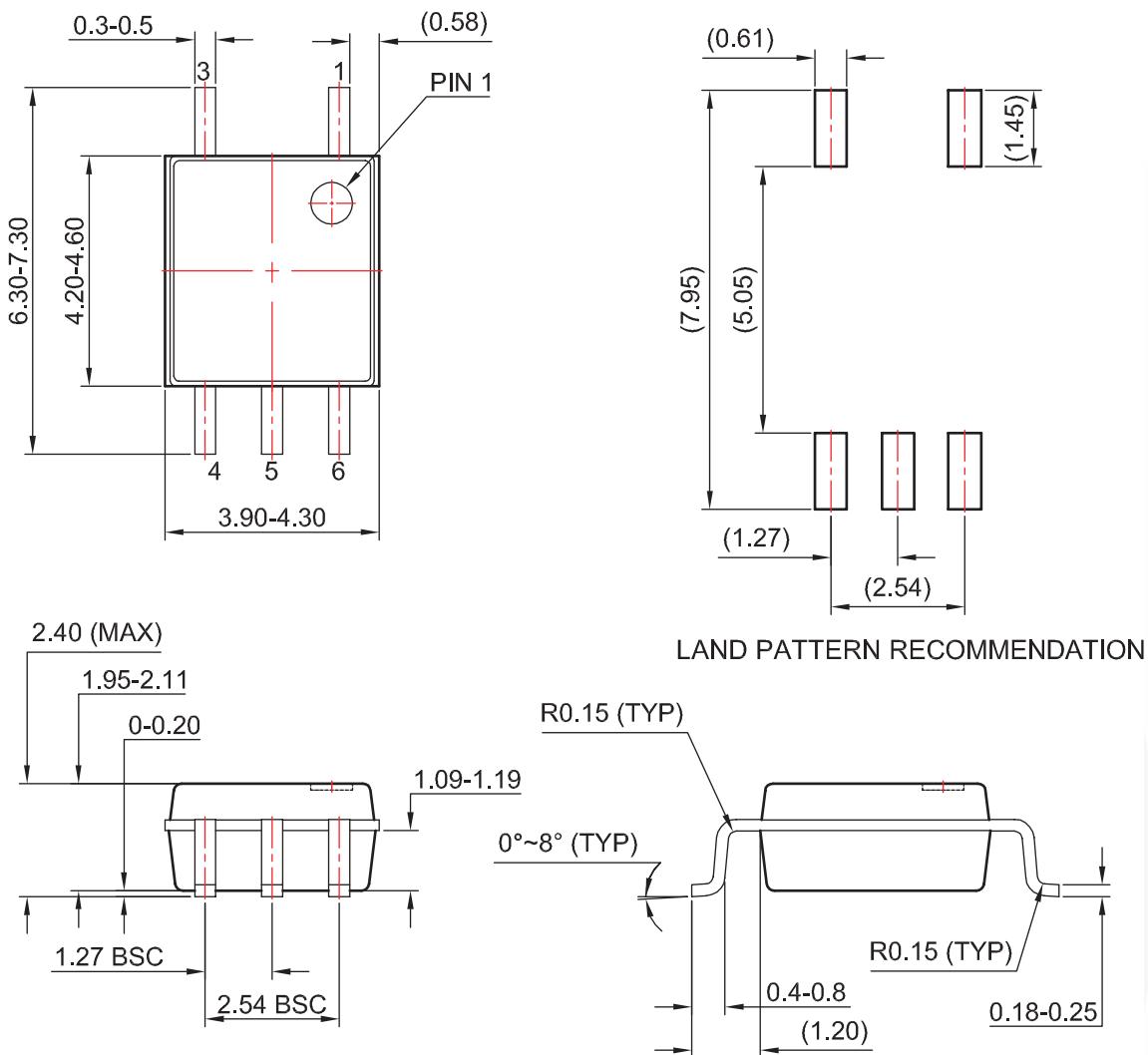


Figure 13. Test Circuit for Instantaneous Common Mode Rejection Voltage

## Package Dimensions



### Notes:

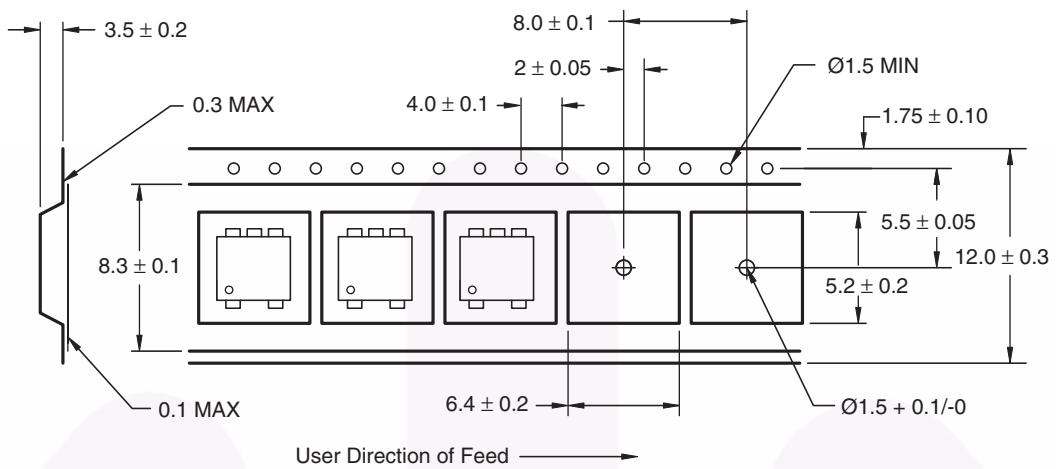
1. No standard applies to this package.
2. All dimensions are in millimeters.
3. Dimensions are exclusive of burrs, mold flash, and tie bar extrusion.
4. Drawings file name and revision: MKT-MFP05A.

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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## Carrier Tape Specification



**Note:**

All dimensions are in millimeters.

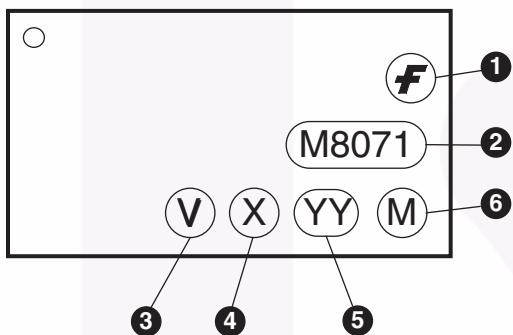
## Ordering Information

Option	Order Entry Identifier	Description
No Suffix	FODM8071	Mini-Flat 5-pin, shipped in tubes (100 units per tube)
R2	FODM8071R2	Mini-Flat 5-pin, tape and reel (2,500 units per reel)



All packages are lead free per JEDEC: J-STD-020B standard.

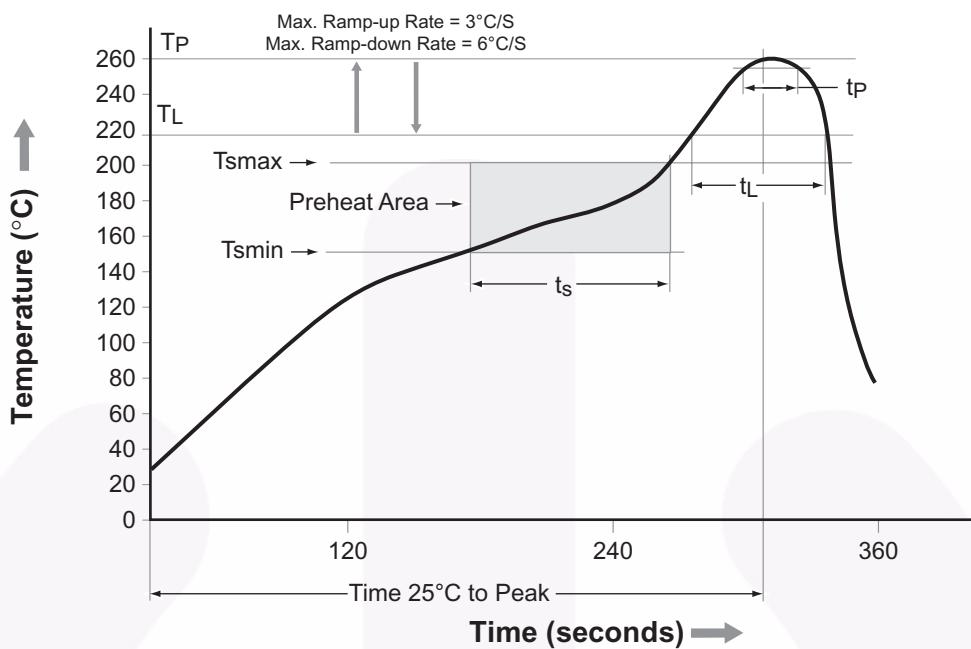
## Marking Information



### Definitions

1	Fairchild logo
2	Device number
3	IEC60747-5-2 (VDE marking)
4	One digit year code, e.g., '9'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

## Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (t <sub>S</sub> ) from (Tsmin to Tsmax)	60–120 seconds
Ramp-up Rate (t <sub>L</sub> to t <sub>P</sub> )	3°C/second max.
Liquidous Temperature (T <sub>L</sub> )	217°C
Time (t <sub>L</sub> ) Maintained Above (T <sub>L</sub> )	60–150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (t <sub>P</sub> ) within 5°C of 260°C	30 seconds
Ramp-down Rate (T <sub>P</sub> to T <sub>L</sub> )	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.



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## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I45