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WM9715-6123-FL48-M-REV1

Example Configurations

DOC TYPE:	EXAMPLE CONFIGURATIONS
BOARD REFERENCE:	WM9715-6123-FL48-M-REV1
BOARD TYPE:	Customer Mini Board
WOLFSON DEVICE(S):	WM9715
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INTRODUCTION

The WM9715-6123-FL48-M-REV1 customer mini board is compatible with the 6123-EV1-REV2 customer main board and together provide a complete hardware platform for evaluation of the WM9715. The WM9715 customer mini board can also be used independently and connected directly to a processor board using flying field wires or appropriate headers. This document will cover both, but performance data will be based on the Wolfson system with the 6123-EV1-REV2 main board.

Configurations covered are listed below:

- DAC to Headphone playback
- LINEINL/R to ADC recording
- LINEINL/R to Headphone playback (analogue bypass)

This document should be used as a starting point for evaluation of WM9715 but it will not cover every possible configuration.

Assumptions:

1. The user is familiar with the 6123-EV1-REV2 main board and that the board is correctly configured for the path of interest (see related documents below)
2. The user has control of the WM9715 register settings, for example by installing Wolfson WISCE software.

Related documents:

1. WM9715 datasheet
2. WM9715-6123-FL48-M-REV1 Schematic and Layout.pdf
3. 6123-EV1-REV2 Schematic and Layout.pdf
4. WISCE Quick Start Guide.pdf

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BOARD CONFIGURATION STAND-ALONE

The WM9715 Customer Mini Board can be used a stand-alone module for direct connection to a processor board via flying leads or dedicated headers. This section will detail important considerations and provide all information required to do this without risking damage to the device.

CONNECTION DIAGRAM

Figure 1 below shows the connections required to power-up and control the WM9715 Customer Mini Board.

Please refer to the Table 1 for further detail on external I/O connections.

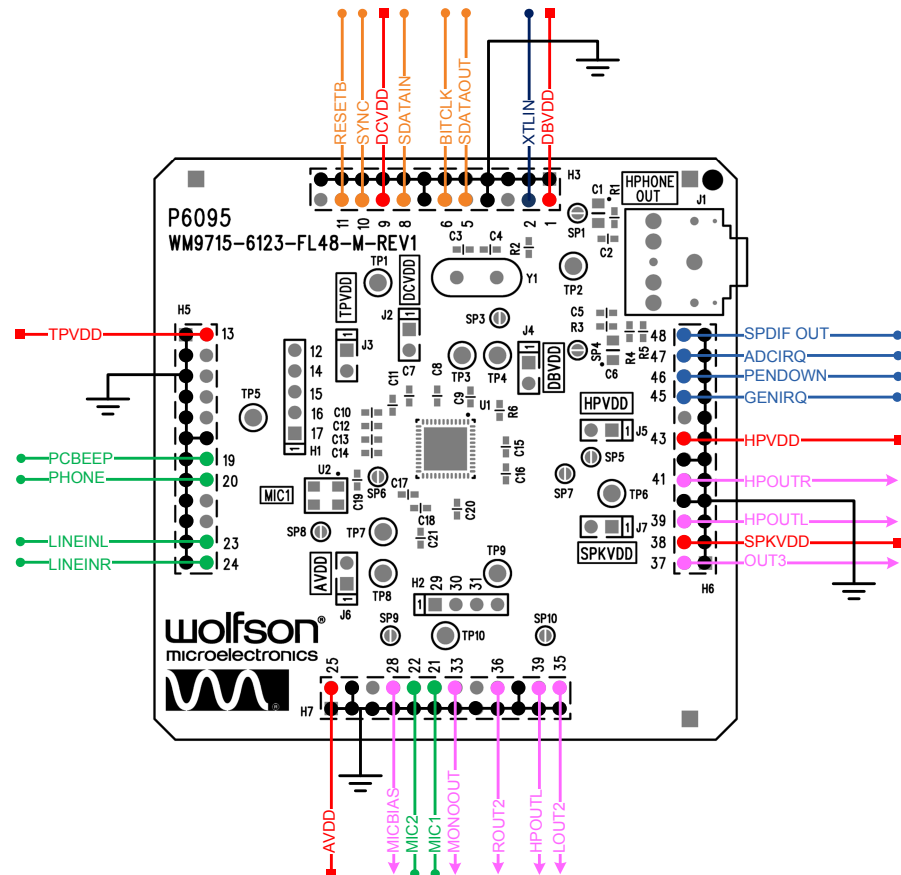


Figure 1 Stand-Alone Board Configuration

I/O TABLE

SIGNAL	BOARD REFERENCE	IMPORTANT NOTES
Voltage Supplies		
AVDD	H7: pin 2	1.8V to 3.6V (Additional restrictions apply. Please refer to the datasheet)
TPVDD	H5: pin 2	
HPVDD	H6: pin 14	
SPKVDD	H6: pin 4	
DCVDD	H3: pin 18	
DBVDD	H3: pin 2	
Ground		
AGND	Common Ground	Analogue and digital grounds must always be within 0.3V of each other
TPGND		
HPGND		
SPKGND		
DCGND		
DBGND		
AC-LINK Interface		
SDATAOUT	H3: pin 10	Signals should swing between DGND and DBVDD
BITCLK	H3: pin 12	
SDATAIN	H3: pin 16	
SYNC	H3: pin 20	
RESETB	H3: pin 22	
Master Clock		
XTLIN	H3: pin 4	Master clock connects to XTLIN pin. Signal should swing between DGND and DBVDD
Digital I/O		
GENIRQ	H6: pin 18	When used as inputs signals should swing between DGND and DBVDD
PENDOWN	H6: pin 20	
ADCIRQ	H6: pin 22	
SPDIF OUT	H6: pin 24	
Analogue Inputs		
MIC1	H7: pin 12	AGND to AVDD
MIC2	H7: pin10	
PCBEEP	H5: pin 14	
PHONE	H5: pin 16	
LINEINL	H5: pin 22	
LINEINR	H5: pin 24	
Analogue Outputs		
OUT3	H6: pin 2	Analogue Outputs
HPOUTL	H6: pin 6 H7: pin 22	
HPOUTR	H6: pin 10	
LOUT2	H7: pin 24	
HPOUTL	H7: pin 22	
ROUT2	H7: pin 18	
MONOOUT	H7: pin 14	
MICBIAS	H7: pin 8	Analogue microphone bias voltage output
5-Wire Touch Interface		
Y-	H1: pin 1	AGND to AVDD
X-	H1: pin 2	
Y+	H1: pin 3	
X+	H1: pin 4	
WIPER	H1: pin 5	

Battery Monitor / AUXADC Connector		
COMP1/AUX1	H2: pin 1	AGND to AVDD
COMP2/AUX2	H2: pin 2	
BMON/AUX3	H2: pin 3	See datasheet for voltage restrictions

Table 1 I/O Configuration

SHORTING POINTS AND JUMPER LINKS TABLE

REFERENCE	FUNCTION	
SP1	Short SP1 and SP4, remove R4 and populate R5 to use capless headphone mode.	
SP4		
SP3	Short SP3 and remove R2 to use crystal as clock source.	
SP5	Short SP5 and SP7 and remove C1 and C6 to use headphone circuitry on mainboard.	
SP7		
SP6	Short SP6 and SP8 and ensure SP9 in open to use onboard silicon microphone.	
SP8		
SP9	Short SP9 to use analogue microphone on the mainboard.	
SP10	Short SP10 to use HPOUTL and OUT3 as second differential pair on the mainboard.	
J2	DCVDD	These jumpers link the relevant pins on the DUT to the different supply voltages. To supply different voltages disconnect the relevant jumper link and apply the chosen voltage directly to pin 2 of the relevant jumper.
J3	TPVDD	
J4	DBVDD	
J5	HPVDD	
J6	AVDD	
J7	SPKVDD	

Table 2 Shorting Points and Jumper Links Table

BOARD CONFIGURATION WITH 6123-EV1-REV2 MAIN BOARD

This section focuses on evaluation of the WM9715-6123-FL48-M-REV1 Customer Mini Board in combination with the 6123-EV1-REV2 main board. This system is the reference platform for measurement data contained in this document. Please note that only a limited number of usage modes will be covered.

DAC TO HEADPHONE PLAYBACK

The following section details the configuration for DAC to headphone playback through HPOUTL/R. For board configuration, please refer to Figure 3

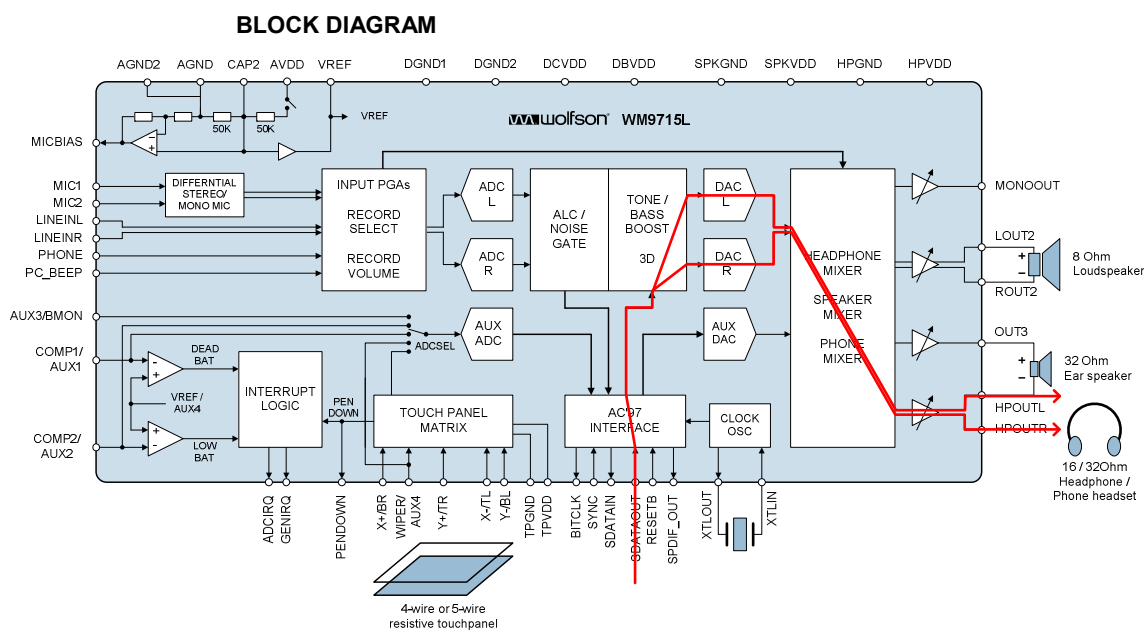


Figure 2 Path Diagram for DAC to HPOUTL/R

BOARD CONFIGURATION

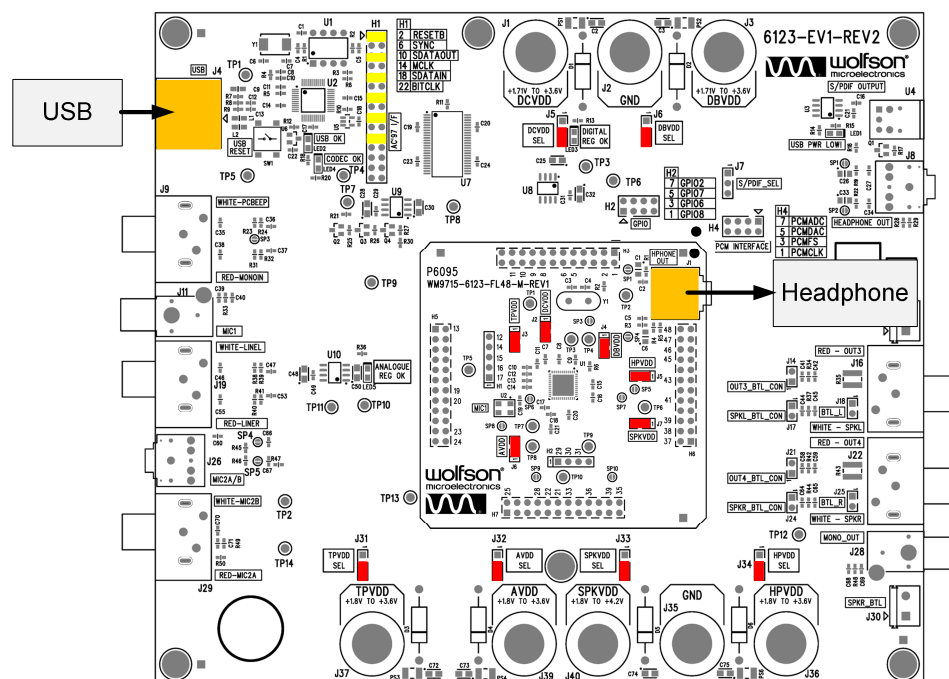


Figure 3 Board Configuration for DAC to HPOUTL/R

REGISTER SETTINGS

Register settings provided below are the typical sequence to configure the desired path and have not been optimised for pop suppression.

REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	Software Reset
0x04	0x0080	Set headphone volume to 0dB and unmute.
0x18	0x6808	Unmute DAC to HPMIX path.
0x26	0x0100	Enable HP out, AC link, Vref, Analogue mixers and Stereo DAC

Table 3 Register Settings for DAC to Headphone

LINEINL/R TO ADC RECORDING

The following section details the configuration for LINEINL/R to ADC recording. For board configuration, please refer to Figure 5.

BLOCK DIAGRAM

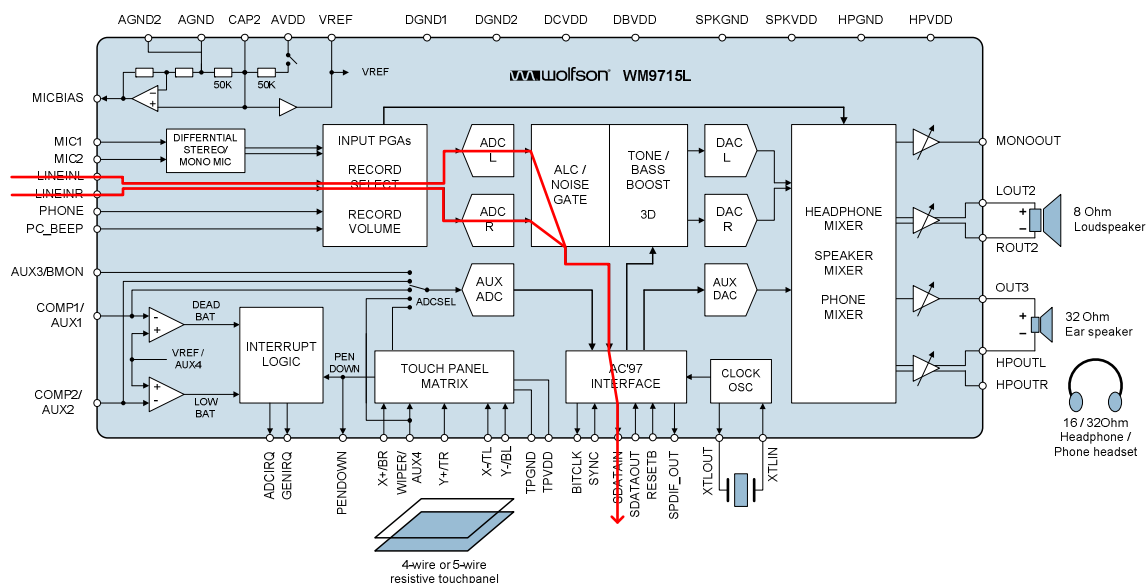


Figure 4 Path Diagram for LINEINL/R to ADC

BOARD CONFIGURATION

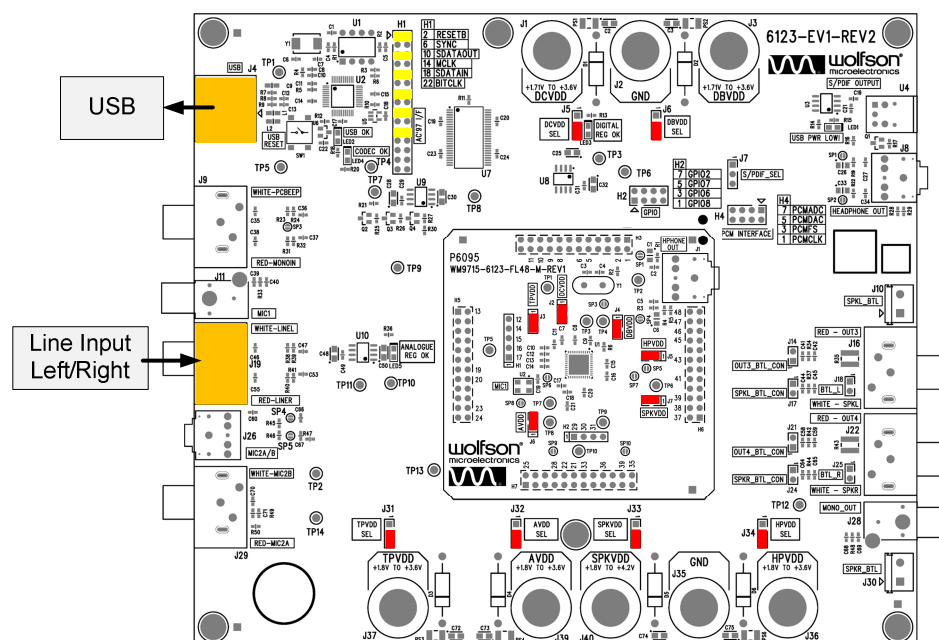


Figure 5 Board Configuration for LINEINL/R to ADC

REGISTER SETTINGS

Register settings provided below are simply the minimum requirement to configure the desired path and have not been optimised for pop suppression.

REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	Software Reset
0x1A	0x3404	Select LINEINL/R as record source
0x1C	0x0000	Unmute record volume
0x26	0xC20D	Enable internal clock, AC-link, Vref, Analogue mixers and ADCs

Table 4 Register Settings for LINEINL/R to ADC

LINEINL/R TO HEADPHONE PLAYBACK (BYPASS)

The following section details the configuration for headphone playback from line input, bypassing the ADCs and DACs. For board configuration, please refer to Figure 5.

BLOCK DIAGRAM

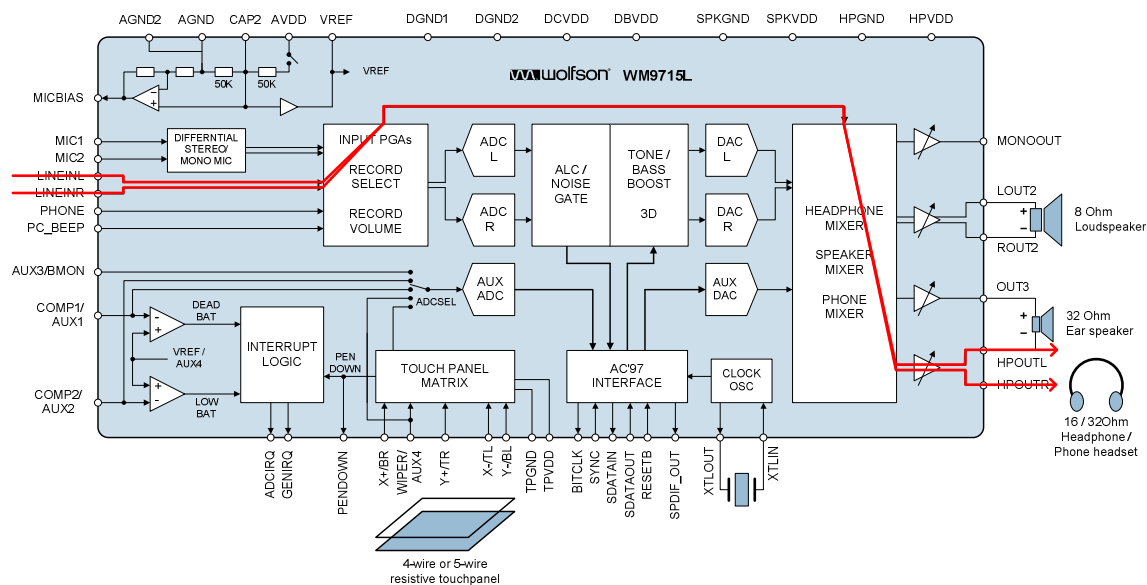


Figure 6 Path Diagram for LINEINL/R to Headphone (bypass)

BOARD CONFIGURATION

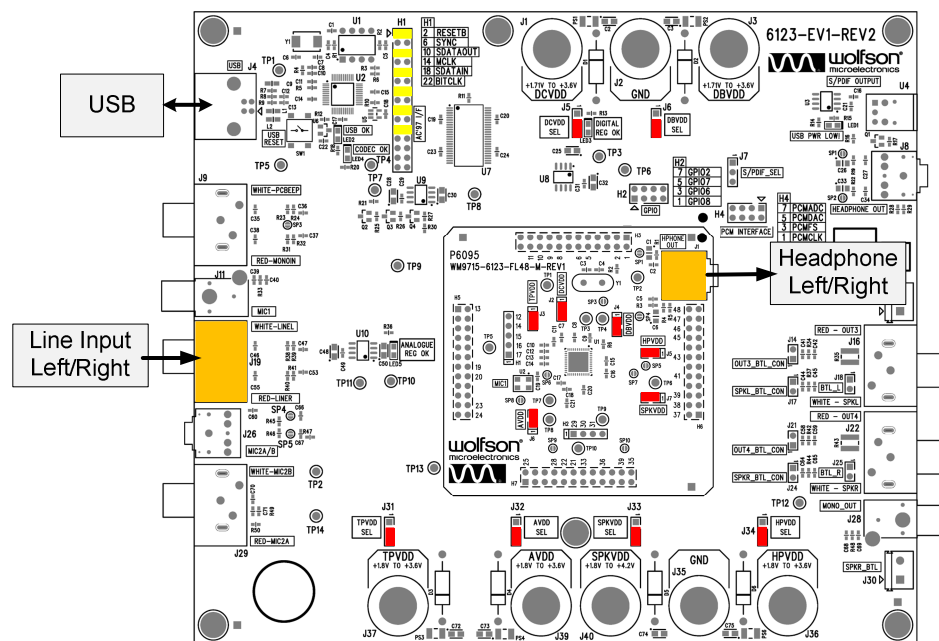


Figure 7 Board Configuration for LINEINL/R to Headphone (bypass)

REGISTER SETTINGS

Register settings provided below are the typical sequence to configure the desired path and have not been optimised for pop suppression.

REG INDEX	DATA VALUE	COMMENT
0x00	0x0000	Software Reset
0x04	0x0080	Set headphone volume to 0dB and unmute.
0x10	0x6808	Unmute line-in to headphone path
0x26	0xA30C	Enable headphones, AC-Link, Vref and Analogue mixers

Table 5 Register Settings for LINEINL/R to Headphone (bypass)

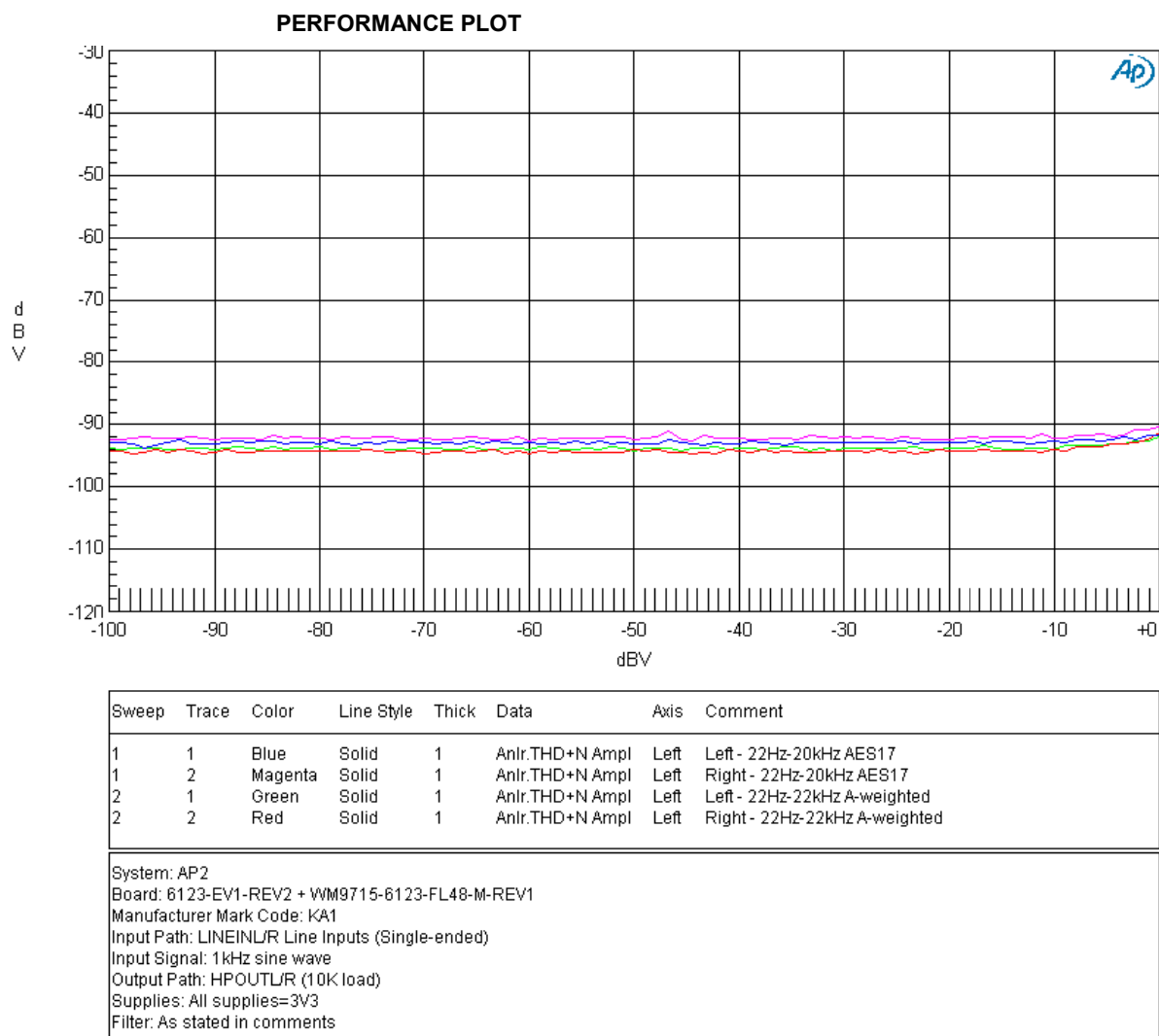


Figure 8 Performance Plot for LINEINL/R to Headphone (bypass)

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