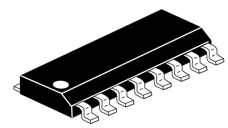
The MRFIC Line
900 MHz TX-Mixer/Exciter

MRFIC2101

The MRFIC2101 is a high linearity transmit mixer and exciter designed primarily for Digital Cellular radio systems. The mixer is double-balanced for excellent LO and spurious rejection. An on-board LO buffer is provided to reduce LO power requirements and eliminate the need for an external LO balun. A power down control is provided to minimize current drain with minimum recovery/turn-on time. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device.

- High Linearity $IP3_0$ = 23 dBm (Typ)
- Low LO Drive Required = –15 dBm (Typ)
- Externally Adjustable Exciter Bias Current
- Power Down Supply Current = 2.0 µA (Typ)
- SO-16 Narrow Body Plastic Package
- Order MRFIC2101R2 for Tape and Reel.
  R2 suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M2101

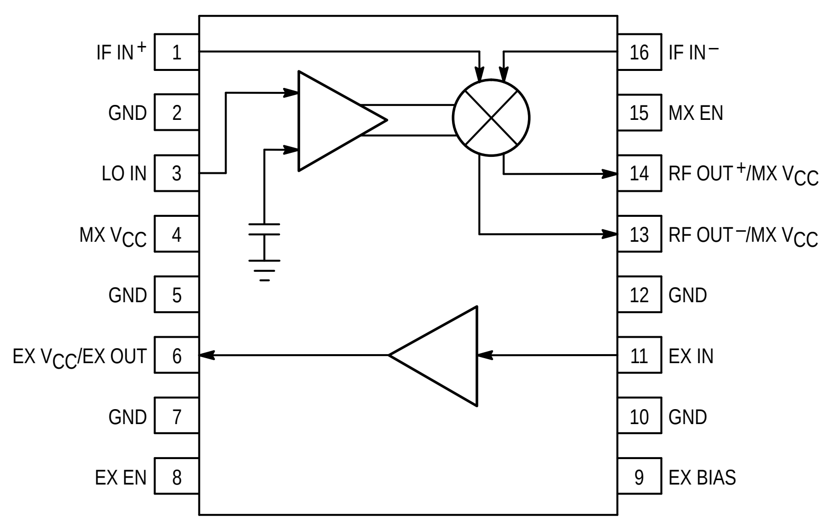
**900 MHz
TX-MIXER/EXCITER
SILICON MONOLITHIC
INTEGRATED CIRCUIT**



**CASE 751B-05
(SO-16)**

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Ratings	Symbol	Value	Unit
Supply Voltage	EX V_{CC}, MX V_{CC}, EX BIAS	5	Vdc
Enable Voltages	MX EN, EX EN	6	Vdc
Input Power, LO and IF Ports	P_{LO}, P_{IF}	+10	dBm
Operating Ambient Temperature	T_A	– 35 to + 85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C
RF Output Power (EX V_{CC} < 4 V)	P_{out}	18	dBm
RF Output Power (4 V< EX V_{CC} ≤ 5 V)	P_{out}	38 – 5 EX V_{CC}	dBm



Pin Connections and Functional Block Diagram

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltages	EX V_{CC}, MX V_{CC}, EX BIAS	4.75	Vdc
Enable Voltages	MX EN, EX EN	0, 4.75	Vdc
RF Port Frequency Range	RF	800 to 1000	MHz
IF Port Frequency Range	IF	0 to 250	MHz

LOGIC LEVELS (T_A = 25°C)

Input Voltage (MX EN, EX EN)	Min	Max	Unit
High	MX V_{CC} –0.8, EX V_{CC} –0.8	—	Volts
Low	—	0.8	Volts

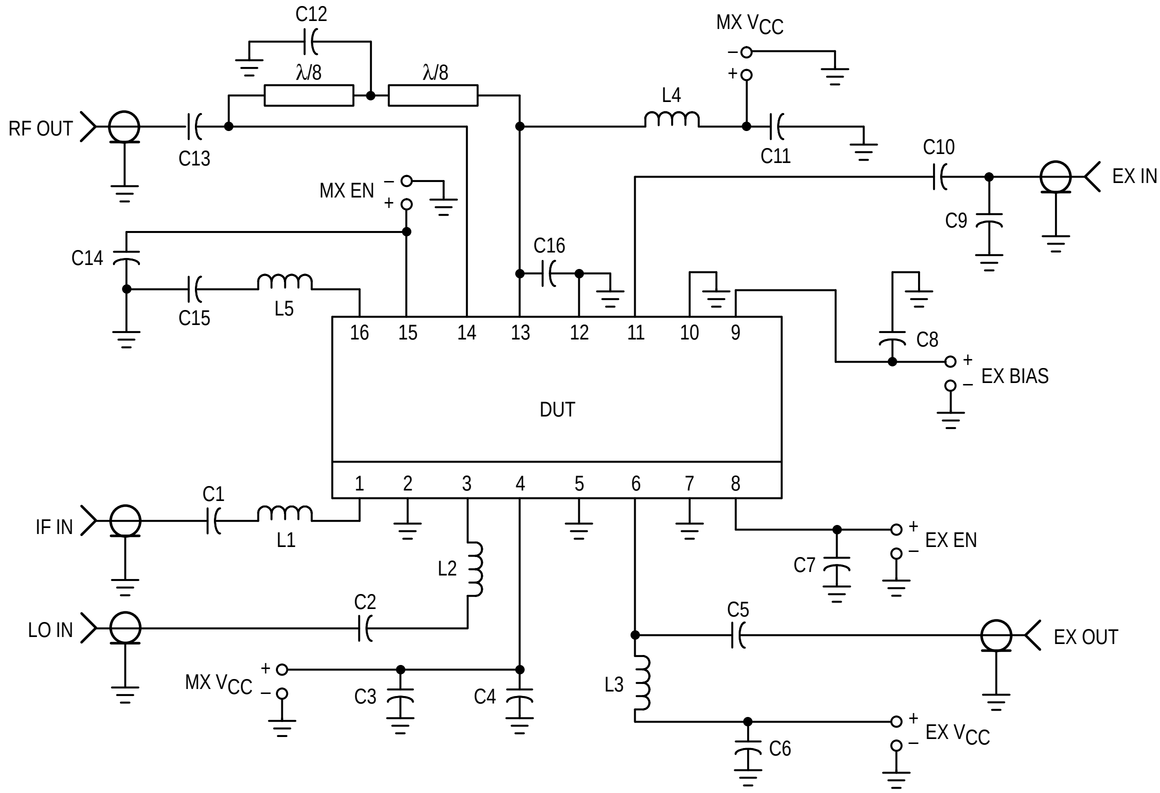
MIXER ELECTRICAL CHARACTERISTICS (MX V_{CC}, MX EN = 4.75 V, T_A = 25°C, RF @ 900 MHz, LO @ 800 MHz, IF @ 100 MHz, P_{LO} = –15 dBm unless otherwise noted)

Characteristic (1)	Min	Typ	Max	Unit
Conversion Gain (Small Signal)	24	26.5	29	dB
Output Power at 1 dB Gain Compression	2.5	4.5	—	dBm
Output Third Order Intercept Point (– 5 dBm out/tone)	—	14	—	dBm
Output Fifth Order Intercept Point (– 5 dBm out/tone)	—	11	—	dBm
LO Leakage	—	– 30	—	dBm
Supply Current (Enabled)	—	45	54	mA
Supply Current (Disabled)	—	1	—	µA
Noise Figure (Single Sideband)	—	5	—	dB

EXCITER ELECTRICAL CHARACTERISTICS (EX V_{CC}, EX EN, EX BIAS = 4.75 V, T_A = 25°C, RF @ 900 MHz unless otherwise noted)

Characteristic (1)	Min	Typ	Max	Unit
Gain (Small Signal)	14	16	18	dB
Output Power at 1 dB Gain Compression	16	18	—	dBm
Output Third Order Intercept Point (+ 3 dBm out/tone)	—	30	—	dBm
Output Fifth Order Intercept Point (+ 3 dBm out/tone)	—	22	—	dBm
LO Leakage (P_{LO} = –15 dBm into Mixer)	—	– 30	—	dBm
Supply Current (Enabled)	—	38	46	mA
Supply Current (Disabled)	—	1	—	µA
Noise Figure	—	5	—	dB

(1) All electrical characteristics are measured in test circuit schematic as shown in Figure 1.



C1, C2, C3,	1000 pF, Chip Capacitor	L1, L5	82 nH, Chip Inductor
C4	100 pF, Chip Capacitor	L2	15 nH, Chip Inductor
C5, C6, C7	1000 pF, Chip Capacitor	L3	8.2 nH, Chip Inductor
C8, C10, C11	1000 pF, Chip Capacitor	L4	12 nH, Chip Inductor
C9, C12	5.6 pF, Chip Capacitor	RF Connectors	SMA Type
C13, C16	2.7 pF, Chip Capacitor	Board Material	0.031″ Thick FR4, 0.5 oz. Copper,
C14, C15	1000 pF, Chip Capacitor		ε_r = 4.45, Coplanar Waveguide

Figure 1. Test Circuit Configuration

Table 1. Mixer Deembedded Port Reflection Coefficients
(Z_O = 50 Ω, T_A = 25°C)

f (MHz)	Γ_{IF}		Γ_{RF}		Γ_{LO}	
	Mag	∠φ Degrees	Mag	∠φ Degrees	Mag	∠φ Degrees
50	0.68	– 9.4	—	—	—	—
100	0.68	– 18	—	—	—	—
150	0.67	– 26	—	—	—	—
200	0.66	– 33	—	—	—	—
250	0.65	– 40	—	—	—	—
500	—	—	0.93	– 28	0.79	– 30
600	—	—	0.92	– 33	0.79	– 32
700	—	—	0.91	– 37	0.79	– 33
800	—	—	0.89	– 41	0.77	– 34
900	—	—	0.87	– 45	0.75	– 34
1000	—	—	0.85	– 48	0.73	– 35
1100	—	—	0.82	– 50	0.69	– 36
1200	—	—	0.79	– 53	0.65	– 37
1300	—	—	0.75	– 56	0.61	– 41
1400	—	—	0.71	– 61	0.56	– 47
1500	—	—	0.66	– 66	0.52	– 55

Table 2. Exciter Small Signal Deembedded S Parameters
(Z_O = 50 Ω, T_A = 25°C)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠φ	$\|S_{21}\|$	∠φ	$\|S_{12}\|$	∠φ	$\|S_{22}\|$	∠φ
100	0.51	–121	35.51	131	0.02	50	0.65	–67
200	0.62	–149	22.61	109	0.03	42	0.49	–103
300	0.65	–162	16.05	96	0.03	41	0.43	–122
400	0.65	–170	12.16	87	0.04	41	0.40	–134
500	0.63	–177	9.75	81	0.04	42	0.38	–141
600	0.61	176	8.18	75	0.05	41	0.37	–146
700	0.59	169	7.06	70	0.05	40	0.36	–149
800	0.58	161	6.18	65	0.06	38	0.35	–153
900	0.58	154	5.44	60	0.07	33	0.35	–156
1000	0.59	145	4.91	55	0.07	30	0.35	–163
1100	0.61	139	4.39	51	0.08	27	0.35	–170
1200	0.65	134	3.94	47	0.08	22	0.35	–177
1300	0.67	131	3.56	43	0.08	20	0.37	174
1400	0.69	129	3.22	39	0.09	16	0.40	166
1500	0.71	127	2.92	36	0.09	13	0.43	160

TYPICAL CHARACTERISTICS

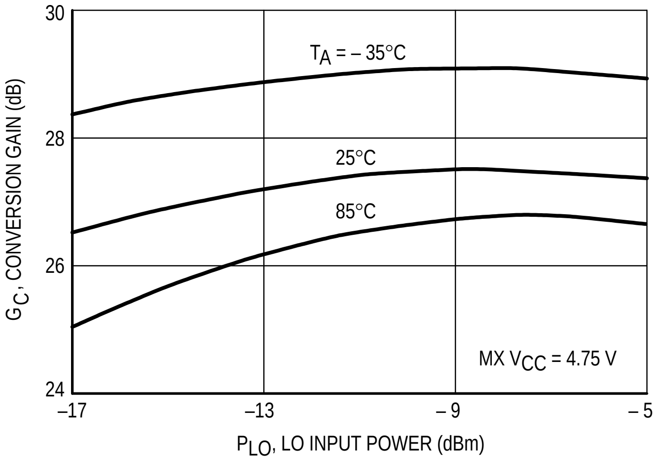


Figure 2. Mixer Gain versus LO Input Power

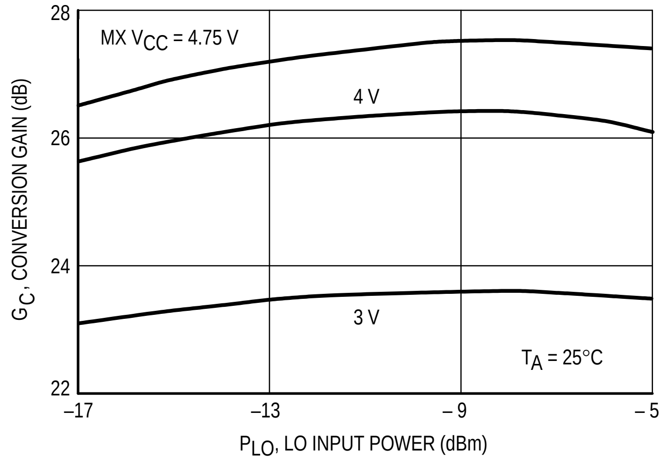


Figure 3. Mixer Gain versus LO Input Power

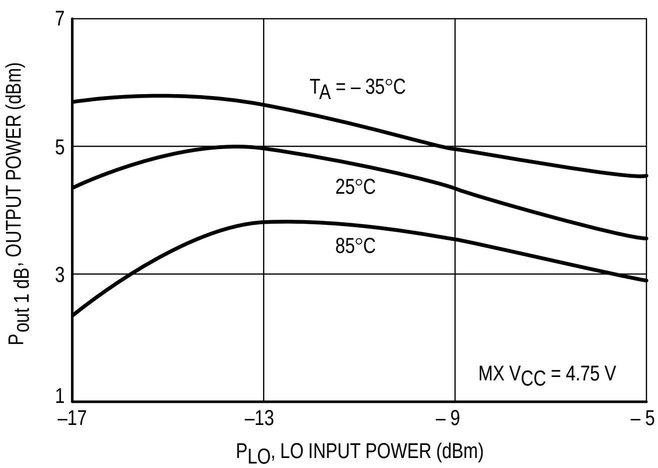


Figure 4. Mixer Output Power at 1 dB Gain Compression versus LO Input Power

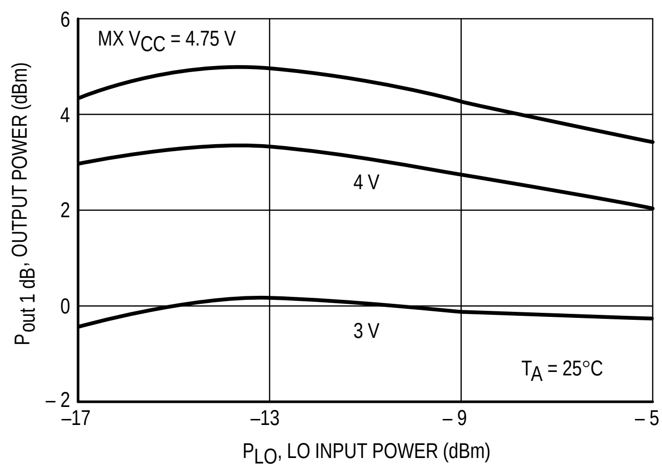


Figure 5. Mixer Output Power at 1 dB Gain Compression versus LO Input Power

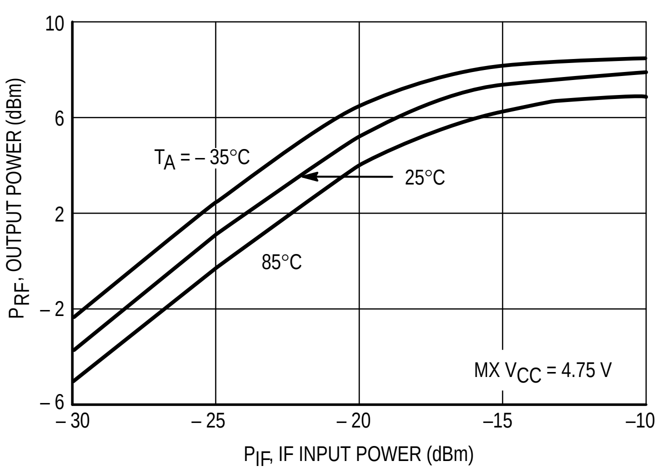


Figure 6. Mixer Output Power versus IF Input Power

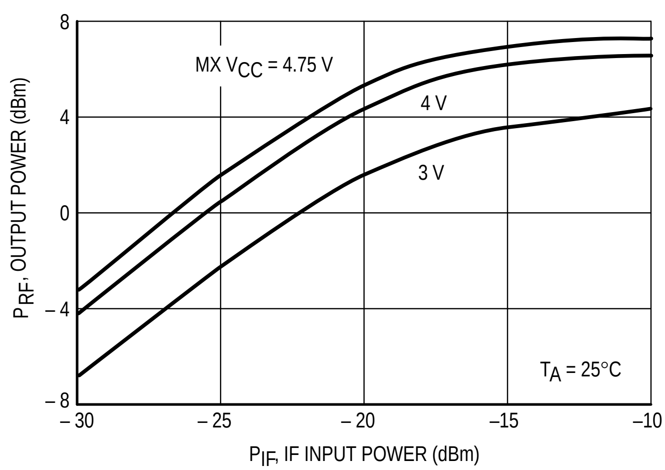


Figure 7. Mixer Output Power versus IF Input Power

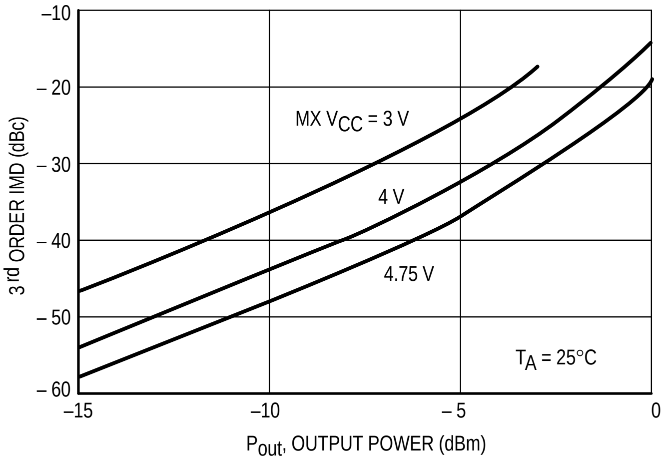


Figure 8. Mixer 3rd Order Intermodulation Distortion versus Output Power

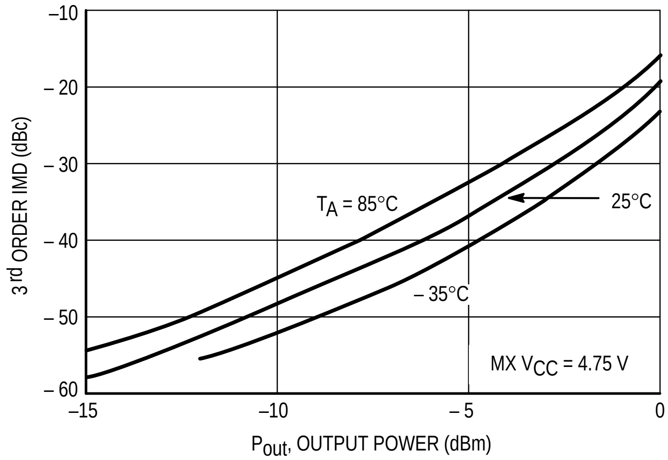


Figure 9. Mixer 3rd Order Intermodulation Distortion versus Output Power

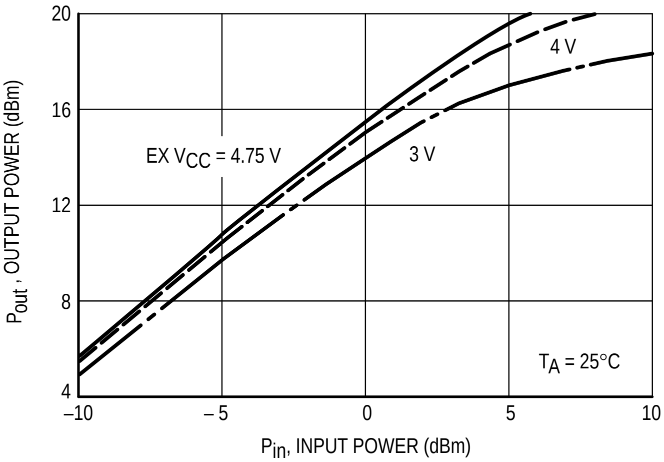


Figure 10. Exciter Output Power versus Input Power

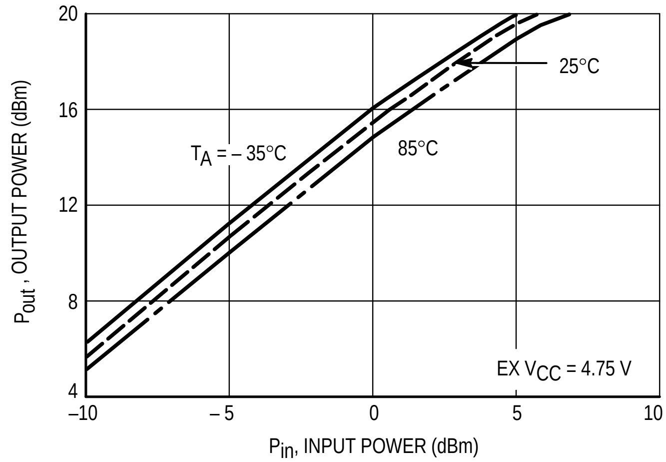


Figure 11. Exciter Output Power versus Input Power

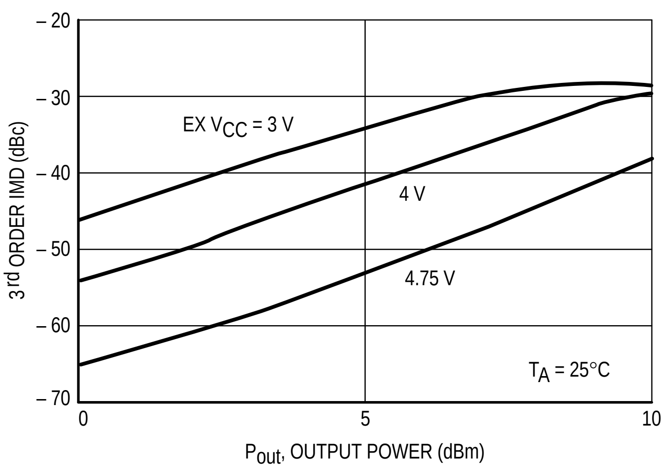


Figure 12. Exciter 3rd Order Intermodulation Distortion versus Output Power

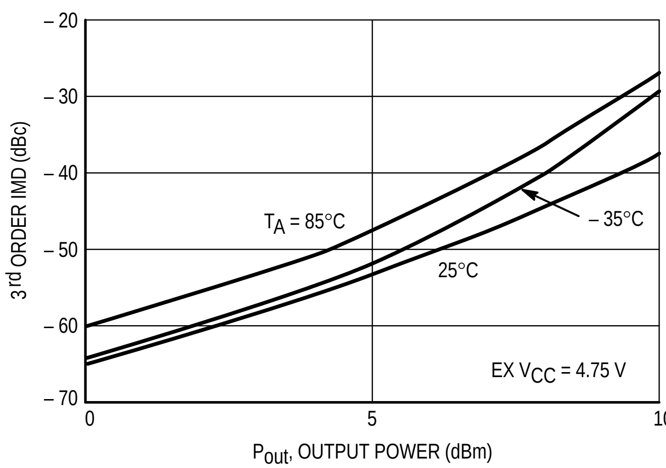


Figure 13. Exciter 3rd Order Intermodulation Distortion versus Output Power

TYPICAL CHARACTERISTICS

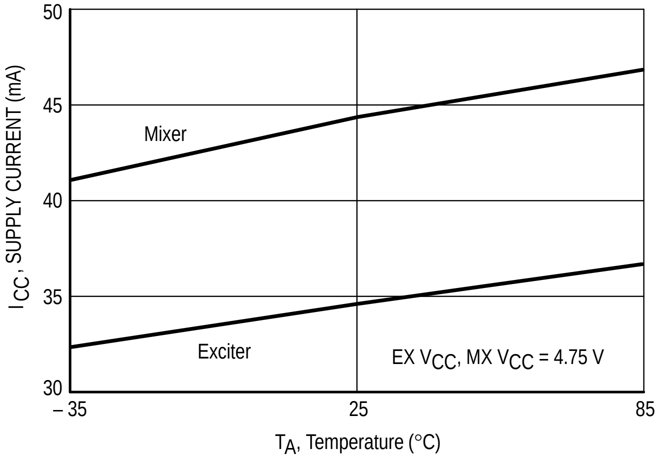


Figure 14. I_{CC} versus Temperature

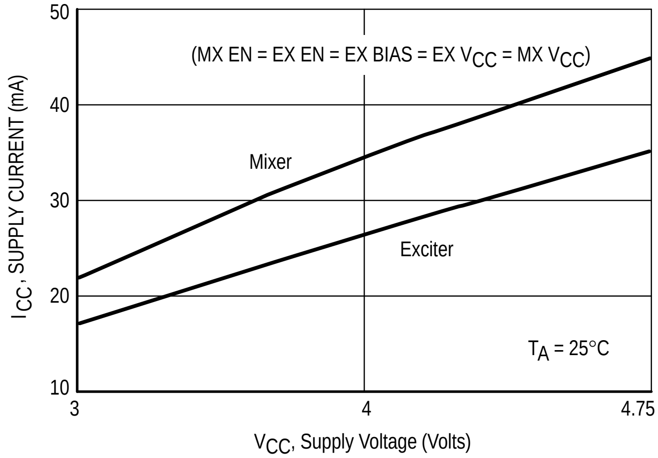


Figure 15. I_{CC} versus V_{CC}

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2101 was designed as a linear upconverter for U.S. and Japan digital cellular radios. However, it is versatile enough to be used in other applications such as analog cellular, GSM, CDMA and the 900 MHz ISM band.

The mixer is double-balanced to minimize spurious and LO emission. An external balun is required on the mixer RF output to maximize linearity and maintain good balance. An inexpensive and easy to implement balun is described below in the theory of operation. The IF and LO ports do not require baluns. The LO split is achieved on-chip with a buffer amplifier which also reduces the LO power requirement. The IF port can be driven differentially or single-ended with a decoupling capacitor on the unused IF input. Baseband signals can be applied directly to the IF inputs and the device becomes a complete low–power transmitter.

To maximize efficiency in various systems, the exciter bias current is externally adjustable. The bias current can also be ramped to reduce spectral splatter.

To minimize current drain in TDD/TDMA systems, the MRFIC2101 has separate TTL/CMOS compatible enable pins for the mixer and the exciter.

THEORY OF OPERATION

Matching the LO port to 50 ohms can be done several ways. The recommended approach is a series inductor as close to the IC as possible. The inductor value is small enough (~8 – 15 nH depending on LO frequency and distance from the IC) to be printed on the board. A DC block is required and should not be placed between the inductor and IC since the added electrical length will cause a poor match.

The IF ports are approximately 250 ohms resistive in parallel with 5.0 pF of capacitance. Matching directly into this impedance is not recommended. Series 82 nH chip inductors should first be placed as close to both IF ports as possible. This presents a high impedance to the IF ports at the LO frequency which substantially reduces the LO leakage out of the RF port. The resulting impedance then may be matched to the desired characteristic impedance. DC blocking capacitors are also required.

Both RF ports are approximately 25 ohms resistive in series with 1.5 pF of capacitance (or the parallel equivalent, 380 ohms in parallel with 1.9 pF). Best linearity is achieved by loading each port with 100 ohms resistive and resonating the 1.9 pF. Ideally, a half wavelength transmission line could be used to combine the two differential RF ports into one; however, the size of such a line would be very large. Any number of balun type network can be employed so long as the network presents 100 ohms to each port, resonates 1.9 pF capacitance at each port, and exhibits 180 degree phase difference between the two ports. The network shown in Figure 1 combines very well without a lot of added board space or complexity. Essentially, a quarter wavelength of transmission line (~1.5 inches of 50 ohms stripline in FR4) is used with additional phase shift coming from capacitors C12, C13 and C16. This network will operate anywhere from 800–1000 MHz by adjusting bias inductor L4 and C16 only.

The exciter input requires external matching and a DC block. It is best matched to 50 ohms using a short 50 ohms transmission line followed by a 5–10 pF shunt capacitor. The exciter output is approximately 50 ohms resistive in parallel with 4 pF of capacitance in the 800–1000 MHz range. It is best matched to 50 ohms using a 6–10 nH bias inductor placed as close to the IC as possible. The exciter is conditionally stable. Placing a 100-300 ohm resistor in parallel with the bias inductor, when driving large VSWR loads, may be needed to keep the exciter stable.

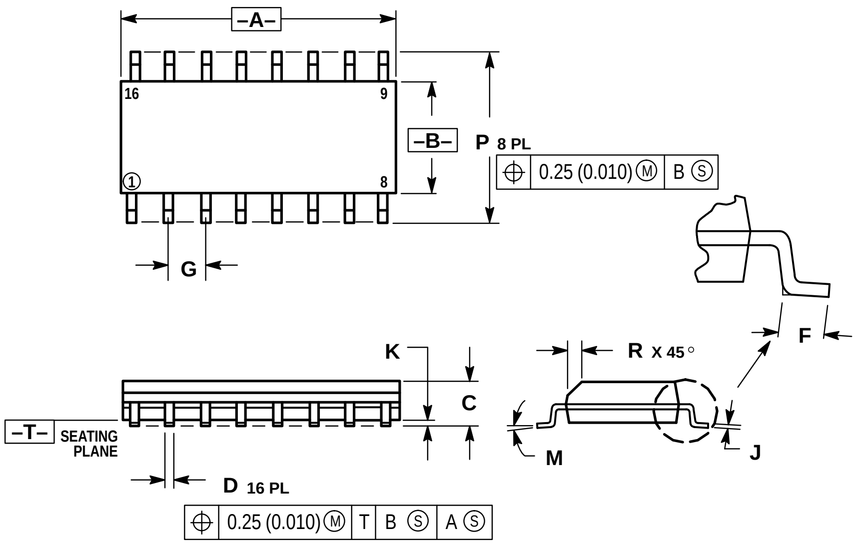
Supply decoupling must be done as close to the IC as possible. A 1000 pF capacitor is recommended. An additional 100 pF capacitor and an RF choke are recommended to keep the LO signal off the supply line.

Enabling/Disabling the MRFIC2101 can be done with the separate TTL/CMOS compatible enable pins for the mixer and exciter. The trip point is between 1 and 2 volts.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

CASE 751B–05
ISSUE J

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