

3.3V, 7-Channel Analog Video Switch

Features

- Designed specifically to switch VGA signals
- 7-Channels for VGA signals (R,G,B, Hsync, Vsync, DDC Data, and DDC CLK)
- $V_{DD} = 3.3V \pm 10\%$
- DDC path will operate as a 5V to 3.3V level shifter
- H/V output buffer with $\pm 24mA$ drive
- ESD tolerance on video I/O pins is up to 12kV HBM per JEDEC standard
- -3dB BW of 1.7GHz (typ)
- Low Xtalk, (-38dB typ)
- Low and Flat ON-STATE resistance ($R_{on} = 4.8\text{-Ohm}$, $R_{on}(\text{Flat}) = 0.5\text{ohm}$, typ)
- Low input/output capacitance ($C_{on} = 5.6\text{pF}$, typ)
- Packaging (Pb-free and Green):
 - 32-contact TQFN (ZLE)

Applications

- Routes physical layer signals for high bandwidth digital video

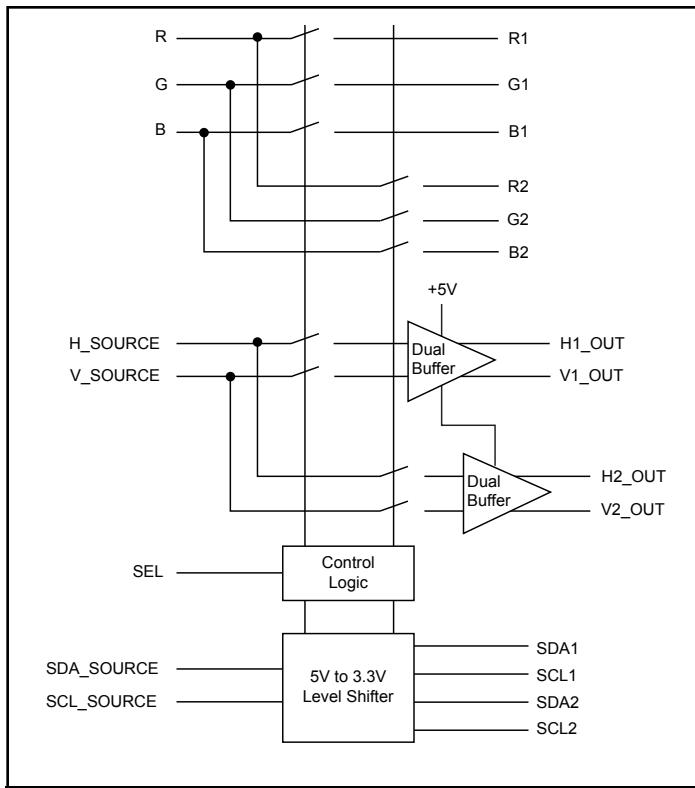
Description

Pericom's PI3V713-A is a 7-channel video mux/demux used to switch between multiple VGA sources or end points. In a notebook application where analog video signals are found in both the notebook and the dock, a switch solution is required to switch between the two video port locations. With the high bandwidth of $\sim 1.7\text{GHz}$, the signal integrity will remain strong even through the long FR4 trace between the notebook and the docking station. In addition to high signal performance, the video signals are also protected against high ESD with integrated diodes to V_{DD} and GND that will support up to 12kV HBM ESD protection.

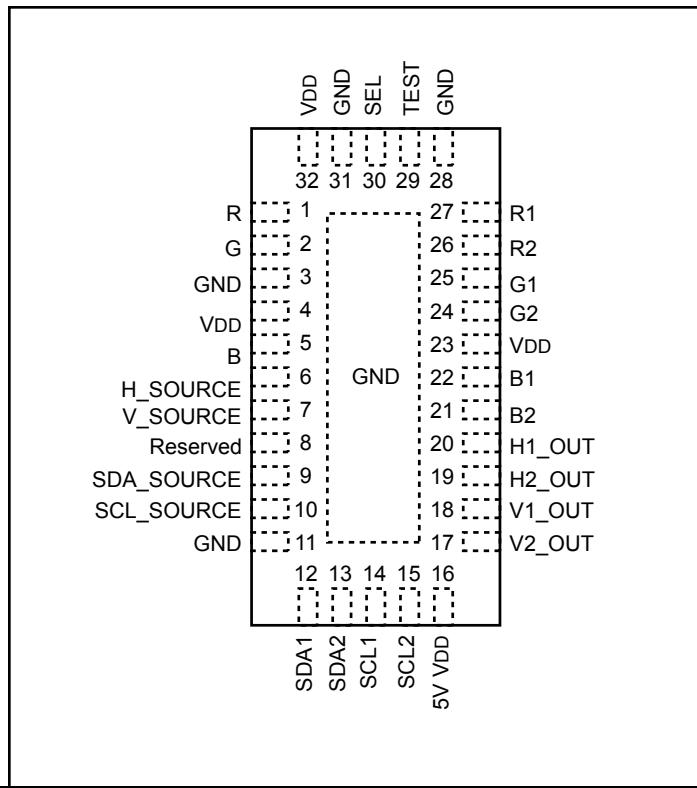
Application

Routing VGA signals with low signal attenuation and high ESD.

Block Diagram



Pin Diagram



Pin Description

Pin Number	Pin Name	Pin Type	Description
1	R	I/O	Red signal from VGA Transmitter
2	G	I/O	Green signal from VGA Transmitter
3	GND	Ground	Ground
4	V _{DD}	Power	3.3V +/-10% power rail
5	B	I/O	Blue signal from VGA Transmitter
6	H_SOURCE	I	Horizontal Synchronous signal from VGA Transmitter
7	V_SOURCE	I	Vertical Synchronous signal from VGA Transmitter
8	Reserved	I	For normal operation, this pin needs to be tied HIGH
9	SDA_SOURCE	I/O	DDC, data signal from VGA Transmitter
10	SCL_SOURCE	I/O	DDC, clock signal from VGA Transmitter
11	GND	Ground	Ground
12	SDA1	I/O	DDC, data signal for VGA output port 1
13	SDA2	I/O	DDC, data signal for VGA output port 2
14	SCL1	I/O	DDC, clock signal for VGA output port 1
15	SCL2	I/O	DDC, clock signal for VGA output port 2
16	5V V _{DD}	Power	5V +/-10% Power rail
17	V2_OUT	O	Vertical Synchronous buffered signal for VGA output port 2
18	V1_OUT	O	Vertical Synchronous buffered signal for VGA output port 1
19	H2_OUT	O	Horizontal Synchronous buffered signal for VGA output port 2
20	H1_OUT	O	Horizontal Synchronous buffered signal for VGA output port 1
21	B2	I/O	Blue signal for VGA port 2
22	B1	I/O	Blue signal for VGA port 1
23	V _{DD}	Power	3.3V +/-10% power rail
24	G2	I/O	Green signal for VGA port 2
25	G1	I/O	Green signal for VGA port 1
26	R2	I/O	Red signal for VGA port 2
27	R1	I/O	Red signal for VGA port 1
28	GND	Ground	Ground
29	TEST	Input	Description is TEST pin to enable TEST mode. IF this pin is LOW, then test mode is enabled. For normal usage disable TEST mode by holding this pin high, or floating. There is an internal 100Kohm pull-up on this pin
30	SEL	I	Control signal. If pin 30 is LOW, port 1 is chosen If pin 30 is HIGH, port 2 is chosen
31	GND	Ground	Ground
32	V _{DD}	Power	3.3V +/-10% power rail

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....	-65°C to +150°C
Supply Voltage to Ground Potential.....	-0.5V to +4.0V
DC Input Voltage.....	-0.5V to +5.5V
DC Output Current.....	120mA
Power Dissipation.....	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth Table

SEL	Result
0	Port 1 is active
1	Port 2 is active

DC Electrical Characteristics for Video Switching over Operating Range

($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 10\%$, 5V $V_{DD} = 5\text{V}$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units
V_{IH}	Input HIGH Voltage (SEL/Priority and MS pins)	Guaranteed HIGH level	2	-	-	V
V_{IL}	Input LOW Voltage (SEL/Priority, and MS pins)	Guaranteed LOW level	-0.5	-	0.8	
V_{IK}	Clamp Diode Voltage	$V_{DD} = \text{Max.}$, $I_{SELx} = -18\text{mA}$	-	-0.8	-1.2	
I_{IH}	Input HIGH Current (SEL/Priority)	$V_{DD} = \text{Max.}$, $V_{SELx} = V_{DD}$	-	-	± 5	μA
I_{IL}	Input LOW Current (SEL/Priority)	$V_{DD} = \text{Max.}$, $V_{SELx} = \text{GND}$	-	-	± 5	
$I_{OFF_H/V/DDC}$	Power Down Leakage Current for H/V and DDC channels only	$V_{DD} = 0\text{V}$, $V_B = 0\text{V}$, $V_A \leq 3.6$	-	-	± 5	
R_{ON}	Switch On-Resistance for RGB path ⁽³⁾	$V_{DD} = \text{Min.}$, $0\text{V} \leq V_{\text{input}} \leq 1.2\text{V}$, $I_{\text{input}} = -40\text{mA}$	-	4.8	5.6	Ω
$R_{FLAT(ON)}$	On-Resistance Flatness for RGB path ⁽⁴⁾	$V_{DD} = \text{Min.}$, $V_{\text{input}} @ 0\text{V}$ and 1.2V , $I_{\text{input}} = -40\text{mA}$	-	0.5	+1	
ΔR_{ON}	On-Resistance match from center ports to any other port (RGB path only) ⁽⁴⁾	$V_{DD} = \text{Min.}$, $0\text{V} \leq V_{\text{input}} \leq 1.2\text{V}$, $I_{\text{input}} = -40\text{mA}$	-	0.1	1	
$V_{OH}(\text{H/V})$	Output high for H/V signals	5V $V_{DD} = 5\text{V}$, $I_{OH} = -24\text{mA}$	3.0			V
$V_{OL}(\text{H/V})$	Output low for H/V signals	5V $V_{DD} = 5\text{V}$, $I_{OL} = 24\text{mA}$	0		0.8	

Capacitance (T_A = 25°C, f = 1MHz)

Parameters ⁽⁴⁾	Description	Test Conditions ⁽¹⁾	Typ. ⁽²⁾	Units
C _{IN}	Input Capacitance		2.0	pF
C _{OFF}	RGB Capacitance, Switch OFF		2.4	
C _{ON}	RGB Switch Capacitance, Switch ON		5.6	

Notes:

1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.
3. Measured by the voltage drop between input and output pins at indicated current through the switch. On-Resistance is determined by the lower of the voltages on the two pins.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units
I _{CC} _3.3V rail	Quiescent Power Supply Current for 3.3V power rail	V _{DD} = Max., V _{DD} = 3.6V, 5V V _{DD} = 5.5V V _{SEL} = GND or V _{DD}	-	250	500	µA
I _{CC} _5V V _{DD}	Quiescent Power supply current for 5V V _{DD}	5V V _{DD} = 5.5V, V _{DD} = 3.6V, V _{SEL} = GND or V _{DD}		100	500	nA

Notes:

1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Dynamic Electrical Characteristics Over the Operating Range (T_A=-40° to +85°C, V_{DD}=3.3V±10%, GND=0V)

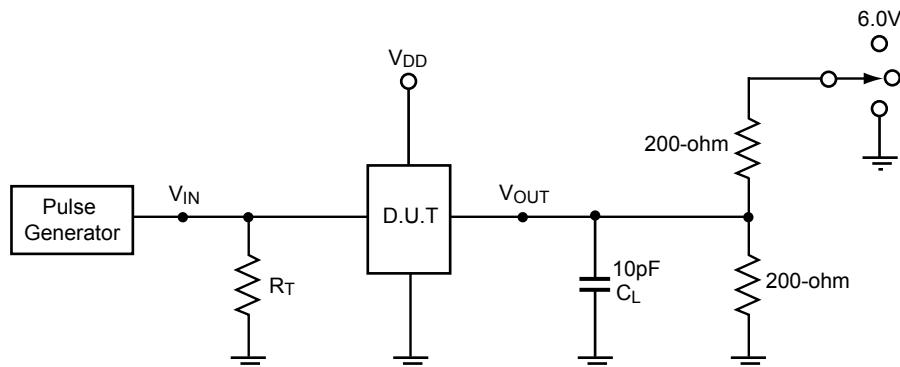
Parameters	Description	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Units
X _{TALK}	Crosstalk	f = 250MHz, See Fig. 2		-	-38	-	dB
O _{IRR}	OFF Isolation			-	-46	-	
BW	Bandwidth -3dB	See Fig. 1		-	1.7	-	GHz
I _{LOSS}	Insertion Loss for RGB path	with 75-Ohm load	Freq = 10MHz (VGA)		-1.77		dB
			Freq = 100MHz (XGA)		-1.88		
			Freq = 300MHz (UXGA)		-2.09		

Switching Characteristics

Parameters	Description	Min.	Typ. ⁽²⁾	Max.	Units
t _{PD}	Propagation Delay ^(2,3)	- 0.5 0.5 - 1.5 1.6	0.25		ns
t _{PZH} , t _{PZL}	Line Enable Time - SEL to Input, Output		-	15	
t _{PHZ} , t _{PLZ}	Line Disable Time - SEL to Input, Output		-	10	
t _{SK(p)}	Skew between opposite transitions of the same output (t _{PHL} - t _{PLH}) ⁽²⁾		0.1	0.2	
Trise (H/V)	Horizontal/Vertical synchronous output rise time (H1_out, V1_out, H2_out, and V2_out) with 15pF load			1.5	
Tfall (H/V)	Horizontal/Vertical synchronous output fall time (H1_out, V1_out, H2_out, and V2_out) with 15pF load			1.6	

Notes:

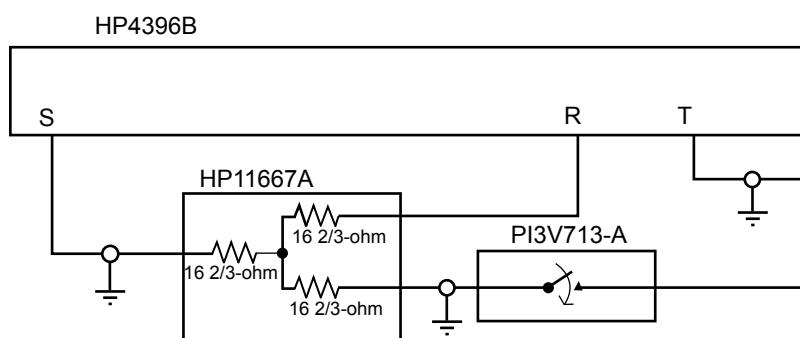
1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Guaranteed by design.
3. The switch contributes no propagational delay other than the RC delay of the On-Resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 10pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

Test Circuit for Electrical Characteristics⁽¹⁾

Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. All input impulses are supplied by generators having the following characteristics: $f = 10$ MHz, $Z_0 = 50\Omega$, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
4. The outputs are measured one at a time with one transition per measurement.

Switch Positions

Test	Switch
t_{PLZ} , t_{PZL} (output on I-side)	6.0V
t_{PHZ} , t_{PZH} (output on I-side)	GND
Prop Delay	Open

Test Circuit for Dynamic Electrical Characteristics

Figure 1. Bandwidth -3dB Testing

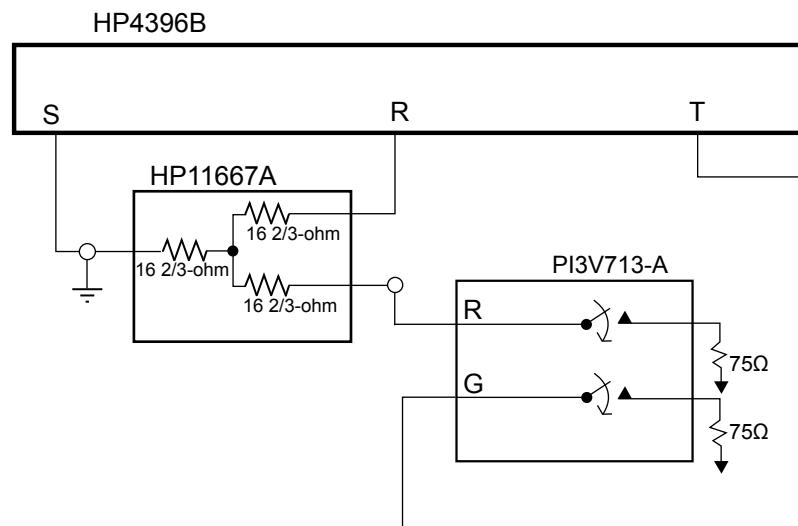


Figure 2. Crosstalk Test Setup

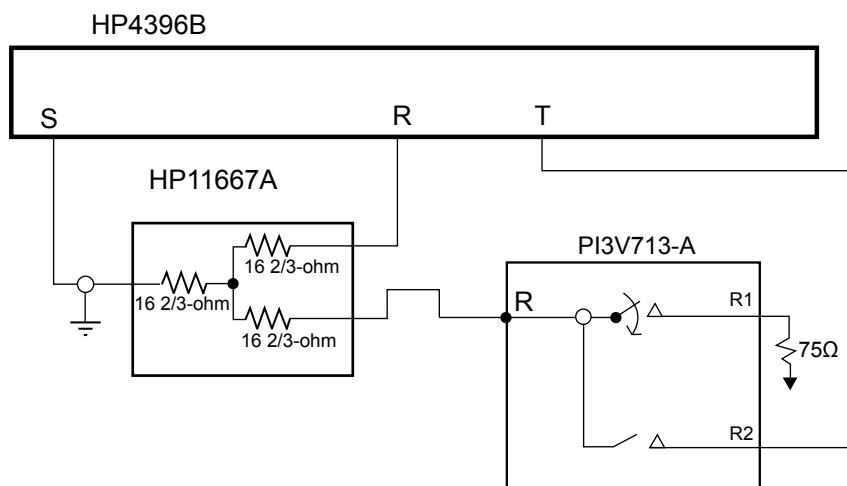
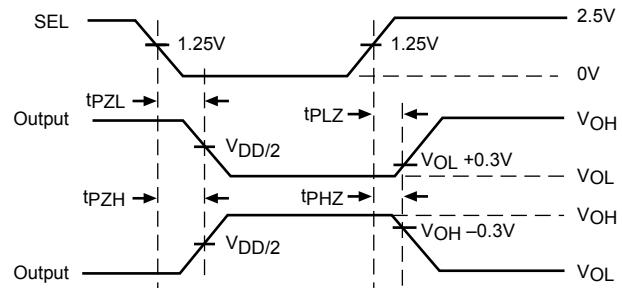
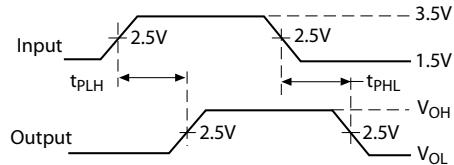
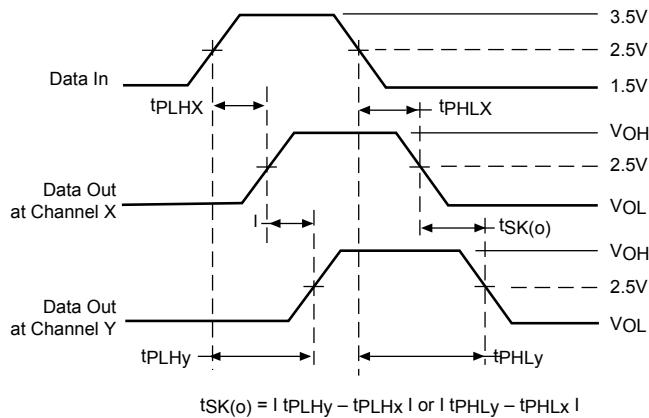


Figure 3. Off Isolation Test Setup

Switching Waveforms

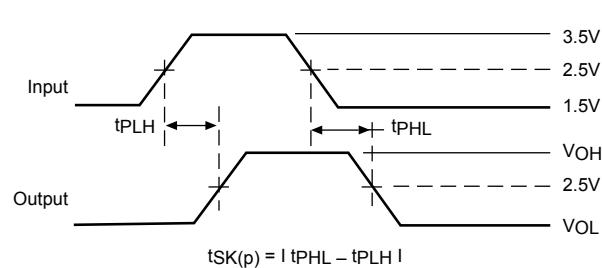


Voltage Waveforms Propagation Delay Times



Output Skew - $t_{SK(o)}$

Voltage Waveforms Enable and Disable Times

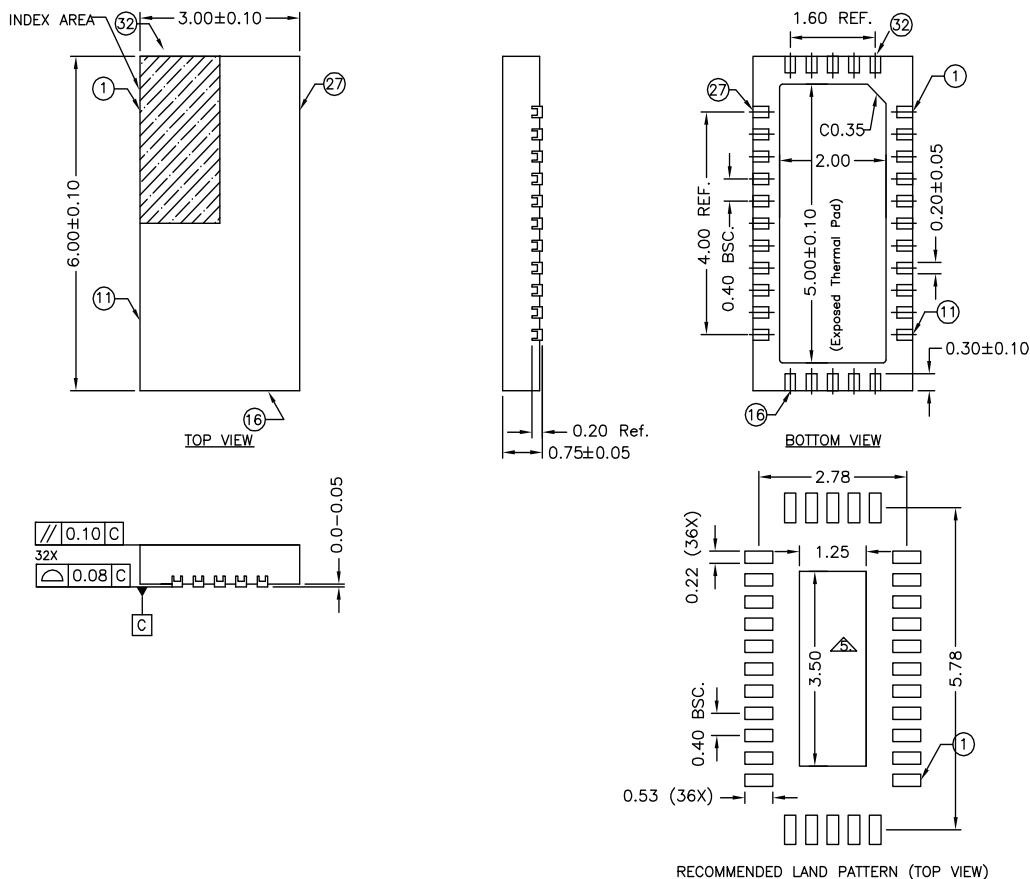


Pulse Skew - $t_{SK(p)}$

Applications Information

Logic Inputs

The logic control inputs can be driven up to +3.6V regardless of the supply voltage. For example, given a +3.3V supply, the output enables or select pins may be driven low to 0V and high to 3.6V. Driving IN Rail-to-Rail® minimizes power consumption.


NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA

PERICOM®
Enabling Serial Connectivity
DATE: 10/09/09
DESCRIPTION: 32-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)
PACKAGE CODE: ZL (ZL32)
DOCUMENT CONTROL #: PD-2044
REVISION: A

09-0125

Note:

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Ordering Information

Ordering Code	Package Code	Package Description
PI3V713-A ZLE	ZL	Pb-free & Green, 32-pin TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging