

# RF Power Field Effect Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies up to 1000 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 28 volt base station equipment.

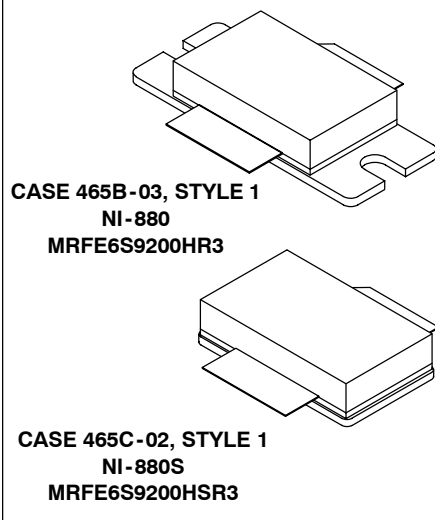
- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ} = 1400$  mA,  $P_{out} = 58$  Watts Avg.,  $f = 880$  MHz, 3GPP Test Model 1, 64 DPCH with 45.2% Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.  
Power Gain — 21 dB  
Drain Efficiency — 35%  
Device Output Signal PAR — 6.36 dB @ 0.01% Probability on CCDF  
ACPR @ 5 MHz Offset — -40 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 880 MHz,  $P_{out} = 300$  W CW (3 dB Input Overdrive from Rated  $P_{out}$ ), Designed for Enhanced Ruggedness.

### Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 32  $V_{DD}$  Operation
- Integrated ESD Protection
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

**MRFE6S9200HR3**  
**MRFE6S9200HSR3**

**880 MHz, 58 W AVG., 28 V**  
**SINGLE W-CDMA**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



**Table 1. Maximum Ratings**

| Rating                               | Symbol    | Value        | Unit |
|--------------------------------------|-----------|--------------|------|
| Drain-Source Voltage                 | $V_{DSS}$ | -0.5, +66    | Vdc  |
| Gate-Source Voltage                  | $V_{GS}$  | -0.5, +12    | Vdc  |
| Storage Temperature Range            | $T_{stg}$ | - 65 to +150 | °C   |
| Case Operating Temperature           | $T_C$     | 150          | °C   |
| Operating Junction Temperature (1,2) | $T_J$     | 225          | °C   |

**Table 2. Thermal Characteristics**

| Characteristic                       | Symbol          | Value (2,3) | Unit |
|--------------------------------------|-----------------|-------------|------|
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ |             | °C/W |
| Case Temperature 80°C, 200 W CW      |                 | 0.29        |      |
| Case Temperature 79°C, 58 W CW       |                 | 0.33        |      |

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

**Table 3. ESD Protection Characteristics**

| Test Methodology                      | Class        |
|---------------------------------------|--------------|
| Human Body Model (per JESD22-A114)    | 1C (Minimum) |
| Machine Model (per EIA/JESD22-A115)   | A (Minimum)  |
| Charge Device Model (per JESD22-C101) | IV (Minimum) |

**Table 4. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

**Off Characteristics**

|                                                                                                   |           |   |   |    |                 |
|---------------------------------------------------------------------------------------------------|-----------|---|---|----|-----------------|
| Zero Gate Voltage Drain Leakage Current<br>( $V_{DS} = 66\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ ) | $I_{DSS}$ | — | — | 10 | $\mu\text{Adc}$ |
| Zero Gate Voltage Drain Leakage Current<br>( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ ) | $I_{DSS}$ | — | — | 1  | $\mu\text{Adc}$ |
| Gate-Source Leakage Current<br>( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )              | $I_{GSS}$ | — | — | 10 | $\mu\text{Adc}$ |

**On Characteristics**

|                                                                                                                |              |     |     |     |     |
|----------------------------------------------------------------------------------------------------------------|--------------|-----|-----|-----|-----|
| Gate Threshold Voltage<br>( $V_{DS} = 10\text{ Vdc}$ , $I_D = 600\text{ }\mu\text{Adc}$ )                      | $V_{GS(th)}$ | 1.2 | 2   | 2.7 | Vdc |
| Gate Quiescent Voltage<br>( $V_{DD} = 28\text{ Vdc}$ , $I_D = 1400\text{ mAdc}$ , Measured in Functional Test) | $V_{GS(Q)}$  | 2   | 2.7 | 3.8 | Vdc |
| Drain-Source On-Voltage<br>( $V_{GS} = 10\text{ Vdc}$ , $I_D = 4.1\text{ Adc}$ )                               | $V_{DS(on)}$ | 0.1 | 0.2 | 0.3 | Vdc |

**Dynamic Characteristics <sup>(1)</sup>**

|                                                                                                                       |           |   |        |   |    |
|-----------------------------------------------------------------------------------------------------------------------|-----------|---|--------|---|----|
| Reverse Transfer Capacitance<br>( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ ) | $C_{rss}$ | — | 2.41   | — | pF |
| Output Capacitance<br>( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )           | $C_{oss}$ | — | 74.61  | — | pF |
| Input Capacitance<br>( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz)            | $C_{iss}$ | — | 557.27 | — | pF |

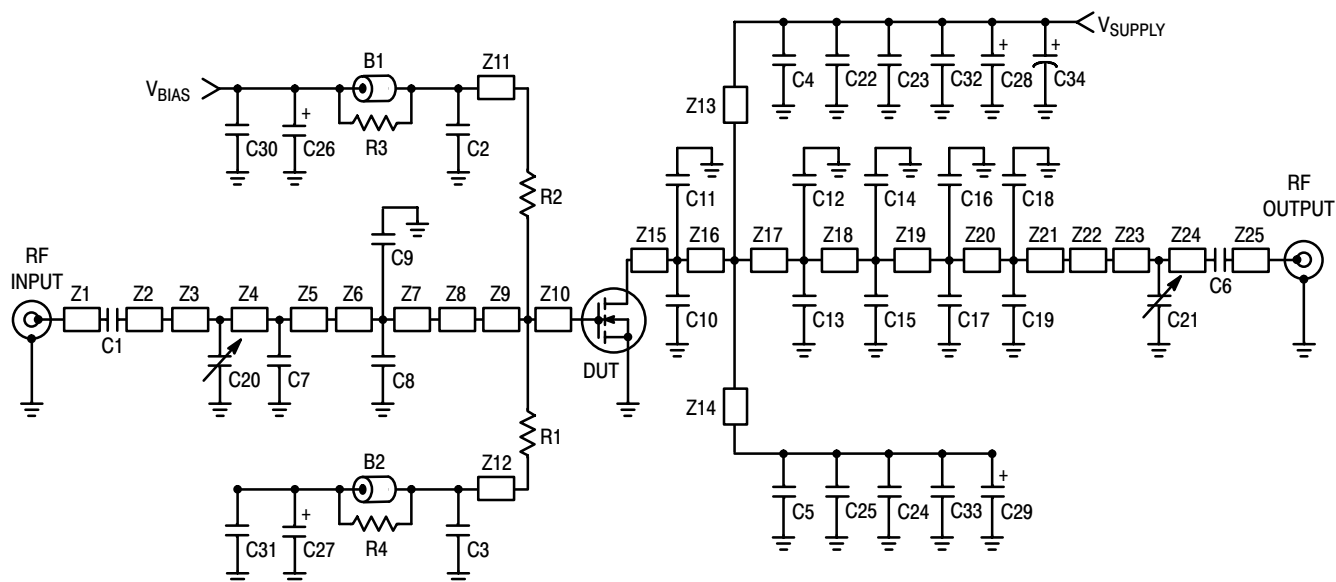
**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 1400\text{ mA}$ ,  $P_{out} = 58\text{ W Avg.}$  W-CDMA,  $f = 880\text{ MHz}$ , Single-Carrier W-CDMA, 3.84 MHz Channel Bandwidth Carrier. ACPR measured in 3.84 MHz Channel Bandwidth @ 5 MHz Offset. PAR = 7.5 dB @ 0.01% Probability on CCDF.

|                                                          |          |    |      |       |     |
|----------------------------------------------------------|----------|----|------|-------|-----|
| Power Gain                                               | $G_{ps}$ | 20 | 21   | 23    | dB  |
| Drain Efficiency                                         | $\eta_D$ | 33 | 35   | —     | %   |
| Output Peak-to-Average Ratio @ 0.01% Probability on CCDF | PAR      | 6  | 6.36 | —     | dB  |
| Adjacent Channel Power Ratio                             | ACPR     | —  | -40  | -36.5 | dBc |
| Input Return Loss                                        | IRL      | —  | -15  | -9    | dB  |

**Typical Performances** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 1400\text{ mA}$ , 865-900 MHz Bandwidth

|                                                                                                                                                                                           |                  |   |       |   |        |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|---|-------|---|--------|
| Video Bandwidth @ 200 W PEP $P_{out}$ where $IM3 = -30\text{ dBc}$<br>(Tone Spacing from 100 kHz to VBW)<br>$\Delta IM3 = IM3$ @ VBW frequency - $IM3$ @ 100 kHz < 1 dBc (both sidebands) | VBW              | — | 10    | — | MHz    |
| Gain Flatness in 35 MHz Bandwidth @ $P_{out} = 58\text{ W Avg.}$                                                                                                                          | $G_F$            | — | 0.5   | — | dB     |
| Average Deviation from Linear Phase in 35 MHz Bandwidth<br>@ $P_{out} = 200\text{ W CW}$                                                                                                  | $\Phi$           | — | 0.28  | — | °      |
| Average Group Delay @ $P_{out} = 200\text{ W CW}$ , $f = 880\text{ MHz}$                                                                                                                  | Delay            | — | 3.72  | — | ns     |
| Part-to-Part Insertion Phase Variation @ $P_{out} = 200\text{ W CW}$ ,<br>$f = 880\text{ MHz}$ , Six Sigma Window                                                                         | $\Delta\Phi$     | — | 15.9  | — | °      |
| Gain Variation over Temperature ( $-30^\circ\text{C}$ to $+85^\circ\text{C}$ )                                                                                                            | $\Delta G$       | — | 0.016 | — | dB/°C  |
| Output Power Variation over Temperature ( $-30^\circ\text{C}$ to $+85^\circ\text{C}$ )                                                                                                    | $\Delta P_{1dB}$ | — | 0.008 | — | dBm/°C |

1. Part is internally matched on input.

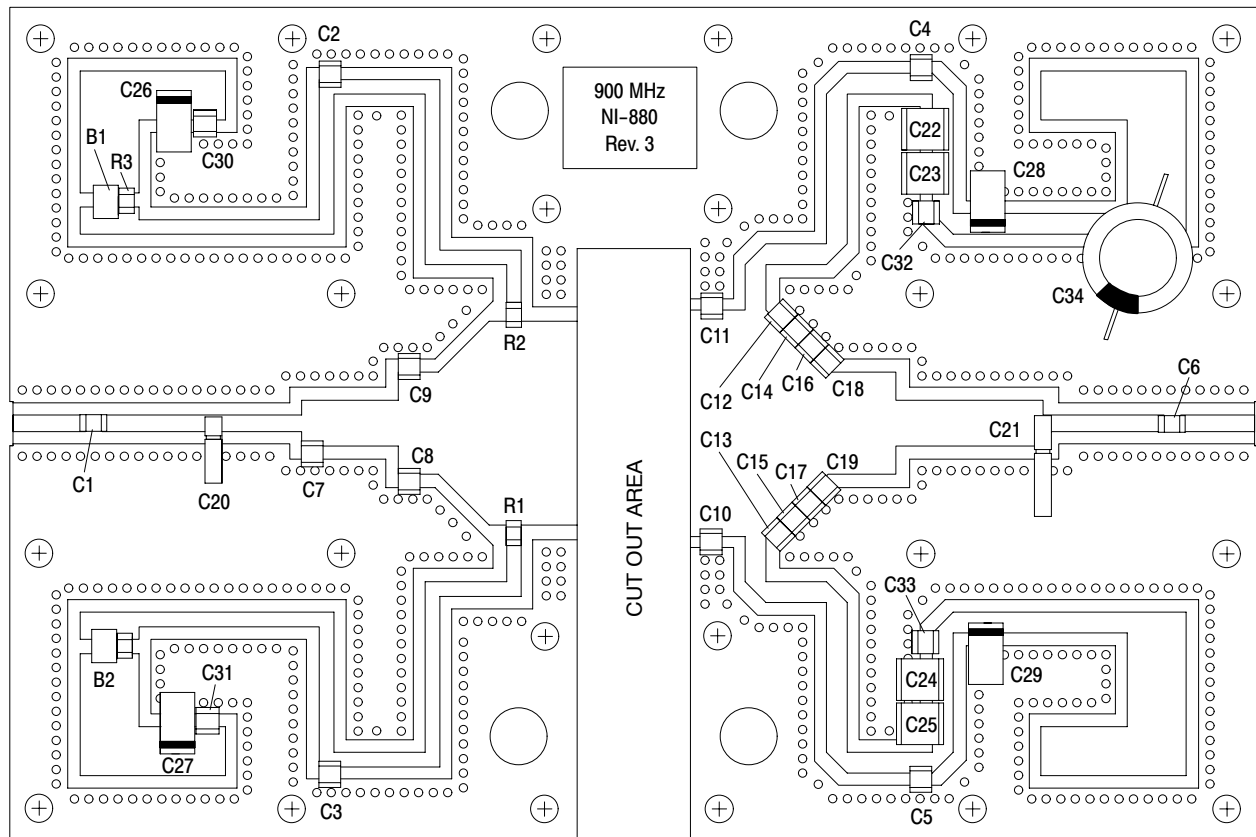


|    |                                |          |                                |     |                                                               |
|----|--------------------------------|----------|--------------------------------|-----|---------------------------------------------------------------|
| Z1 | 0.351" x 0.080" Microstrip     | Z9       | 0.119" x 0.118" Microstrip     | Z19 | 0.074" x 0.669" x 0.707" Taper                                |
| Z2 | 0.538" x 0.080" Microstrip     | Z10      | 0.305" x 0.980" Microstrip     | Z20 | 0.074" x 0.524" x 0.595" Taper                                |
| Z3 | 0.424" x 0.080" Microstrip     | Z11, Z12 | 2.134" x 0.070" Microstrip     | Z21 | 0.058" x 0.474" x 0.488" Taper                                |
| Z4 | 0.052" x 0.220" Microstrip     | Z13, Z14 | 1.885" x 0.100" Microstrip     | Z22 | 0.326" x 0.491" Microstrip                                    |
| Z5 | 0.414" x 0.220" Microstrip     | Z15      | 0.100" x 1.090" Microstrip     | Z23 | 0.708" x 0.220" Microstrip                                    |
| Z6 | 0.052" x 0.491" Microstrip     | Z16      | 0.212" x 1.090" Microstrip     | Z24 | 0.555" x 0.080" Microstrip                                    |
| Z7 | 0.140" x 0.491" Microstrip     | Z17      | 0.083" x 0.962" x 1.036" Taper | Z25 | 0.356" x 0.080" Microstrip                                    |
| Z8 | 0.244" x 0.736" x 0.980" Taper | Z18      | 0.074" x 0.816" x 0.888" Taper | PCB | Arlon CuClad 250GX-0300-55-22,<br>0.030", $\epsilon_r = 2.55$ |

**Figure 1. MRFE6S9200HR3(SR3) Test Circuit Schematic**

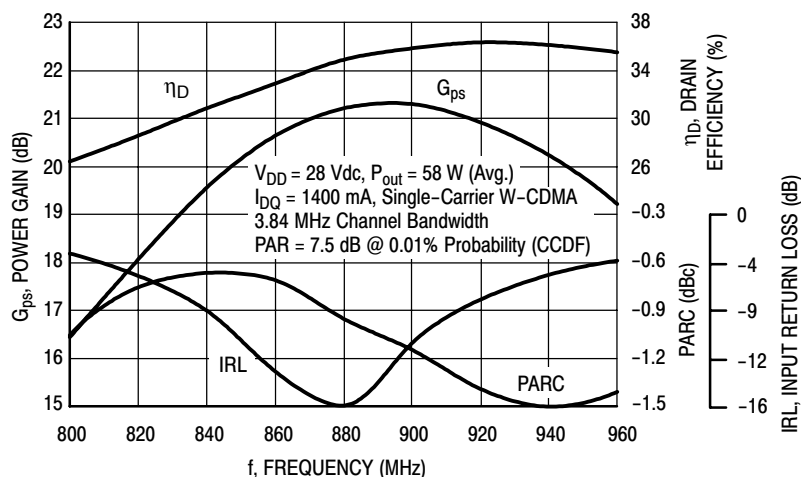
**Table 5. MRFE6S9200HR3(SR3) Test Circuit Component Designations and Values**

| Part                   | Description                               | Part Number        | Manufacturer     |
|------------------------|-------------------------------------------|--------------------|------------------|
| B1, B2                 | Small Ferrite Beads, Surface Mount        | 2743019447         | Fair Rite        |
| C1, C2, C3, C4, C5, C6 | 47 pF Chip Capacitors                     | ATC100B470JT500XT  | ATC              |
| C7                     | 2.7 pF Chip Capacitor                     | ATC100B2R7JT500XT  | ATC              |
| C8, C9, C18, C19       | 1.3 pF Chip Capacitors                    | ATC100B1R3JT500XT  | ATC              |
| C10, C11               | 12 pF Chip Capacitors                     | ATC100B120JT500XT  | ATC              |
| C12, C13               | 4.3 pF Chip Capacitors                    | ATC100B4R3JT500XT  | ATC              |
| C14, C15, C16, C17     | 3.3 pF Chip Capacitors                    | ATC100B3R3JT500XT  | ATC              |
| C20                    | 0.6-4.5 pF Variable Capacitor, Gigatrim   | 27271SL            | Johanson         |
| C21                    | 0.8-8.0 pF Variable Capacitor, Gigatrim   | 27291SL            | Johanson         |
| C22, C23, C24, C25     | 10 $\mu$ F, 50 V Chip Capacitors          | GRM55DR61H106KA88B | Murata           |
| C26, C27               | 10 $\mu$ F, 35 V Tantalum Chip Capacitors | T491C106K035AT     | Kemet            |
| C28, C29               | 22 $\mu$ F, 35 V Tantalum Chip Capacitors | T491C226K035AT     | Kemet            |
| C30, C31, C32, C33     | 0.1 $\mu$ F Chip Capacitors               | CDR33Bx104AKYS     | Kemet            |
| C34                    | 330 $\mu$ F, 63 V Electrolytic Capacitor  | EKMG630ELL331MJ205 | United Chemi-Con |
| R1, R2, R3, R4         | 10 $\Omega$ , 1/4 W Chip Resistors        | CRCW120610R0FKEA   | Vishay           |

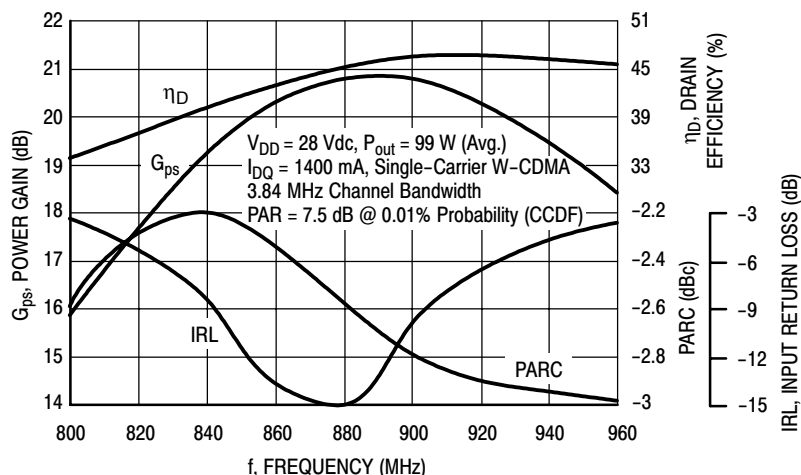


**Figure 2. MRFE6S9200HR3(SR3) Test Circuit Component Layout**

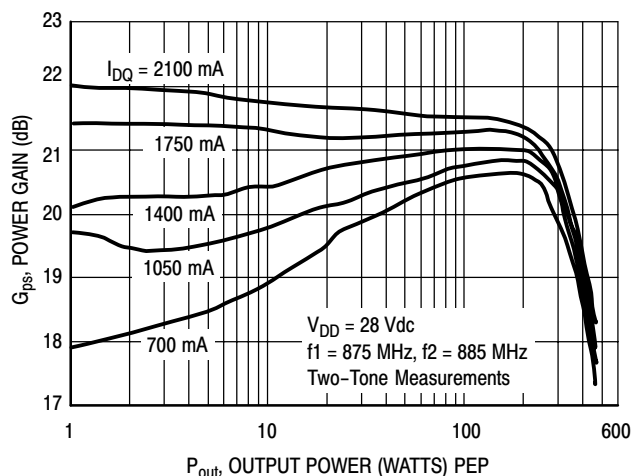
## TYPICAL CHARACTERISTICS



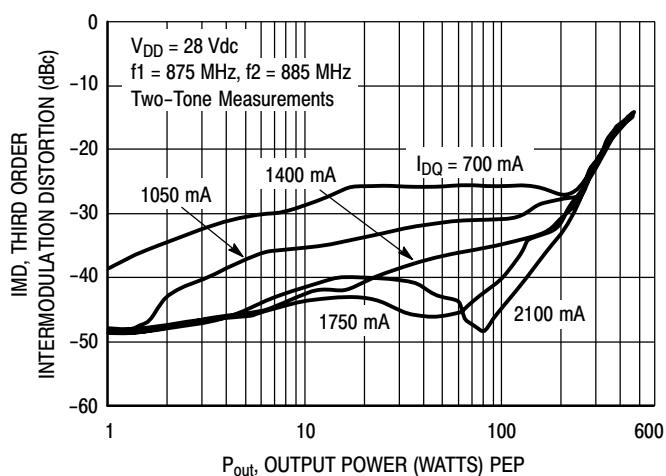
**Figure 3. Single-Carrier W-CDMA Broadband Performance  
@  $P_{out} = 58$  Watts Avg.**



**Figure 4. Single-Carrier W-CDMA Broadband Performance  
@  $P_{out} = 99$  Watts Avg.**

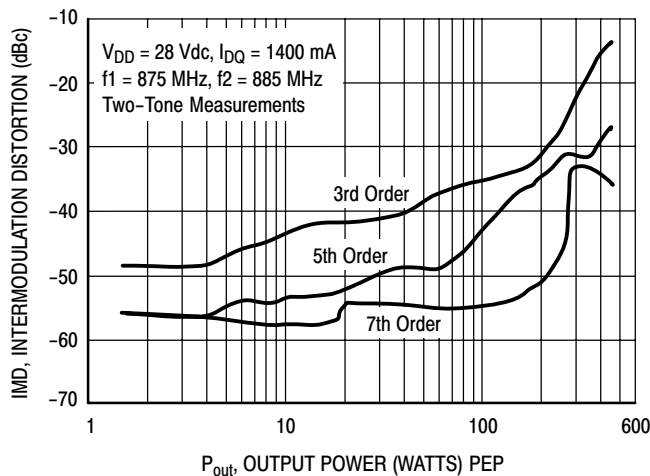


**Figure 5. Two-Tone Power Gain versus  
Output Power**

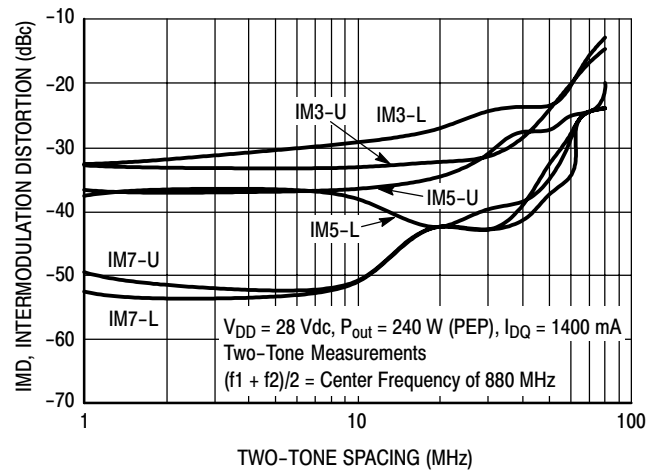


**Figure 6. Third Order Intermodulation Distortion  
versus Output Power**

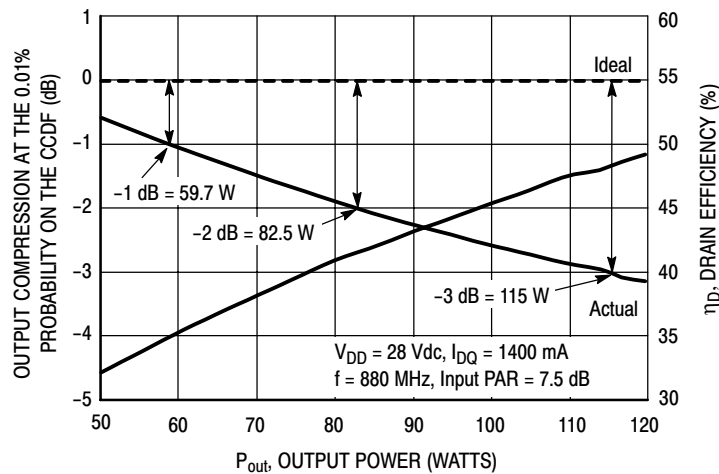
## TYPICAL CHARACTERISTICS



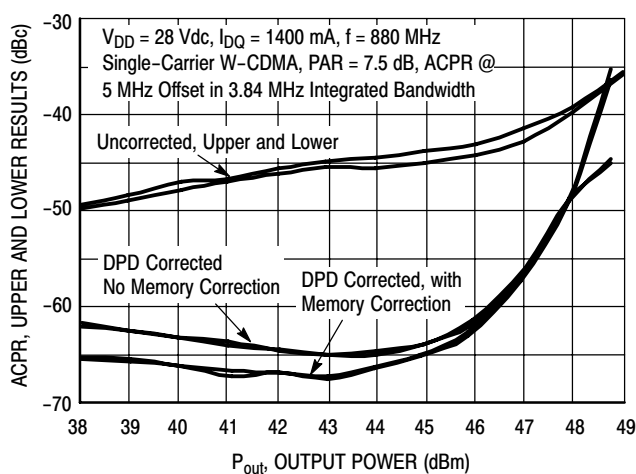
**Figure 7. Intermodulation Distortion Products versus Output Power**



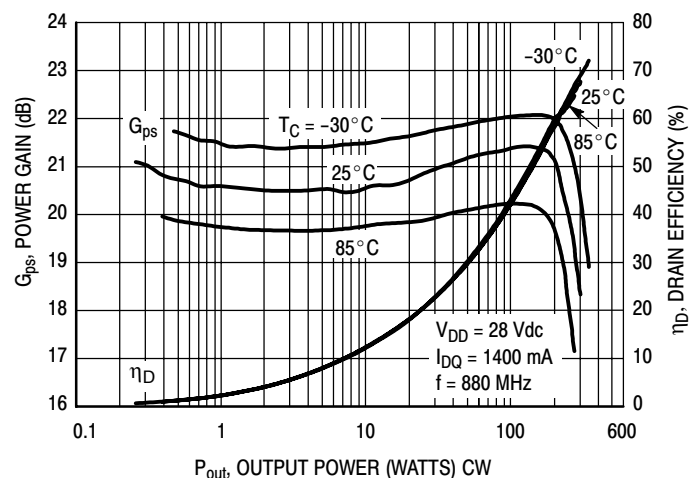
**Figure 8. Intermodulation Distortion Products versus Tone Spacing**



**Figure 9. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

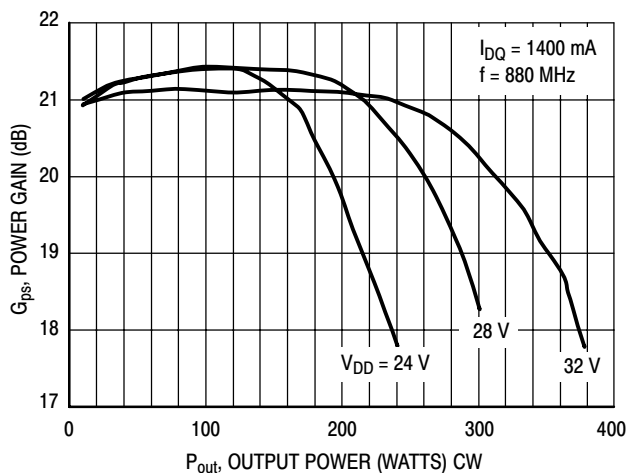


**Figure 10. Digital Predistortion Correction versus ACPR and Output Power**

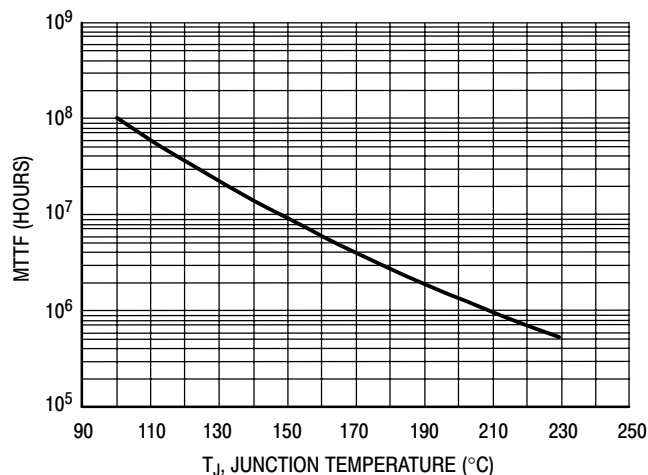


**Figure 11. Power Gain and Drain Efficiency versus CW Output Power**

## TYPICAL CHARACTERISTICS



**Figure 12. Power Gain versus Output Power**

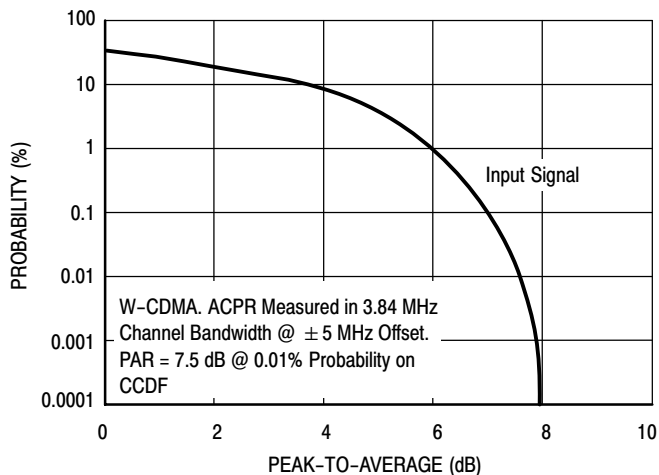


This above graph displays calculated MTTF in hours when the device is operated at  $V_{DD} = 28$  Vdc,  $P_{out} = 58$  W Avg., and  $\eta_D = 35\%$ .

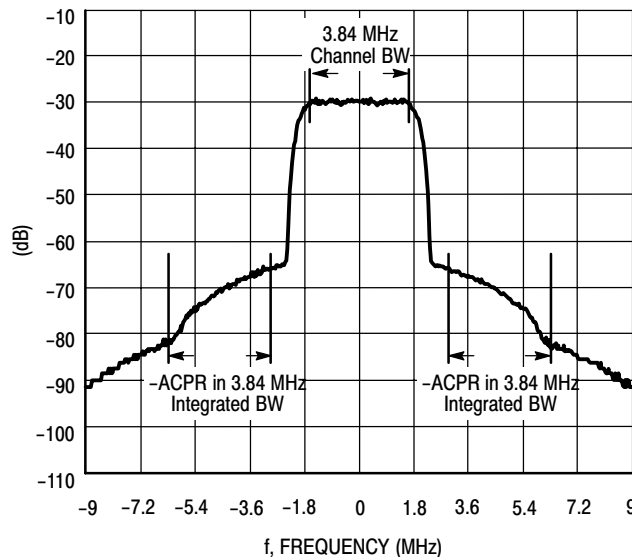
MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

**Figure 13. MTTF versus Junction Temperature**

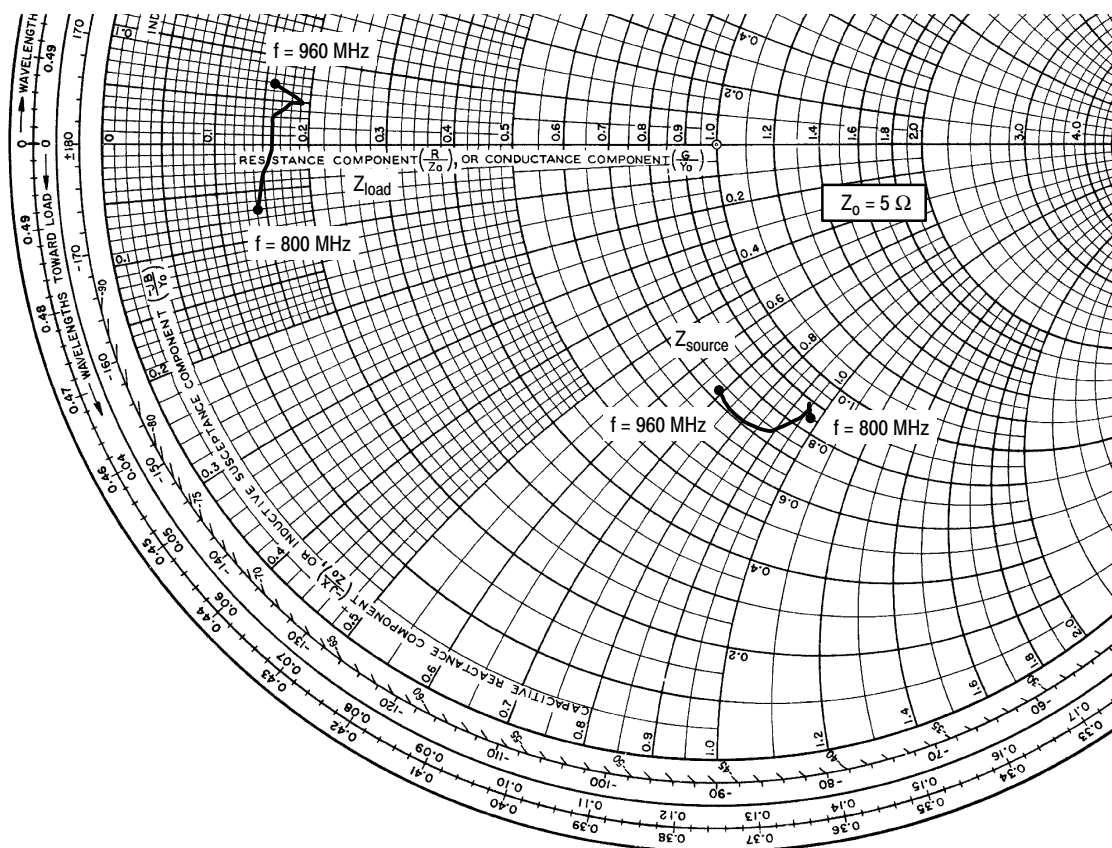
## W-CDMA TEST SIGNAL



**Figure 14. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal**



**Figure 15. Single-Carrier W-CDMA Spectrum**



$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 1400 \text{ mA}$ ,  $P_{out} = 58 \text{ W Avg.}$

| f<br>MHz | $Z_{source}$<br>$\Omega$ | $Z_{load}$<br>$\Omega$ |
|----------|--------------------------|------------------------|
| 800      | $4.23 - j4.85$           | $0.70 - j0.33$         |
| 820      | $4.46 - j4.69$           | $0.76 - j0.13$         |
| 840      | $4.39 - j4.75$           | $0.78 - j0.02$         |
| 860      | $4.06 - j4.68$           | $0.79 + j0.09$         |
| 880      | $3.70 - j4.45$           | $0.81 + j0.16$         |
| 900      | $3.55 - j4.04$           | $0.86 + j0.21$         |
| 920      | $3.57 - j3.71$           | $0.89 + j0.27$         |
| 940      | $3.67 - j3.47$           | $0.89 + j0.31$         |
| 960      | $3.67 - j3.45$           | $0.82 + j0.33$         |

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

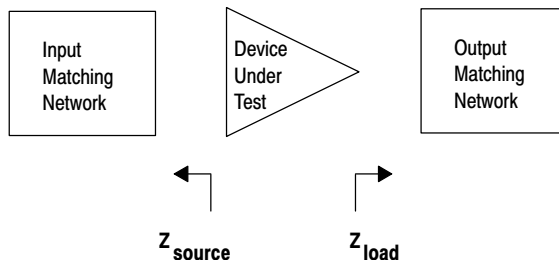
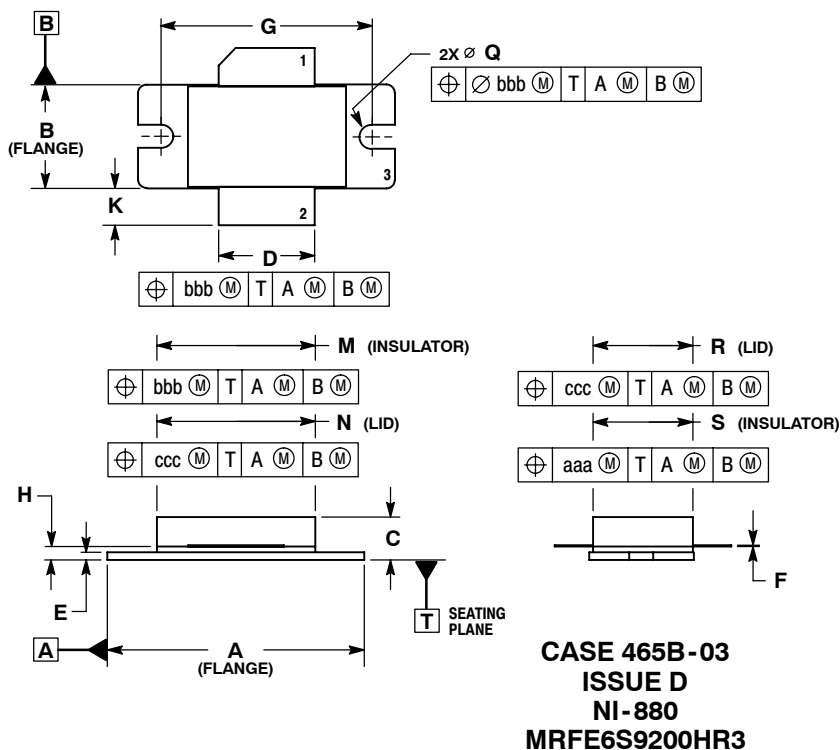


Figure 16. Series Equivalent Source and Load Impedance

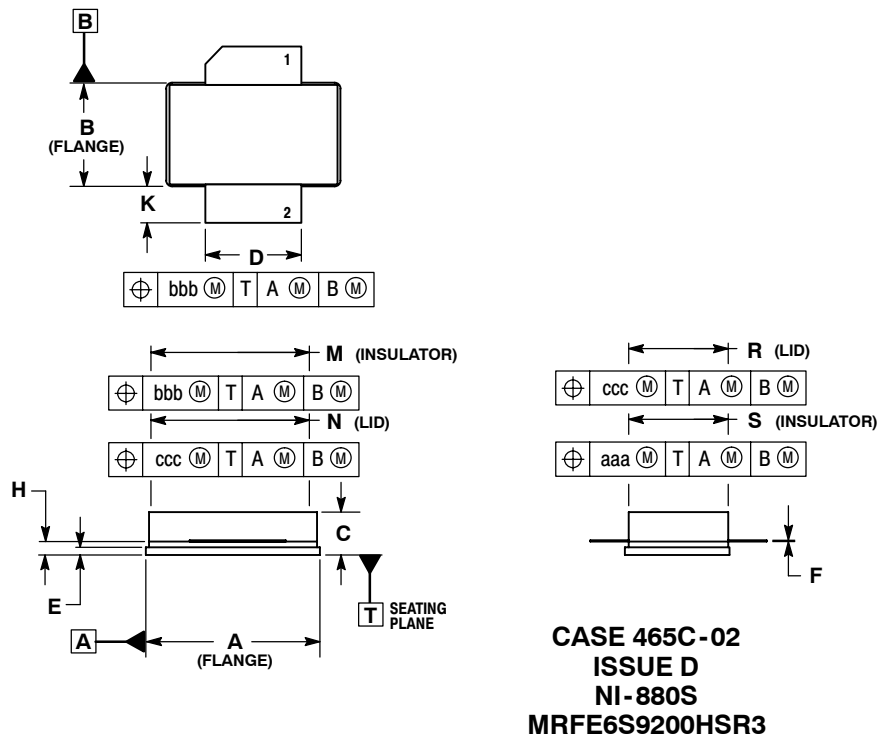
## PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
  4. DELETED

| DIM | INCHES |       | MILLIMETERS |        |
|-----|--------|-------|-------------|--------|
|     | MIN    | MAX   | MIN         | MAX    |
| A   | 1.335  | 1.345 | 33.91       | 34.16  |
| B   | 0.535  | 0.545 | 13.6        | 13.8   |
| C   | 0.147  | 0.200 | 3.73        | 5.08   |
| D   | 0.495  | 0.505 | 12.57       | 12.83  |
| E   | 0.035  | 0.045 | 0.89        | 1.14   |
| F   | 0.003  | 0.006 | 0.08        | 0.15   |
| G   | 1.100  | BSC   | 27.94       | BSC    |
| H   | 0.057  | 0.067 | 1.45        | 1.70   |
| K   | 0.170  | 0.210 | 4.32        | 5.33   |
| M   | 0.872  | 0.888 | 22.15       | 22.55  |
| N   | 0.871  | 0.889 | 19.30       | 22.60  |
| Q   | Ø.118  | Ø.138 | Ø.3.00      | Ø.3.51 |
| R   | 0.515  | 0.525 | 13.10       | 13.30  |
| S   | 0.515  | 0.525 | 13.10       | 13.30  |
| aaa | 0.007  | REF   | 0.178       | REF    |
| bbb | 0.010  | REF   | 0.254       | REF    |
| ccc | 0.015  | REF   | 0.381       | REF    |

- STYLE 1:  
PIN 1. DRAIN  
2. GATE  
3. SOURCE



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

| DIM | INCHES |       | MILLIMETERS |       |
|-----|--------|-------|-------------|-------|
|     | MIN    | MAX   | MIN         | MAX   |
| A   | 0.905  | 0.915 | 22.99       | 23.24 |
| B   | 0.535  | 0.545 | 13.60       | 13.80 |
| C   | 0.147  | 0.200 | 3.73        | 5.08  |
| D   | 0.495  | 0.505 | 12.57       | 12.83 |
| E   | 0.035  | 0.045 | 0.89        | 1.14  |
| F   | 0.003  | 0.006 | 0.08        | 0.15  |
| H   | 0.057  | 0.067 | 1.45        | 1.70  |
| K   | 0.170  | 0.210 | 4.32        | 5.33  |
| M   | 0.872  | 0.888 | 22.15       | 22.55 |
| N   | 0.871  | 0.889 | 19.30       | 22.60 |
| R   | 0.515  | 0.525 | 13.10       | 13.30 |
| S   | 0.515  | 0.525 | 13.10       | 13.30 |
| aaa | 0.007  | REF   | 0.178       | REF   |
| bbb | 0.010  | REF   | 0.254       | REF   |
| ccc | 0.015  | REF   | 0.381       | REF   |

- STYLE 1:  
PIN 1. DRAIN  
2. GATE  
3. SOURCE

## PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

## REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0        | Mar. 2007 | <ul style="list-style-type: none"> <li>• Initial Release of Data Sheet</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 1        | Dec. 2008 | <ul style="list-style-type: none"> <li>• Updated Full Frequency Band in Typical Performance bullet to <math>f = 880</math> MHz to match actual production test, p. 1</li> <li>• Clarified 3 dB overdrive test condition for HV6E enhanced ruggedness parts, p. 1</li> <li>• Corrected <math>C_{iss}</math> test condition to indicate AC stimulus on the <math>V_{GS}</math> connection versus the <math>V_{DS}</math> connection, Dynamic Characteristics table, p. 2</li> <li>• Changed maximum adjacent channel power ratio specification from -38.5 dBc to -36.5 dBc to match actual production test limits, p. 2</li> <li>• Updated PCB information to show more specific material details, Fig. 1, Test Circuit Schematic, p. 3</li> <li>• Updated Part Numbers in Table 5, Component Designations and Values, to latest RoHS compliant part numbers, p. 3</li> <li>• Deleted output signal data from Fig. 14, CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal, p. 7</li> </ul> |

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