DSC1104/24

Low Jitter Precision HCSL Oscillator

Features

- Low RMS Phase Jitter: <1 ps (typ.)
- High Stability: ±10 ppm, ±20 ppm, ±25 ppm, ±50 ppm
- Wide Temperature Range
  - Industrial: –40°C to +85°C
  - Ext. Commercial: –20°C to +70°C
  - Ext. Industrial: –40°C to +105°C
- High Supply Noise Rejection: –50 dBc
- Wide Frequency Range: 2.3 MHz to 460 MHz
- Small Industry Standard Footprints:
  - 2.5 mm x 2.0 mm, 3.2 mm x 2.5 mm, 5.0 mm x 3.2 mm, and 7.0 mm x 5.0 mm
- Excellent Shock and Vibration Immunity
  - Qualified to MIL-STD-883
- High Reliability
  - 20x Better MTF than Quartz Oscillators
- Low Current Consumption
- Supply Range of 2.25V to 3.6V
- Standby and Output Enable Function
- Lead Free and RoHS Compliant

Applications

- Storage Area Networks
  - SATA, SAS, Fibre Channel
- Passive Optical Networks
  - EPON, 10G-EPON, GPON, 10G-PON
- Ethernet
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- HD/SD/SDI Video and Surveillance
- PCI Express: Gen 1 to Gen 4
- Display Port

General Description

The DSC1104 and DSC1124 series of high performance oscillators utilizes a proven silicon MEMS technology to provide excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the need for quartz or SAW technology, MEMS oscillators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

DSC1104 has a standby feature allowing it to completely power down when EN pin is pulled low; whereas for DSC1124, only the outputs are disabled when EN is low. Both oscillators are available in industry standard packages, including the small 2.5 mm x 2.0 mm, and are drop-in replacements for standard 6-pin HCSL quartz crystal oscillators.

Block Diagram

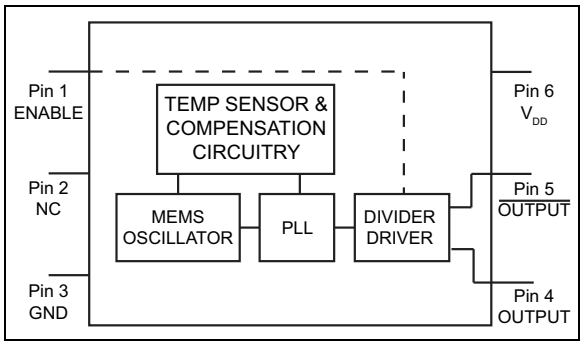


TABLE 1: OUTPUT ENABLE MODES

EN Pin	DSC1104	DSC1124
High	Outputs Active	Outputs Active
NC	Outputs Active	Outputs Active
Low	Standby	Outputs Disabled

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ..... –0.3V to +4.0V
Input Voltage ..... –0.3V to V_{DD} + 0.3V
ESD Protection (HBM) ..... 4 kV
ESD Protection (MM) 400V
ESD Protection (CDM) ..... 1.5 kV

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Specifications: V_{DD} = 3.3V; T_A = +25°C unless otherwise specified.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	V_{DD}	2.25	—	3.6	V	—
Supply Current	I_{DD}	—	—	0.095	mA	DSC1104, EN pin low, Output is disabled
		—	20	22		DSC1124, EN pin low, Output is disabled
Frequency Stability	Δf	—	—	±10	ppm	Includes frequency variation due to initial tolerance, temp., and power supply voltage
		—	—	±20		
		—	—	±25		
		—	—	±50		
Aging	Δf_{Y1}	—	—	±5	ppm	One year at +25°C
Start-up Time (Note 2)	t_{SU}	—	—	5	ms	T = +25°C
Input Logic Levels	V_{IH}	0.75 x V_{DD}	—	—	V	Input logic high
	V_{IL}	—	—	0.25 x V_{DD}		Input logic low
Output Disable Time (Note 3)	t_{DA}	—	—	5	ns	—
Output Enable Time	t_{EN}	—	—	5	ms	DSC1104
		—	—	20	ns	DSC1124
Enable Pull-Up Resistor (Note 4)	R_{PU}	—	40	—	kΩ	Pull-up resistor exists
HCSL Outputs						
Supply Current	I_{DD}	—	40	42	mA	Output Enabled, R_L = 50Ω
Output Logic Levels	V_{OH}	0.725	—	—	V	Output logic high, R_L = 50Ω
	V_{OL}	—	—	0.1		Output logic low
Peak-to-Peak Output Swing	—	—	750	—	mV	Single-Ended
Output Transition Time (Note 3)	t_r	200	—	400	ps	Rise time, 20% to 80%, R_L = 50Ω, C_L = 2 pF
	t_f	200	—	—		Fall time, 20% to 80%, R_L = 50Ω, C_L = 2 pF
Frequency	f_0	2.3	—	460	MHz	Single frequency
Output Duty Cycle	SYM	48	—	52	%	Differential

ELECTRICAL CHARACTERISTICS (CONTINUED)

Specifications: V_{DD} = 3.3V; T_A = +25°C unless otherwise specified.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Period Jitter	J_{PER}	—	2.5	—	ps_{RMS}	—
Integrated Phase Noise	J_{PH}	—	0.25	—	ps_{RMS}	200 kHz to 20 MHz @ 156.25 MHz
		—	0.38	—		100 kHz to 20 MHz @ 156.25 MHz
		—	1.7	2		12 kHz to 20 MHz @ 156.25 MHz

Note 1: Pin 6 V_{DD} should be filtered with a 0.1 µF capacitor.

2: t_{SU} is time to 100 ppm stable output frequency after V_{DD} is applied and outputs are enabled.

3: Output Waveform and Test Circuit figures below define the parameters.

4: Output is enabled if pad is floated or not connected.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Operating Temperature Range	T_A	–20	—	+70	°C	Ordering Option E
		–40	—	+85	°C	Ordering Option I
		–40	—	+105	°C	Ordering Option L
Junction Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_S	–55	—	+150	°C	—
Soldering Temperature	—	—	—	+260	°C	40 sec. max.

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature, and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

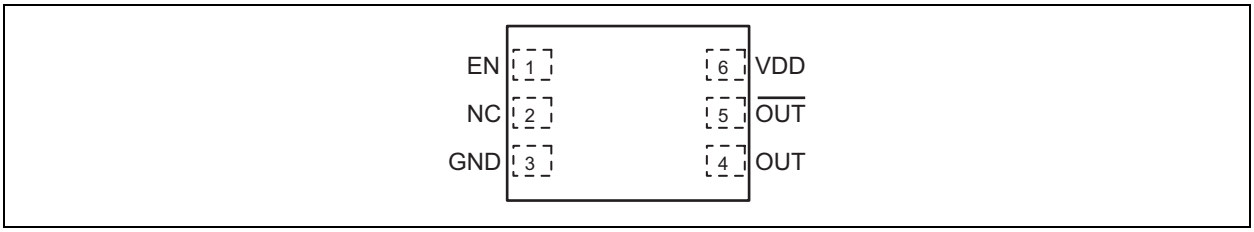


FIGURE 2-1: *Pin Configuration, 6-Lead QFN.*

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	EN	Enable.
2	NC	Leave unconnected.
3	GND	Ground.
4	OUT	Output.
5	$\overline{\text{OUT}}$	Complementary output.
6	VDD	Input.

3.0 NOMINAL PERFORMANCE PARAMETERS

Unless specified otherwise, T = +25°C, V_{DD} = 3.3V.

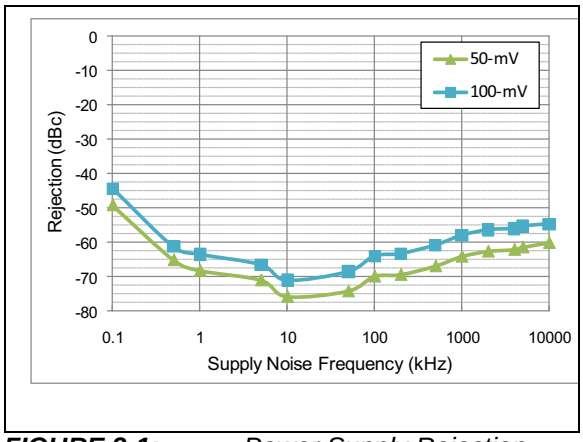


FIGURE 3-1: *Power Supply Rejection Ratio.*

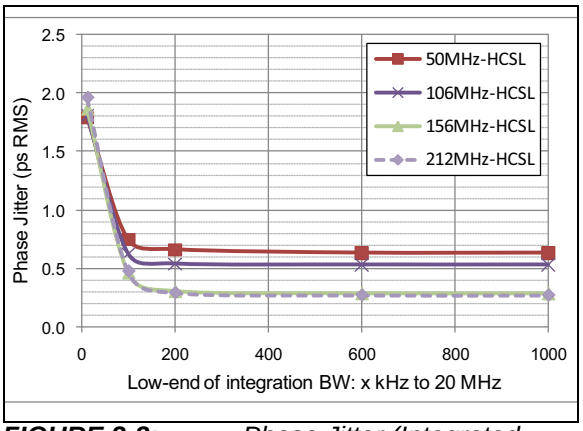


FIGURE 3-2: *Phase Jitter (Integrated Phase Noise).*

4.0 OUTPUT WAVEFORM

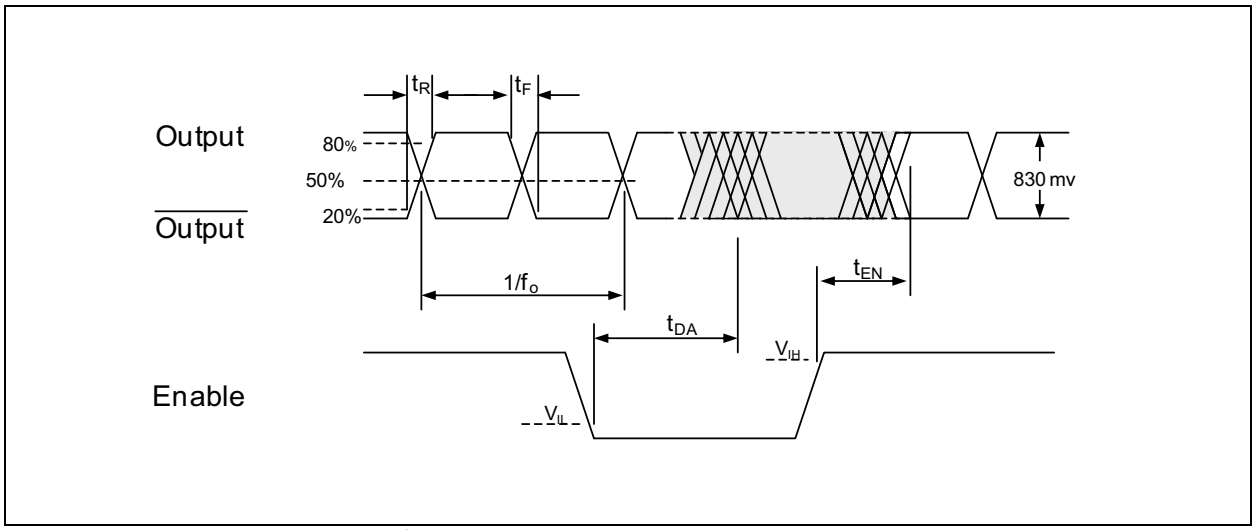


FIGURE 4-1: *Output Waveform.*

5.0 TYPICAL TERMINATION SCHEME

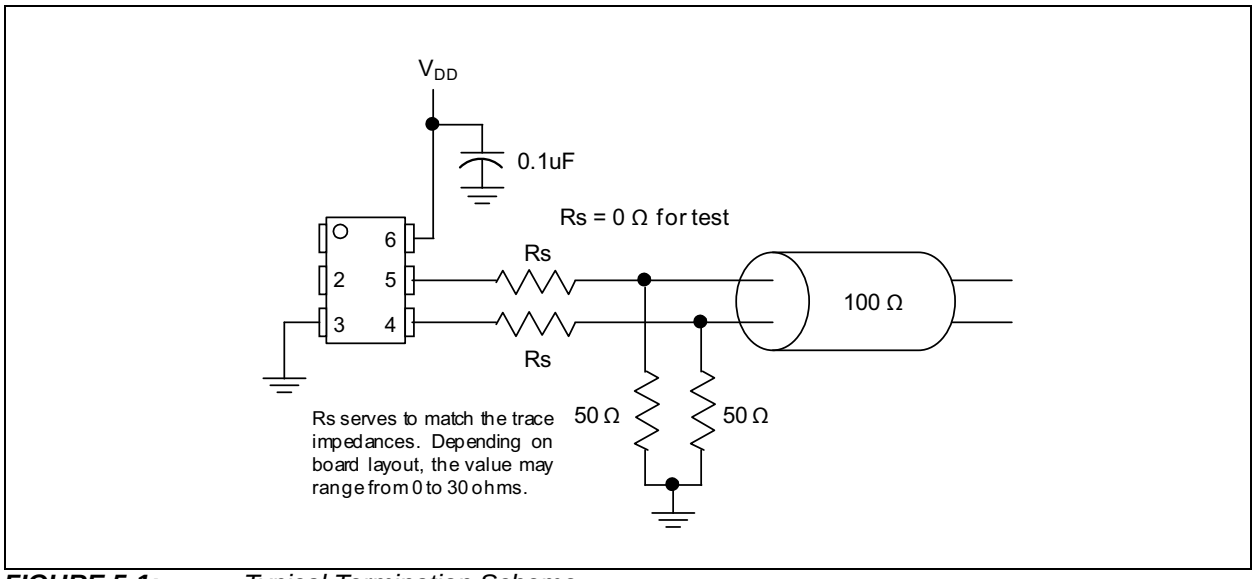


FIGURE 5-1: *Typical Termination Scheme.*

6.0 TEST CIRCUIT

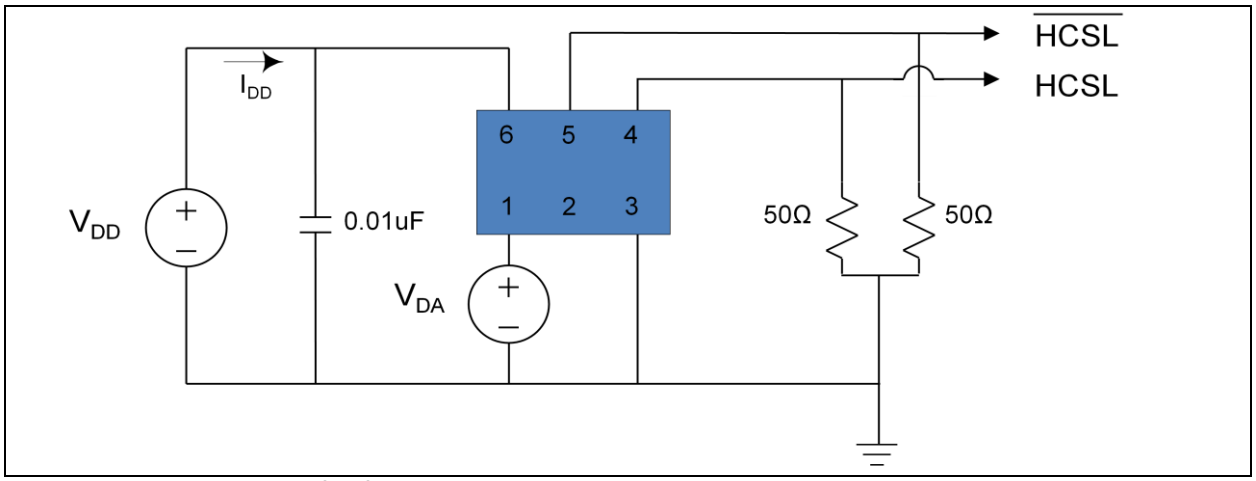
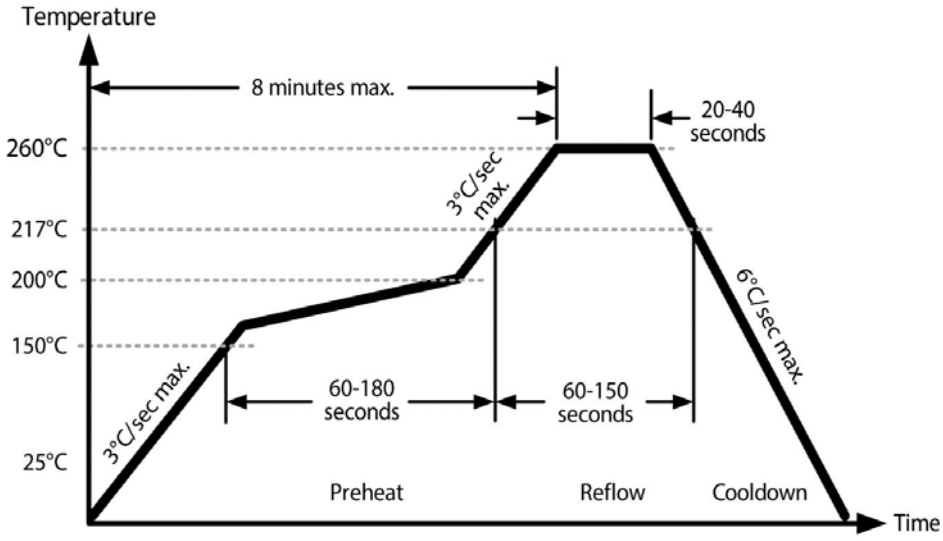


FIGURE 6-1: *Test Circuit.*

7.0 SOLDER REFLOW PROFILE

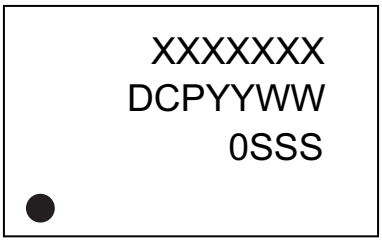


MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/sec. max.
Preheat Time 150°C to 200°C	60-180 sec.
Time Maintained above 217°C	60-150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of Actual Peak	20-40 sec.
Ramp-Down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

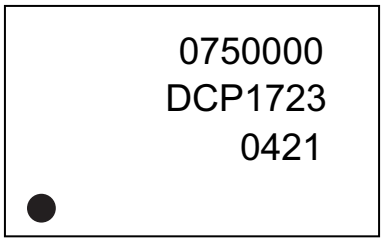
8.0 PACKAGE MARKING INFORMATION

8.1 Package Marking Information

6-Pin CDFN/VDFN*



Example



Legend:	XX...X	Product code, customer-specific information, or frequency in MHz without printed decimal point
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	SSS	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

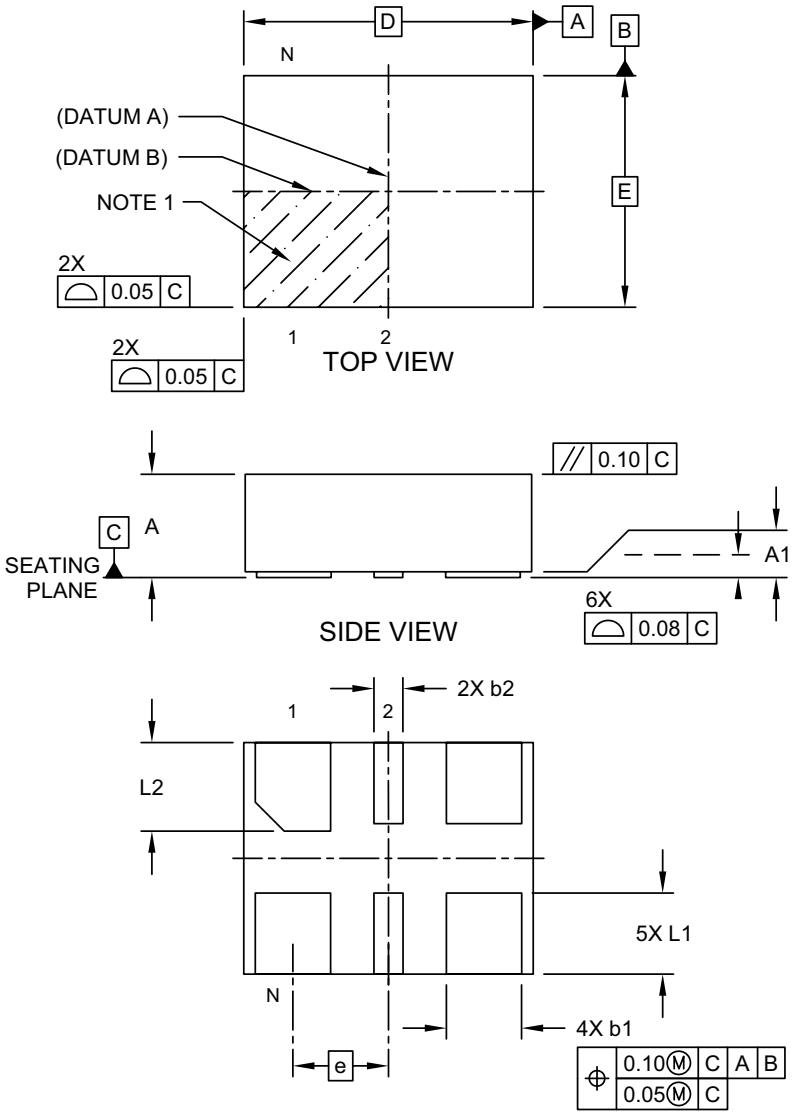
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

6-Lead VDFN 2.5 mm x 2.0 mm Package Outline and Recommended Land Pattern

6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

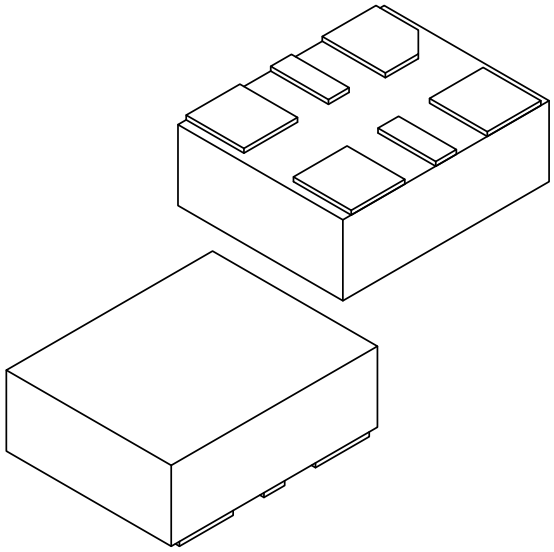
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1005A Sheet 1 of 2

6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		0.825 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D		2.50 BSC	
Overall Width	E		2.00 BSC	
Terminal Width	b1	0.60	0.65	0.70
Terminal Width	b2	0.20	0.25	0.30
Terminal Length	L1	0.60	0.70	0.80
Terminal Length	L2	0.665	0.765	0.865

Notes:

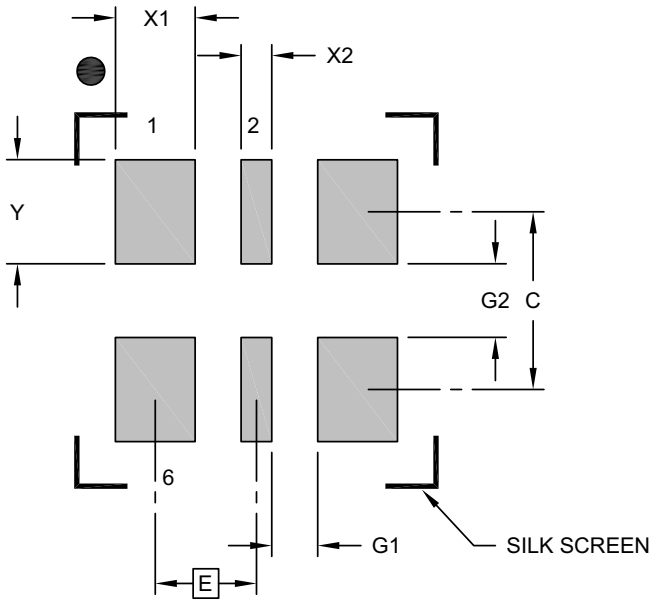
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1005A Sheet 2 of 2

6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.825 BSC		
Contact Pad Width (X4)	X1			0.65
Contact Pad Width (X2)	X2			0.25
Contact Pad Length (X6)	Y			0.85
Contact Pad Spacing	C		1.45	
Space Between Contacts (X4)	G1	0.38		
Space Between Contacts (X3)	G2	0.60		

Notes:

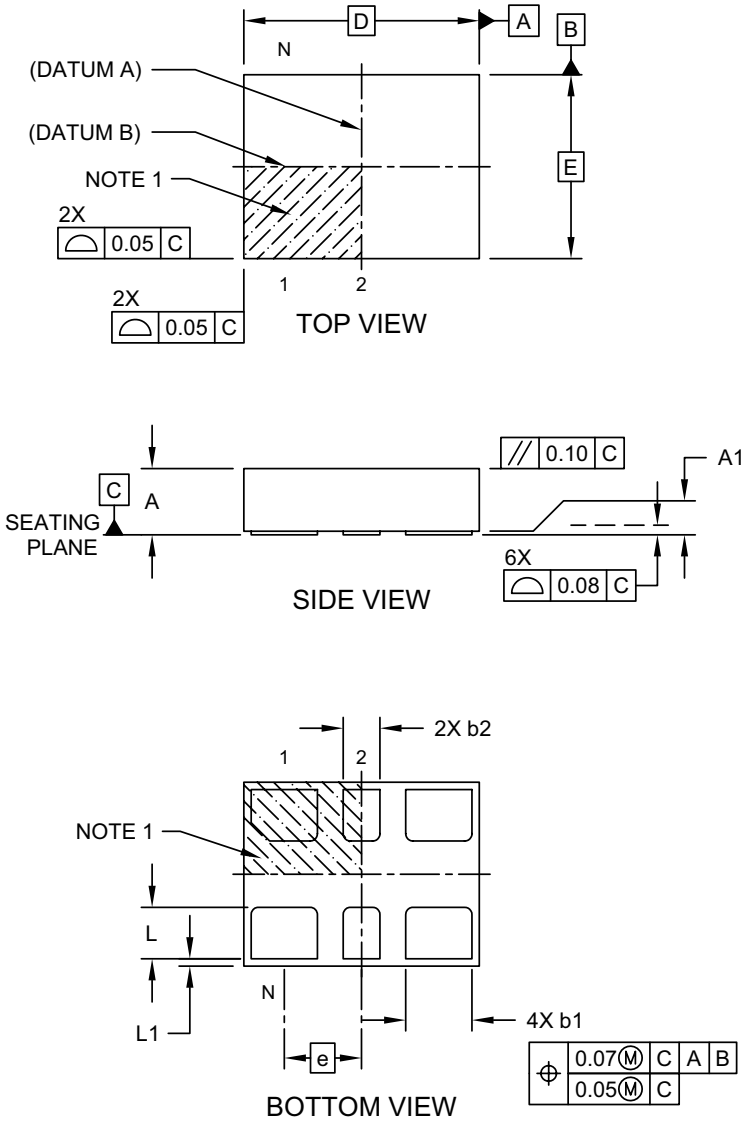
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3005A

6-Lead VDFN 3.2 mm x 2.5 mm Package Outline and Recommended Land Pattern

6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

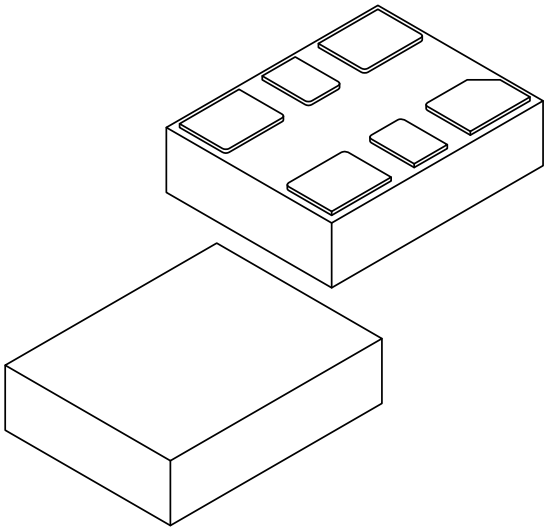
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1007A Sheet 1 of 2

6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		1.05 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D		3.20 BSC	
Overall Width	E		2.50 BSC	
Terminal Width	b1	0.85	0.90	0.95
Terminal Width	b2	0.45	0.50	0.55
Terminal Length	L	0.65	0.70	0.75
Terminal Pullback	L1		0.10 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

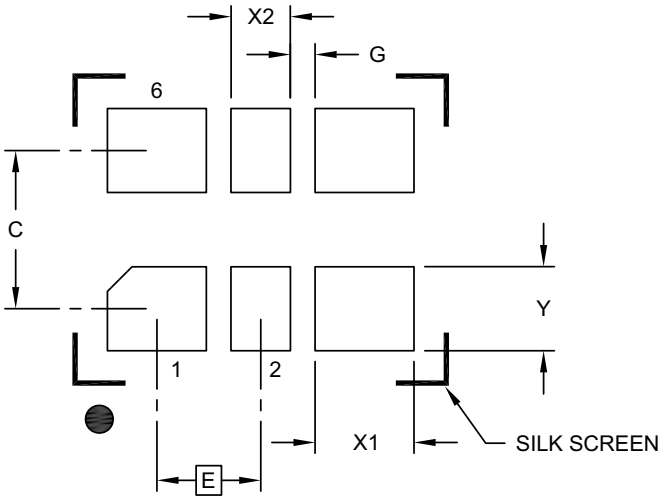
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1007A Sheet 2 of 2

6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.05 BSC		
Contact Pad Spacing	C		1.60	
Contact Pad Width (X4)	X1			1.00
Contact Pad Width (X2)	X2			0.60
Contact Pad Length (X6)	Y			0.85
Space Between Contacts (X4)	G1	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

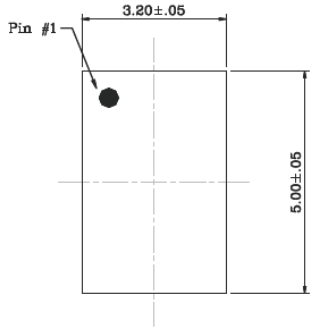
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3007A

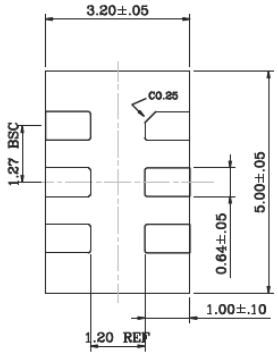
6-Lead CDFN 5.0 mm x 3.2 mm Package Outline and Recommended Land Pattern

TITLE
6 LEAD CDFN 5.0x3.2mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

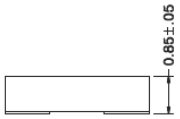
DRAWING #	CDFN5032-6LD-PL-1	UNIT	MM



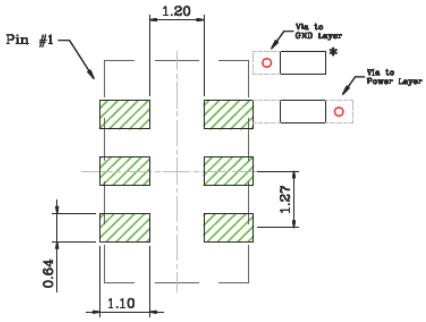
Top View



Bottom View



Side View



Recommended Land Pattern

NOTE:

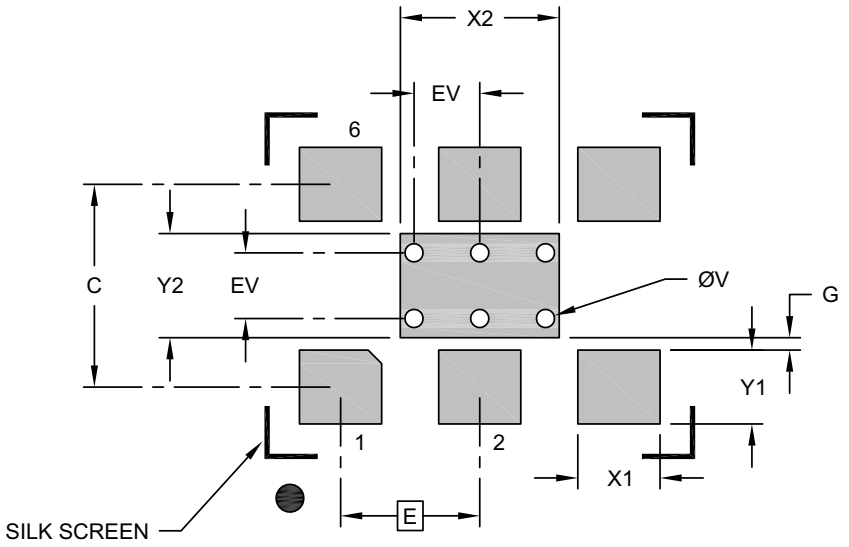
1. * Power Supply Decoupling Capacitor is required in Recommended Land Pattern.
2. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
3. Red circles in Recommended Land Pattern are thermal VIA.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

6-Lead VDFN 7.0 mm x 5.0 mm Package Outline and Recommended Land Pattern

6-Lead Very Thin Plastic Quad Flat, No Lead Package (H8A) - 7x5 mm Body [VDFN] With 2.8x1.8 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		2.54 BSC	
Optional Center Pad Width	X2			2.90
Optional Center Pad Length	Y2			1.90
Contact Pad Spacing	C		3.70	
Contact Pad Width (X6)	X1			1.50
Contact Pad Length (X6)	Y1			1.35
Contact Pad to Center Pad (X2)	G	0.20		
Thermal Via Diameter (X6)	V		0.33	
Thermal Via Pitch	EV		1.20	

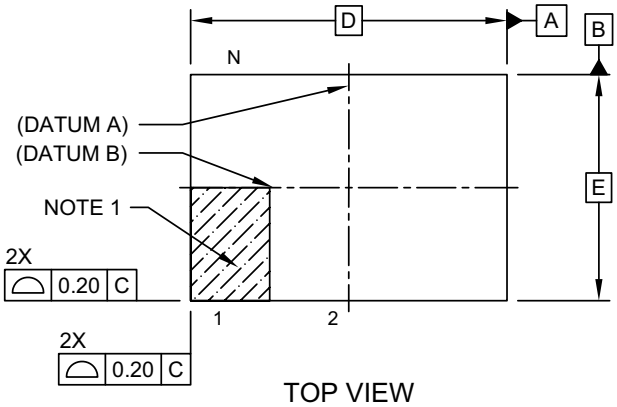
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

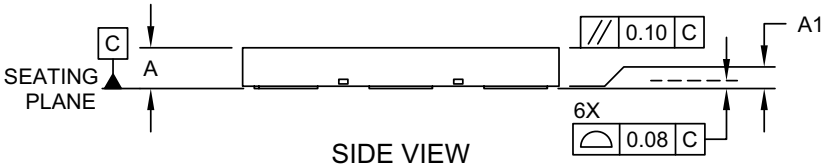
Microchip Technology Drawing C04-3010A

6-Lead Very Thin Plastic Quad Flat, No Lead Package (H8A) - 7x5 mm Body [VDFN] With 2.8x1.8 mm Exposed Pad

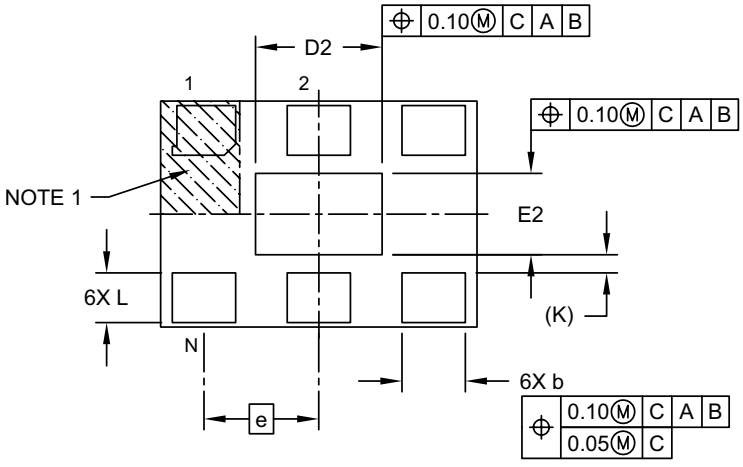
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

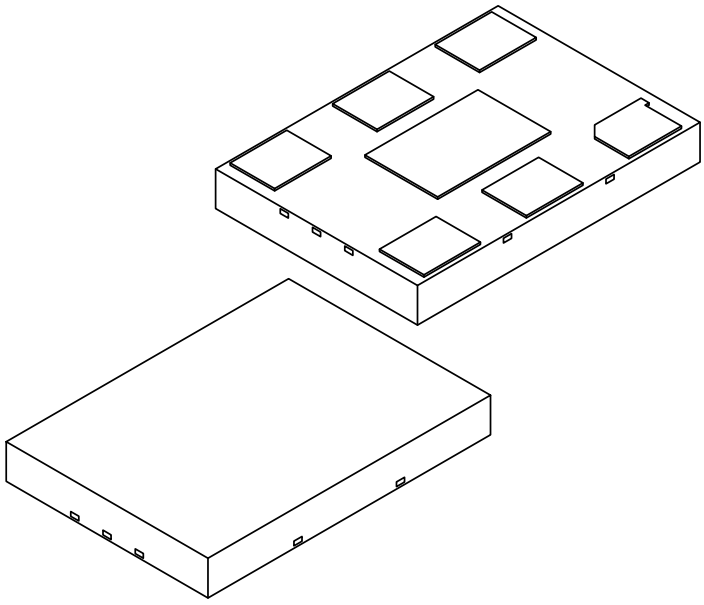


BOTTOM VIEW

Microchip Technology Drawing C04-1010A Sheet 1 of 2

6-Lead Very Thin Plastic Quad Flat, No Lead Package (H8A) - 7x5 mm Body [VDFN] With 2.8x1.8 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		2.54	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D		7.00 BSC	
Exposed Pad Length	D2	2.70	2.80	2.90
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	1.70	1.80	1.90
Terminal Width	b	1.35	1.40	1.45
Terminal Length	L	1.00	1.10	1.20
Terminal-to-Exposed-Pad	K		0.20 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

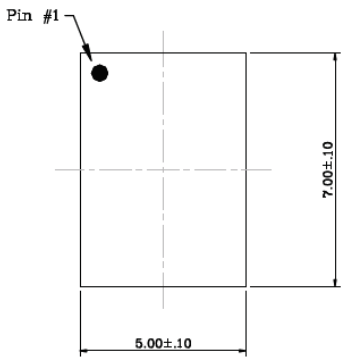
Microchip Technology Drawing C04-1010A Sheet 2 of 2

6-Lead CDFN 7.0 mm x 5.0 mm Package Outline and Recommended Land Pattern

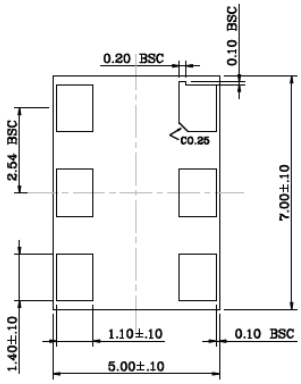
TITLE

6 LEAD CDFN 7.0x5.0mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	CDFN75-6LD-PL-1	UNIT	MM

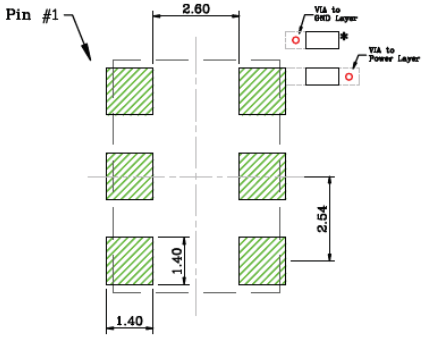


Top View



Bottom View

Side View



Recommended Land Pattern

NOTE:

1. * Power Supply Decoupling Capacitor is required in Recommended Land Pattern.
2. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
3. Red circles in Recommended Land Pattern are thermal VIA.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (December 2017)

- Initial conversion of Micrel document DSC1104/24 to Microchip data sheet template DS20005870A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XXX.XXXX	X
Device	Package	Temperature Range	Stability	Frequency	Packaging Option

Device:	DSC1104:		Low-Jitter Precision HCSL Oscillator with Standby
	DSC1124:		Low-Jitter Precision HCSL Oscillator
Package:	A	=	6-Lead 7.0 mm x 5.0 mm CDFN
	B	=	6-Lead 5.0 mm x 3.2 mm CDFN
	C	=	6-Lead 3.2 mm x 2.5 mm CDFN
	D	=	6-Lead 2.5 mm x 2.0 mm CDFN
	N	=	6-Lead 7.0 mm x 5.0 mm CDFN w/o center pad
Temperature Range:	E	=	–20°C to +70°C (Extended Commercial)
	I	=	–40°C to +85°C (Industrial)
	L	=	–40°C to +105°C (Extended Industrial)
Stability:	1	=	±50 ppm
	2	=	±25 ppm
	3	=	±20 ppm
	5	=	±10 ppm
Frequency:	xxx.xxxx	=	2.3 MHz to 460 MHz (User Defined)
Packing Option:	<blank>	=	Tube
	T	=	1000/Reel

Examples:

a) DSC1104AE1-053.5000: Low Jitter Precision HCSL Oscillator with Standby, 6-Lead 7x5 CDFN, Ext. Commercial Temp. Range, ±50 ppm Stability, 53.5 MHz Frequency, Tube

b) DSC1124BI2-246.8100T: Low Jitter Precision HCSL Oscillator, 6-Lead 5x3.2 VDFN, Industrial Temp. Range, ±25 ppm Stability, 246.81 MHz Frequency, 1000/Reel

c) DSC1104CL5-156.2500: Low Jitter Precision HCSL Oscillator with Standby, 6-Lead 3.2x2.5 VDFN, Ext. Industrial Temp. Range, ±10 ppm Standby, 156.25 MHz Frequency, Tube

d) DSC1124DE3-094.5500T: Low Jitter Precision HCSL Oscillator, 6-Lead 2.5x2.0 CDFN, Ext. commercial Temp. Range, ±20 ppm Stability, 94.55 MHz Frequency, 1000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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