GS12181

12G UHD-SDI Re-timing Cable Driver

Key Features

- Multi-standard operation from 1Mb/s to 11.88Gb/s
- SMPTE ST 2082-1, ST 2081-1, ST 424, ST 292-1 and ST 259 compliant output
- Support for DVB-ASI at 270Mb/s and MADI at 125Mb/s
- Low power operation: approx. 340mW
- Single 1.8V power supply for analog and digital core, 2.5V or 3.3V for output supply
- Differential input support DC-coupling from 1.2V to 2.5V CML logic
- Automatic power down on loss of signal
- Programmable trace equalization to compensate for up to 20" FR4 at 11.88Gb/s
- 75Ω cable driver outputs
  - High levels of pre-emphasis available (up to 8" of FR4) using higher output driver voltage supply
  - Automatic/manual output slew rate control
  - Individually selectable output pre-emphasis to compensate for FR4 losses after chip output at all rates
- Manual Bypass function for low data rates with slow rise/fall times
- Configurable automatic bypass for low data rates
- On-chip 100Ω differential input data termination and 75Ω output termination
- GSPI serial control and monitoring interface
- Four configurable GPIO pins for control or status monitoring
- Wide operating temperature range: -40°C to +85°C
- 6mm x 4mm 40-pin QFN
- Pin compatible with the GS12281, GS12182, GS12081, and GS3281
- Pb-free, Halogen-free, and RoHS/ WEEE-compliant package

Applications

Next Generation 3D / 2D HFR HDTV and 2K D-Cinema, UHDTV1 and 4K D-Cinema end-equipment: Cameras, Monitors, Switchers, etc.

Next Generation 3G, 6G, and 12G UHD-SDI infrastructures designed support of UHDTV2, UHDTV1, 4K D-Cinema and 3D HFR and HDR production image formats.

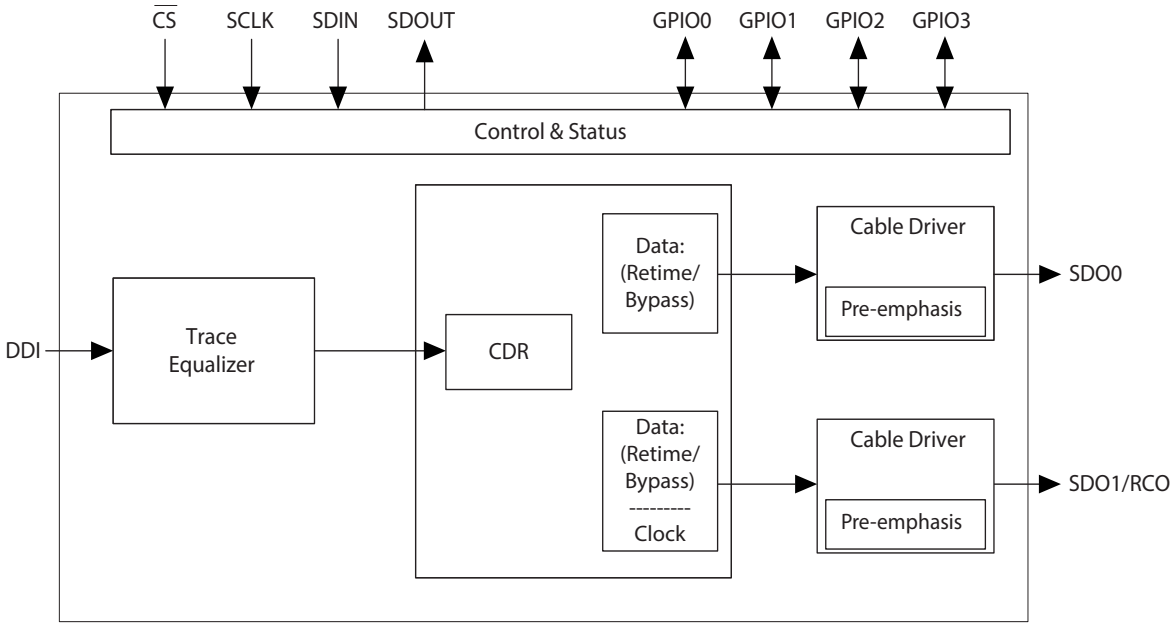
Description

The GS12181 is a low-power, multi-rate, re-timing cable driver supporting rates up to 12G UHD-SDI. It is designed to receive 100Ω differential input signals, automatically recover the embedded clock from the digital video signal and re-time the incoming data, and transmit the re-timed signal over 75Ω coaxial cables.

The device supports SMPTE ST 2082-1 (12G UHD-SDI), ST 2081-1 (6G UHD-SDI), ST 424 (3G SDI), ST 292-1 (HD-SDI) and ST 259 (SD-SDI). Automatic and user selectable output slew rate control is provided for each cable driver output. The device also supports transmission of MADI at 125Mb/s and DVB-ASI.

The GS12181 is pin compatible with the GS12281 single input, and the GS12182 dual input 12G UHD-SDI Multi-rate Re-timing Cable Drivers, the GS12081 12G UHD-SDI Multi-rate Cable Driver, as well as the GS3281 3G SDI Multi-rate Re-timing Cable Driver.

Note: For the GS12181 to be pin compatible with the GS12182, careful design considerations are required. Contact your local Semtech FAE for details.



GS12181 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
6	037849	—	July 2017	Updated Table 1-1: Pins 22,23 corrected so pin numbers match pin names, updated Section 6.1, and added pin compatibility to list of key features.
5	033448	—	October 2016	Update Table 2-1: Input ESD Voltage Updated from 4kV to 2kV.
4	031329	—	June 2016	Converted from Draft to Preliminary Data Sheet.
3	028160	—	October 2015	Correction to document referenced in Section 5. Updated Figure 4-8 and Figure 4-9. Minor updates throughout.
2	026731	—	July 2015	Updated Section 6. and updates throughout the document
1	025090	—	May 2015	Many changes throughout document.
0	022522	—	February 2015	New Document.

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1. Pin Out

1.1 GS12181 Pin Assignment

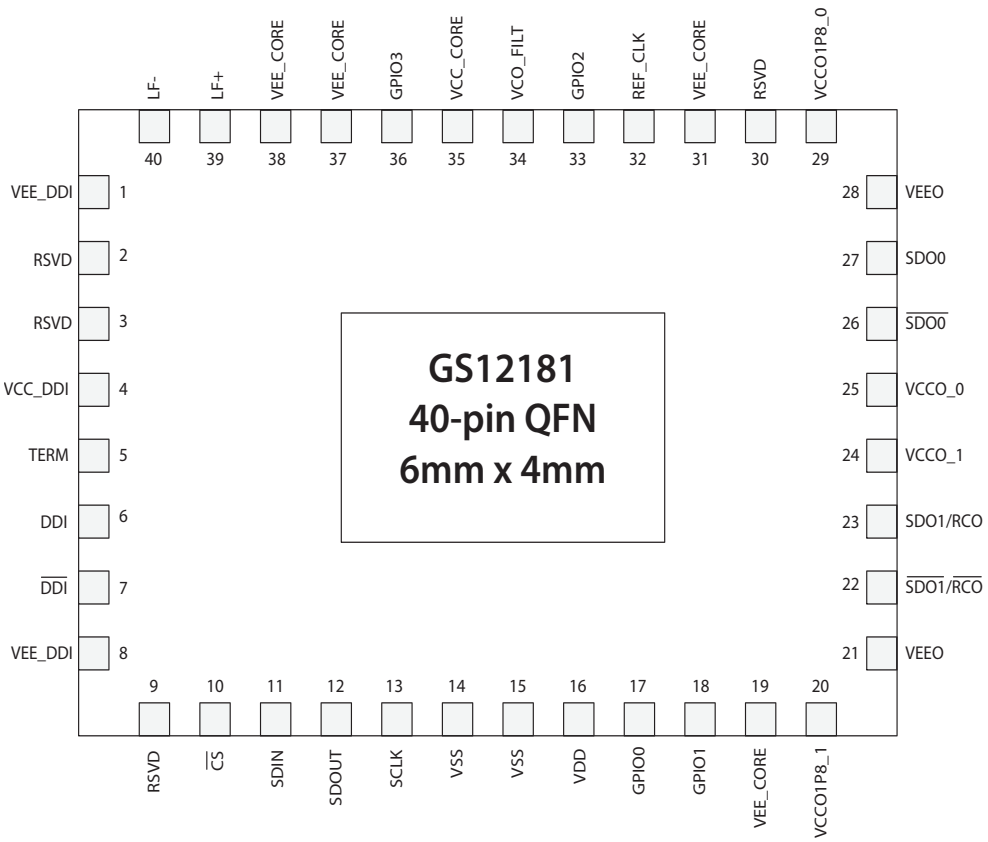


Figure 1-1: GS12181 Pin Out

1.2 GS12181 Pin Descriptions

Table 1-1: GS12181 Pin Descriptions

Pin Number	Name	Type	Description
1, 8	VEE_DDI	Power	Most negative power supply connection for the DDI differential buffer. Connect to GND.
2, 3, 9, 30	RSVD	—	These pins should be left floating. Please contact your Semtech FAE for additional information on circuit compatibility with the GS12090 and GS12281.
4	VCC_DDI	Power	Most positive power supply connection for the DDI differential buffer. Connect to analog supply of 1.8V.

Table 1-1: GS12181 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
5	TERM	—	Input Common Mode termination. Decouple to GND through 10nF capacitor.
6, 7	DDI, $\overline{\text{DDI}}$	Input	Serial digital differential input. Differential CML input with internal 100Ω termination.
10	$\overline{\text{CS}}$	Digital Input	Chip select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-up. Active-low input. Refer to Section 4.5.1 for more details.
11	SDIN	Digital Input	Serial digital data input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.5.2 for more details.
12	SDOUT	Digital Output	Serial digital data output for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS output. Active-high output. Refer to Section 4.5.3 for more details.
13	SCLK	Digital Input	Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.5.4 for more details.
14, 15	VSS	Power	Most negative power supply for digital core logic. Connect to GND.
16	VDD	Power	Most positive power supply connection for the digital core logic. Connect to 1.8V.
17	GPIO0	Digital I/O	Multi-function Control/Status Input/Output 0. Output signal options are: Output driven LOW Output driven HIGH PLL Lock Status LOS (Loss of Signal, inverse of Carrier Detect) (Default) CD (Carrier Detect) SD/$\overline{\text{HD}}$ Status Rate Detected [0] Rate Detected [1] Rate Detected [2] Input signal option is: Output 1 Disable Control Pin is 1.8V CMOS I/O, please refer to GPIO0_CFG for more information on how to configure GPIO0.

Table 1-1: GS12181 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
18	GPIO1	Digital I/O	Multi-function Control/Status Input/Output 1. Output signal options are: Output driven LOW Output driven HIGH PLL Lock Status (Default) LOS (Loss of Signal, inverse of Carrier Detect) CD (Carrier Detect) SD/$\overline{\text{HD}}$ Status Rate Detected [0] Rate Detected [1] Rate Detected [2] Reference Clock (Only applicable to GPIO_1) Input signal option is: Output 1 Disable Control Pin is 1.8V CMOS I/O, please refer to GPIO1_CFG for more information on how to configure GPIO1.
19, 31, 37, 38	VEE_CORE	Power	Most negative power supply connection for the analog core. Connect to GND.
20	VCCO1P8_1	Power	Most positive power supply connection for cable driver 1 pre driver. Connect to 1.8V.
21, 28	VEEO	Power	Most negative power supply connection for the output drivers. Connect to GND.
22, 23	$\overline{\text{SDO1}}$/$\overline{\text{RCO}}$, SDO1/RCO	Output	Serial digital output signals for cable driver 1. Differential CML output with two internal 75Ω pull-ups. If only SDO1 is used as an active output, connect $\overline{\text{SDO1}}$ to GND through 4.7µF capacitor and 75Ω resistor. If both outputs are unused, they can be left floating and disabled through the host interface.
24	VCCO_1	Power	Most positive power supply connection for cable driver 1. Connect to 1.8V, 2.5V or 3.3V.
25	VCCO_0	Power	Most positive power supply connection for cable driver 0. Connect to 1.8V, 2.5V or 3.3V.
26, 27	$\overline{\text{SDO0}}$, SDO0	Output	Serial digital output signals for cable driver 0. Differential CML output with two internal 75Ω pull-ups. If onlySDO0 is used as an active output, connect $\overline{\text{SDO0}}$ to GND through 4.7µF capacitor and 75Ω resistor. If both outputs are unused, they can be left floating and disabled through the host interface.
29	VCCO1P8_0	Power	Most positive power supply connection for cable driver 0 pre driver. Connect to 1.8V.
32	REF_CLK	Digital Input	Optional 27MHz reference input. For details see Section 4.2. 1.8V CMOS input with 100kΩ pull-down.

Table 1-1: GS12181 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
33	GPIO2	Digital I/O	Multi-function Control/Status Input/Output 2. Output signal options are: Output driven LOW Output driven HIGH PLL Lock Status LOS (Loss of Signal, inverse of Carrier Detect) CD (Carrier Detect) SD/$\overline{\text{HD}}$ Status Rate Detected [0] Rate Detected [1] Rate Detected [2] Input signal option is: Output 1 Disable Control **Note:** The default signal option is not active on this version of the device, but will be Sleep control on future devices. Pin is 1.8V CMOS I/O, please refer to GPIO2_CFG for more information on how to configure GPIO2.
34	VCO_FILT	Passive	VCO filter capacitor connection. Decouple to ground through 1µF capacitor.
35	VCC_CORE	Power	Most positive power supply connection for the analog core. Connect to 1.8V.
36	GPIO3	Digital I/O	Multi-function Control/Status Input/Output 3. Output signal options are: Output driven LOW Output driven HIGH PLL Lock Status LOS (Loss of Signal, inverse of Carrier Detect) CD (Carrier Detect) SD/$\overline{\text{HD}}$ Status Rate Detected [0] Rate Detected [1] Rate Detected [2] Input signal option is: Output 1 Disable Control (Default) Pin is 1.8V CMOS I/O, please refer to GPIO3_CFG for more information on how to configure GPIO3.
39	LF+	Passive	Loop filter capacitor connection. Connect to pin 40 through 470nF capacitor.
40	LF-	Passive	Loop filter capacitor connection. Connect to pin 39 through 470nF capacitor.
Tab	—	—	Central paddle can be connected to ground or left unconnected. Its purpose is to provide increased mechanical stability. It is not required for thermal dissipation.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage - Core (VCC_DDI, VCC_CORE, VDD, VCCO1P8_0, VCCO1P8_1)	-0.5V to +2.2V
Supply Voltage - Output Driver (VCCO_0, VCCO_1)	-0.5V to +3.65V
Input ESD Voltage (any pin)	2kV HBM
Storage Temperature Range (T_S)	-50°C to 125°C
Input Voltage Range (DDI, $\overline{DDI}$)	-0.3 to 2.625V
Input Voltage Range (GPIO2, GPIO3, REF_CLK)	-0.3 to (VCC_CORE +0.3)V
Input Voltage Range ($\overline{CS}$, SDIN, SCLK, GPIO0, GPIO1)	-0.3 to (VDD +0.3)V
Solder Reflow Temperature	260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC/DC electrical characteristics tables is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

VCC_DDI, VCC_CORE, VDD, VCCO1P8_0, VCCO1P8_1 = +1.8V ±5%, VCCO_0, VCCO_1 = +2.5V ±5%, TA = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	VCC_DDI, VCC_CORE, VDD, VCCO1P8_0, VCCO1P8_1		1.71	1.8	1.89	V	—
Supply Voltage - Output Driver	VCCO_0, VCCO_1	VCCO = 1.8V	1.71	1.8	1.89	V	1
		VCCO = 2.5V	2.38	2.5	2.63	V	1
		VCCO = 3.3V	3.14	3.3	3.47	V	1
Power	P_D	SDO0/$\overline{SDO0}$ enabled, SDO1/$\overline{SDO1}$ disabled Output Swing = 800mV$_{pp}$	—	340	—	mW	—
		SDO0/$\overline{SDO0}$ enabled, SDO1/$\overline{SDO1}$ disabled Output Swing = 800mV$_{pp}$ with max pre-emphasis	—	355	—	mW	—
		SDO0/$\overline{SDO0}$ and SDO1/$\overline{SDO1}$ enabled Output Swing = 800mV$_{pp}$	—	430	—	mW	—
		SDO0/$\overline{SDO0}$ and SDO1/$\overline{SDO1}$ enabled Output Swing = 800mV$_{pp}$ with max pre-emphasis	—	445	—	mW	—
		SDO0/$\overline{SDO0}$ and SDO1/$\overline{SDO1}$ disabled	—	250	—	mW	—
Supply Current – Analog Core	I_{CC_CORE}	—	—	110	132	mA	—
Supply Current – Trace Equalizer	I_{CC_DDI}	—	—	15	19	mA	—
Supply Current – Digital Logic	I_{DD}	—	—	14	18	mA	—
Supply Current – Cable Driver	I_{CCO_0} ,I_{CCO_1}	VCCO = 3.3V, Output Swing = 800mV$_{pp}$	—	22	30	mA	—
		VCCO = 3.3V, Output Swing = 800mV$_{pp}$ with max pre-emphasis	—	29	37	mA	—
	I_{CCO1P8_0}, $I_{CCO\_1P8\_1}$	Output Swing = 800mV$_{pp}$	—	20	—	mA	—
Serial Input Common Mode Voltage	V_{CMIN}	—	0.94	1.6	2.525	V	2

Table 2-2: DC Electrical Characteristics (Continued)

VCC_DDI, VCC_CORE, VDD, VCCO1P8_0, VCCO1P8_1 = +1.8V ±5%, VCCO_0, VCCO_1 = +2.5V ±5%, TA = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input Termination		Differential	—	100	—	Ω	—
Serial Output Termination		—	—	75	—	Ω	—
Input Voltage - Digital Pins ($\overline{CS}$, SDIN, SCLK, GPIO[0:3])	V_{IH}	—	0.65* VDD	—	VDD	V	—
	V_{IL}	—	0	—	0.35* VDD	V	—
Output Voltage - Digital Pins (SDOUT, GPIO[0:3])	V_{OH}	I_{OH} = -5mA	VDD - 0.45	—	—	V	—
	V_{OL}	I_{OL} = +5mA	—	—	0.45	V	—

Notes:

1. Single 1.8V supply operation is possible, but the output eye is not guaranteed to be SMPTE compliant across all operating conditions. It is recommended to run VCCO_0/VCCO_1 in the range 2.5-3.3V for guaranteed SMPTE compliance.
2. In DC-coupled mode the trace equalizer can sink/source current from/to the upstream driver.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

VCC_DDI, VCC_CORE, VDD, VCCO1P8_0, VCCO1P8_1 = +1.8V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input Data Rate	DR_{DDI}	—	0.001	—	11.88	Gb/s	—
Input Voltage Swing	ΔV_{DDI}	—	200	—	800	mV_{ppd}	—
Intrinsic Input Jitter Tolerance	I_{IJT}	12G	0.7	0.85	—	UI	1
		MADI/SD/HD/3G/6G	0.8	0.95	—	UI	1
Output Return Loss	ORL	5MHz to 1.485GHz	—	—	-17	dB	—
		1.485GHz to 2.97GHz	—	—	-12	dB	—
		2.97GHz to 5.94GHz	—	—	-8	dB	—
		5.94GHz to 11.88GHz	—	—	-5	dB	—
Output Voltage Swing	ΔV_{SDO}	OUTPUT_SWING	720	800	880	mV_{pp}	—
PLL Lock Time – Asynchronous	t_{ALOCK}	Referenceless with MADI Out	—	—	16.7	ms	2
		Referenceless with MADI In	—	—	32	ms	2
PLL Lock Time– Synchronous	t_{SLOCK}	SD	—	—	10	µs	—
		HD/3G/UHD	—	—	2	µs	—
SDO0, $\overline{SDO0}$, SDO1, $\overline{SDO1}$ Rise/Fall Time	$t_{riseSDO0}/t_{fallSDO0}$, $t_{fallSDO1}/t_{fallSDO1}$	SD	400	—	1000	ps	—
		HD/3G/UHD	—	—	40	ps	—
Mismatch in Rise/Fall Time		SD	—	—	25	ps	—
		HD/3G/UHD	—	—	5	ps	—

Table 2-3: AC Electrical Characteristics (Continued)

VCC_DDI, VCC_CORE, VDD, VCCO1P8_0, VCCO1P8_1 = +1.8V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Eye Cross Shift (SDO0, $\overline{SDO0}$, SDO1, $\overline{SDO1}$)		12G	—	—	9	%	—
		MADI/SD/HD/3G/6G	—	—	5	%	—
Overshoot		—	—	—	10	%	—
Intrinsic Serial Data Output Jitter	$t_{OJ(125Mb/s)}$	BW = default, Pattern = PRBS	—	0.015	0.08	UI_{pp}	—
	$t_{OJ(270Mb/s)}$		—	0.02	0.08	UI_{pp}	—
	$t_{OJ(1.485Gb/s)}$		—	0.02	0.08	UI_{pp}	—
	$t_{OJ(2.97Gb/s)}$		—	0.03	0.08	UI_{pp}	—
	$t_{OJ(5.94Gb/s)}$		—	0.03	0.08	UI_{pp}	—
	$t_{OJ(11.88Gb/s)}$		—	0.09	0.16	UI_{pp}	—
	$t_{OJ(Bypass)}$		—	0.13	0.20	UI_{pp}	2
PLL Loop Bandwidth	$BW_{LOOP(125Mb/s)}$	Setting 0.0625x	—	5	—	kHz	—
		Setting 0.125x	—	10	—	kHz	—
		Setting 0.25x	—	19	—	kHz	—
		Setting 0.5x (Default)	—	38	—	kHz	—
		Setting 1x	—	75	—	kHz	—
	$BW_{LOOP(270Mb/s)}$	Setting 0.0625x	—	10	—	kHz	—
		Setting 0.125x	—	20	—	kHz	—
		Setting 0.25x	—	40	—	kHz	—
		Setting 0.5x	—	80	—	kHz	—
		Setting 1x (Default)	—	158	—	kHz	—
	$BW_{LOOP(1.485Gb/s)}$	Setting 0.0625x	—	55	—	kHz	—
		Setting 0.125x	—	110	—	kHz	—
		Setting 0.25x	—	220	—	kHz	—
		Setting 0.5x (Default)	—	438	—	kHz	—
		Setting 1x	—	875	—	kHz	—
	$BW_{LOOP(2.97Gb/s)}$	Setting 0.0625x	—	110	—	kHz	—
		Setting 0.125x	—	220	—	kHz	—
		Setting 0.25x	—	440	—	kHz	—
		Setting 0.5x (Default)	—	0.88	—	MHz	—
		Setting 1x	—	1.75	—	MHz	—

Table 2-3: AC Electrical Characteristics (Continued)

VCC_DDI, VCC_CORE, VDD, VCCO1P8_0, VCCO1P8_1 = +1.8V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
PLL Loop Bandwidth	$BW_{LOOP(5.94Gb/s)}$	Setting 0.0625x	—	220	—	kHz	—
		Setting 0.125x	—	440	—	kHz	—
		Setting 0.25x	—	0.88	—	MHz	—
		Setting 0.5x (Default)	—	1.75	—	MHz	—
		Setting 1x	—	3.5	—	MHz	—
	$BW_{LOOP(11.88Gb/s)}$	Setting 0.0625x	—	440	—	kHz	—
		Setting 0.125x	—	0.88	—	MHz	—
		Setting 0.25x	—	1.75	—	MHz	—
		Setting 0.5x (Default)	—	3.5	—	MHz	—
		Setting 1x	—	7.0	—	MHz	—

Notes:

1. Square-wave modulated jitter
2. Measured using a clean input source.

3. Input/Output Circuits

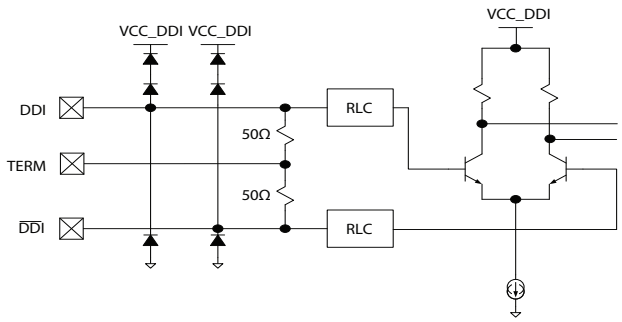


Figure 3-1: DDI, $\overline{\text{DDI}}$

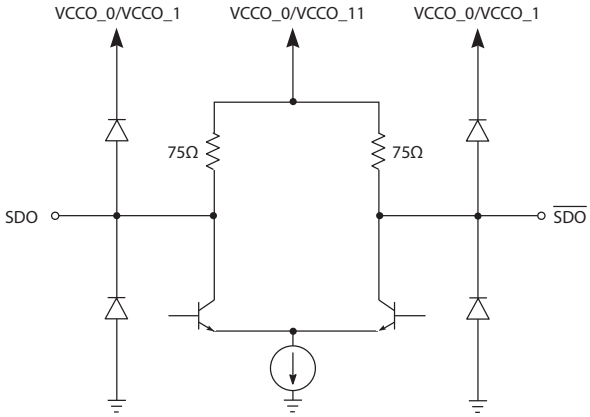


Figure 3-2: SDO0, $\overline{\text{SDO0}}$, SDO1, $\overline{\text{SDO1}}$ Serial Data Output

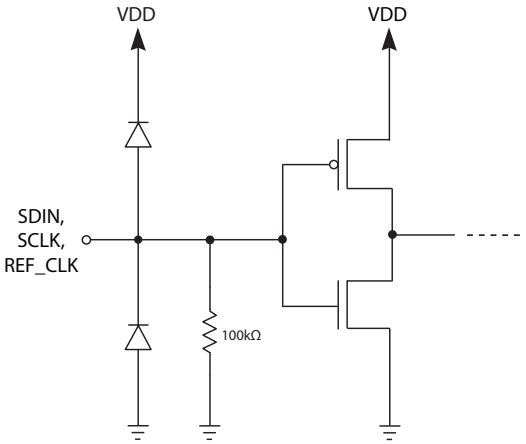


Figure 3-3: SDIN and SCLK, REF_CLK

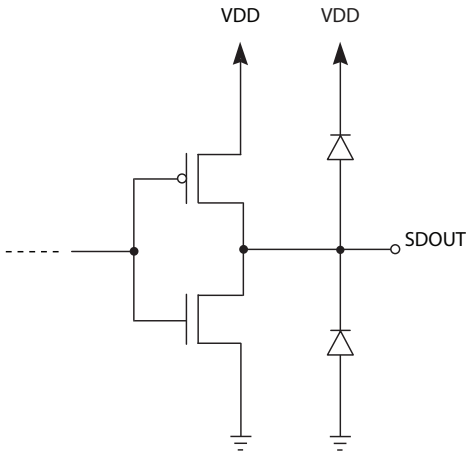


Figure 3-4: SDOUT

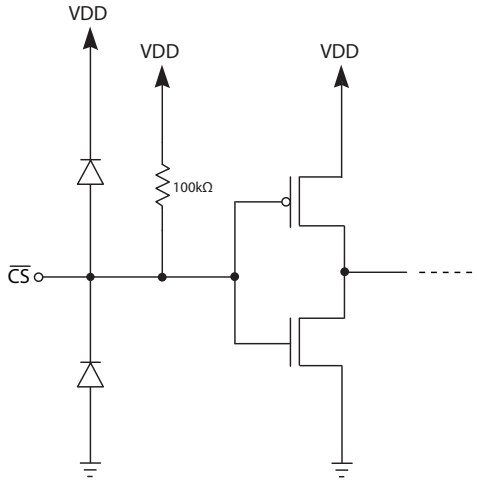


Figure 3-5: $\overline{\text{CS}}$

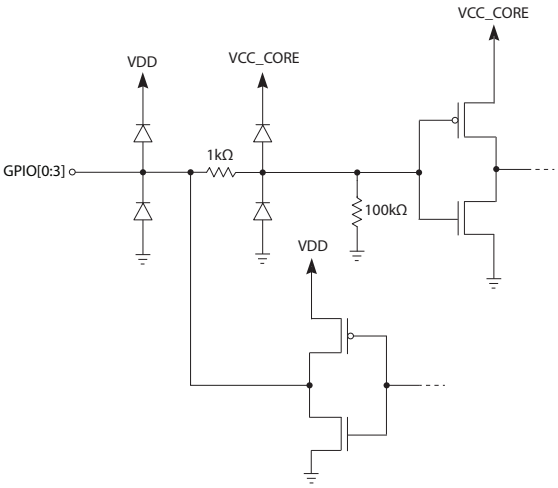


Figure 3-6: GPIO[0:3]

4. Detailed Description

4.1 Trace Equalizer

The GS12181 features a differential input buffer with 100Ω differential input termination, which includes a trace equalizer that can be configured to compensate for up to 17dB of insertion loss at 5.94GHz in microstrip or stripline differential trace.

The differential input signal can be either DC-coupled or AC-coupled and is capable of operation with any binary coded signal between 1Mb/s and 11.88Gb/s.

The input circuit is compatible with industry standard CML differential transmitters when DC-coupled using 100Ω differential termination circuitry.

4.1.1 Input Trace Equalization

The trace equalizer can compensate for up to 17dB of insertion loss at 5.94GHz in 6 increments, which can be adjusted through the **CFG_TREQ_BOOST** parameter in control register 0x731E. The default value of **CFG_TREQ_BOOST** is (0_h), which corresponds to the minimum equalization boost level.

Please refer to Figure 4.1 and Table 4-1 for recommended boost setting.

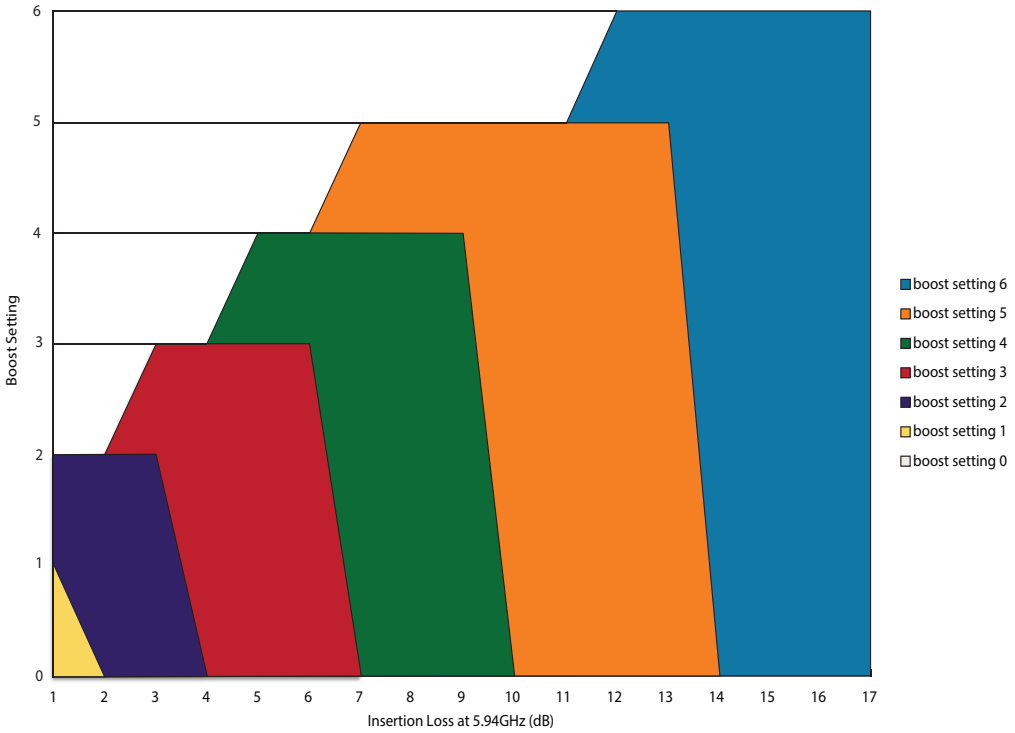


Figure 4-1: GS12181 Trace EQ Boost Setting Recommendation

Note: Launch swing of 200mVppd used for insertion loss <4dB. Launch swing of 800mVppd use for insertion loss >4dB.

Table 4-1: Insertion Loss Per Boost Setting

Insertion Loss at 5.94GHz (dB)	Boost Setting
1 - 2	1
2 - 4	2
4 - 7	3
7 - 10	4
10 - 14	5
14 - 17	6

By default at power up or after system reset, the trace equalizer is configured to compensate for up to 3" of 7-mil stripline in FR4 material at high frequencies.

Note: Although not a requirement, launch swing of 800mV$_{ppd}$ is recommended for trace lengths longer than 5".

4.1.2 CD (Carrier Detect) and LOS (Loss of Signal)

LOS is the complement of CD and is used by various automatic control modes including Mute on LOS and Disable on LOS, which will be covered in the output section of this document.

The default settings of the Carrier Detection sub-block should satisfy most applications; however the Carrier Detection mechanism in the GS12181 is highly configurable and allows the system designer to optimize the sensitivity and hysteresis of Carrier Detect to meet specific system requirements.

The Carrier Detect is reported by status parameter **STAT_PRI_CD** in register 0x7387.

One of the CD control parameters is **CFG_TREQ_CD_BOOST** in register 0x731E. This parameter determines the method and therefore the level of equalization to be used on the input signal routed to the Carrier Detection sub-block. The default value is 0_b, which maximizes the level of equalization. Alternatively, the designer can choose to have this signal equalized at the same level as the main signal routed to the CDR by setting **CFG_TREQ_CD_BOOST** to 1_b. The setting of this parameter has no impact on the main signal routed to the CDR.

The last two CD control parameters can be found in register 0x731F. Parameters **CFG_TREQ_CD_ASSERT_THRESH** and **CFG_TREQ_CD_DEASSERT_THRESH** set the Carrier Detect assert and de-assert thresholds to the input signal, which also defines the hysteresis of CD signal.

The default values of **CFG_TREQ_CD_ASSERT_THRESH** and **CFG_TREQ_CD_ DEASSERT_THRESH** are 4_d and 3_d respectively. With the default settings, the minimum launch swing needed to assert the Carrier Detect is 200mV and it will be de-asserted when the signal level falls below 150mV.

The **STAT_PRI_CD** (Carrier Detect) parameter will be set to 0_b and the LOS will be set to 1_b whenever a new signal at the input does not exceed the assert threshold, or an existing signal falls below the de-assert threshold. The result is that the device will not indicate lock, and the outputs will mute assuming Mute on LOS is left to its default value in the **CONTROL_OUTPUT_MUTE** register (0x7349). See Section 4.3 for more details.

Given a board that is routed with up to 20" of 7-mil stripline in FR4 and CFG_TREQ_CD_BOOST = 0_b, Figure 4-2 illustrates the relationship between launch swing voltage, and minimum threshold setting to assert or de-asset Carrier Detect at all rates up to 11.88Gb/s.

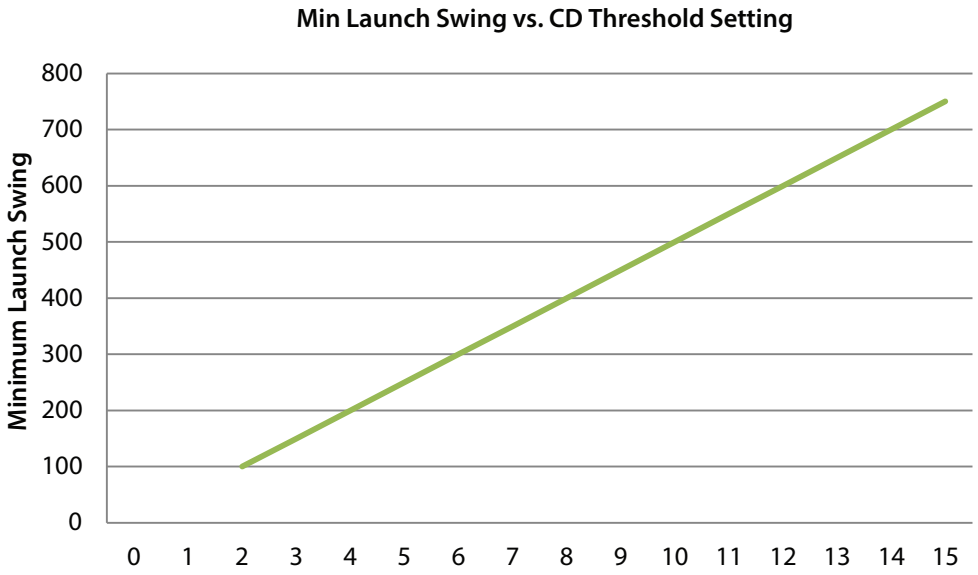


Figure 4-2: Min Launch Swing Vs. CD Threshold Setting

4.1.3 Equalizer Control and Status Parameters Summary

The following two tables list the most commonly used control and status parameters of the Equalizer block. For a complete list of registers and functions, please see Section 5.

Table 4-2: Equalizer Block Control Parameters

Address$_h$	Bit Slice	Parameter Name	Description
0x731E	3:1	CFG_TREQ_BOOST	Sets the Trace Equalizer boost level.
	0:0	CFG_TREQ_CD_BOOST	Selects the boost method of the CD signal.
0x731F	7:4	CFG_TREQ_CD_ASSERT_THRESH	Sets the Carrier Detect assert threshold.
	3:0	CFG_TREQ_CD_DEASSERT_THRESH	Sets the Carrier Detect de-assert threshold.

Table 4-3: Equalizer Block Status Registers

Address$_h$	Bit Slice	Parameter Name	Description
0x7384	15:8	STAT_CNT_PRI_CD_CHANGES	A counter showing the number of times the primary Carrier Detect signal changed.
0x7387	8:8	STAT_PRI_CD	The primary Carrier Detect status.

4.2 Serial Digital Re-timer (CDR)

The GS12181 includes an integrated CDR, whose purpose is to lock to a valid incoming signal from the trace equalizer stage and produce a lower jitter signal at the cable driver outputs SDO0 and SDO1. The CDR will attempt to lock to any of the following data rates: MADI (125Mb/s), SD-SDI (270Mb/s), HD-SDI (1.485Gb/s), 3G-SDI (2.97Gb/s), 6G-SDI (5.94Gb/s) and 12G-SDI (11.88Gb/s). This includes the f/1.001 rates.

The default settings of the re-timer block are optimal for most applications. However, the following controls allow the user to customize the behaviour of the re-timer: LBW control, Automatic and Manual Rate Detection, and External Reference Clock Mode.

4.2.1 PLL Loop Bandwidth Control

The ratio of output peak-to-peak jitter to input peak-to-peak jitter of the CDR can be represented by a low-pass jitter transfer function, with a bandwidth equal to the PLL LBW. Although the default LBW settings for the GS12181 CDR are ideal for most SDI signals, the GS12181 allows the user to adjust the LBW for MADI and each SMPTE compliant rate.

Registers 0x730A through 0x730C contain the following parameters which allow the user to configure rate dependent LBW: **CFG_PLL_LBW_12G**, **CFG_PLL_LBW_6G**, **CFG_PLL_LBW_3G**, **CFG_PLL_LBW_HD**, **CFG_PLL_LBW_SD**, and **CFG_PLL_LBW_MADI**. The LBW settings are defined in terms of ratios of the nominal LBW. For each rate, where '1.0x' is the nominal LBW, the following ratios are available: 0.0625x, 0.125x, 0.25x, 0.5x, and 1.0x. Table 2-3 provides the specific loop bandwidths for each data rate and LBW setting. Lowering the LBW will lower the jitter amplitude above the LBW frequency. Although lower output jitter is desirable, the lower LBW may reduce the device's IJT to very high jitter that may be present outside the LBW.

4.2.2 Automatic and Manual Rate Detection

With the default rate detect setting, the CDR will automatically attempt to lock to any of following data rates: MADI (125Mb/s), SD-SDI (270Mb/s), HD-SDI (1.485Gb/s), 3G-SDI (2.97Gb/s), 6G-SDI (5.94Gb/s) and 12G-SDI (11.88Gb/s). This includes the f/1.001 rates. However, the CDR can be forced to only lock to a single rate by setting the **CFG_AUTO_RATE_DETECT_ENA** and **CFG_MANUAL_RATE** parameters in register 0x7306 to 0_b and 1_b respectively. With automatic rate detection enabled (**CFG_AUTO_RATE_DETECT_ENA** = 1), specific rates can be excluded from the rate detect list through the **CFG_RATE_ENA_<r>** rate disable mask parameter in 0x7306, where r is the rate to be disabled.

The **STAT_LOCK** parameter in register 0x7386 will indicate that the CDR is locked when its value is 1_b and unlocked when its value is 0_b. The lock status can also be monitored externally on GPIO1, which is the default power-up configuration for pin 18. The **STAT_DETECTED_RATE** parameter in register 0x7387 will indicate the data rate at which the CDR is locked to. A value of 0_d in the **STAT_DETECTED_RATE** parameter indicates that the device is not locked, while values between 1_d and 6_d will indicate that the device is locked to one of the six available rates between MADI at 125Mb/s and UHD-SDI at 11.88Gb/s.

Table 4-4: Detected Data Rates

STAT_DETECTED _RATE[2:0]	Detected Data Rate
0	Unlocked
1	MADI (125Mb/s)
2	SD (270Mb/s)
3	HD (1.485Gb/s)
4	3G (2.97Gb/s)
5	6G (5.94Gb/s)
6	12G (11.88Gb/s)
7	Reserved

If the CDR cannot lock to any of the valid rates in automatic mode or the selected rate in manual mode, the non re-timed signal from the trace EQ block will automatically be bypassed to the output. If the CDR does lock to the incoming signal, the re-timed and bypassed (if manual bypass control enabled) signals are available independently at each output. See the Output Driver Section 4.3.1 for more details.

4.2.3 Lock Time and External Reference Clock

4.2.3.1 Synchronous and Asynchronous Lock Time

Synchronous lock time is defined as the time it takes the device to re-lock to an existing signal that has been momentarily interrupted or to a new signal of the same data rate as the previous signal which has been quickly switched in.

Asynchronous lock time is defined as the time it takes the device to lock when a signal is first applied to the serial digital inputs, or when the signal rate changes. The asynchronous lock time can be reduced by using an external reference clock. See Section 4.2.3.2 for more details.

The asynchronous and synchronous lock times are defined in Table 2-3.

Note: To ensure synchronous lock times are met, the maximum interruption time of the signal is 10µs for an SD SDI signal. HD, 3G, 6G, or 12G signals must have a maximum interruption time of 6µs. The new signal, after interruption, must have the same frequency as the original signal but may have an arbitrary phase.

4.2.3.2 External Reference Clock

The GS12181 does not require an external reference clock. However, if asynchronous lock times shorter than those in Table 2-3 are required, an external clock can be supplied on the REF_CLK (pin 32). For faster asynchronous lock times, an external 27MHz ±100ppm clock source is recommended.

If the application is multi-channel in nature, and several GS121xx devices are adjacent to each other, a single external reference can drive up to eight GS121xx devices by daisy chaining the REF_CLOCK buffers of all the devices. The GS121x devices can be set to provide a buffered output of the external reference clock reference only on GPIO1 (pin 18), allowing each device to be the REF_CLOCK source for the next device in the chain.

To use an external reference, set the **CFG_REF_CLK_MODE_MANUAL** parameter to 0_b in register 0x7308.

To output a buffered version of the reference clock to the next device in the chain, set the **CFG_GPIO1_OUTPUT_ENA** and **CFG_GPIO1_FUNCTION** parameters in register 0x7311 to 1_b and 87_d respectively.

4.2.3.3 CDR Control and Status Parameters Summary

Table 4-5 and Table 4-6 list the most commonly used control and status parameters of the CDR block. For a complete list of registers and functions, please see Section 5.

Table 4-5: CDR Control Parameters

Address$_h$	Bit Slice	Parameter Name	Description
0x7306	13:8	CFG_RATE_ENA_<r>	Specific rate disable mask, where r is the rate to be disabled.
	4:1	CFG_MANUAL_RATE	Select a single rate for CDR rate detection when **CFG_AUTO_RATE_DETECT_ENA** is 0_b.
	0:0	CFG_AUTO_RATE_DETECT_ENA	Sets or disables the automatic rate detection mode of the CDR.
0x7308	1:1	CFG_REF_CLK_MODE_MANUAL	Sets or disables external reference clock mode.
0x730A	12:8	CFG_PLL_LBW_12G	Set the LBW for 12G signals.
	4:0	CFG_PLL_LBW_6G	Set the LBW for 6G signals.
0x730B	12:8	CFG_PLL_LBW_3G	Set the LBW for 3G signals.
	4:0	CFG_PLL_LBW_HD	Set the LBW for HD signals.
0x730C	12:8	CFG_PLL_LBW_SD	Set the LBW for SD signals.
	4:0	CFG_PLL_LBW_MADI	Set the LBW for MADI signals.
0x7311	8:8	CFG_GPIO1_OUTPUT_ ENA	Sets the GPIO pin as either an output or an input.
	7:0	CFG_GPIO1_FUNCTION	Sets or disables buffered reference clock output on GPIO1.

Table 4-6: CDR Status Parameters

Address$_h$	Bit Slice	Parameter Name	Description
0x7385	15:8	STAT_CNT_RATE_CHANGES	Counter showing the number of times the PLL lock rate changed.
	7:0	STAT_CNT_PLL_LOCK_CHANGES	Counter showing the number of times the PLL lock status changed.
0x7386	12:12	STAT_LOCK	The status of the PLL. Locked, or unlocked.
0x7387	2:0	STAT_DETECTED_RATE	The rate at which the PLL is locked to.

4.3 Output Cable Drivers

The GS12181 features two independent internally terminated differential cable drivers (see Figure 3-2), with data available on the first output, SDO0, while clock and data are available on the second output, SDO1. Although SDO0 and SDO1 are differential buffers, they can be implemented as 4 SMPTE compliant 75Ω single-ended drivers. However, if the inverted signal on $\overline{SDO0}$ and $\overline{SDO1}$ are not used, those outputs should be terminated through a 75Ω resistor and 4.7µF capacitor to GND. The cable drivers feature highly configurable amplitude and pre-emphasis control, which can compensate for up to 8 inches of 10mil microstrip in standard FR4 at 11.88Gb/s. The LOS (Loss of Signal) status from the input stage and Loss of Lock status from the CDR block can both be used to automatically mute or disable the outputs when asserted.

4.3.1 Bypassed Re-timer Signal Output Control

With the default power-up settings, the GS12181 outputs will automatically switch to the bypassed signal (non-re-timed) whenever the PLL is unlocked. Alternatively, manual re-timer bypass may be configured by setting the **CTRL_OUTPUT<n>_RETIMER_AUTO_BYPASS** and **CTRL_OUTPUT<n>_RETIMER_MANUAL_BYPASS** parameters in register 0x734C to 0_b and 1_b respectively, in which case the PLL will remain bypassed for all rates.

The re-timer bypass function, manual or automatic, does not affect the input equalization function of the device.

In manual bypass, the output signals of the device will not be retimed. Other features of the re-timer such as rate detect and lock detect are still accessible in this mode.

Please refer to Section 5. on how to change the re-timer bypass mode via the device's host interface.

4.3.2 Clock Out on SDO1

The GS12181 provides an optional clock output mode on SDO1. The clock is half of the detected data rate.

To set SDO1 to clock mode, write 1_b to parameter **CTRL_OUTPUT1_SIGNAL_SEL** in register 0x7348. The default value of this bit is 0_b (data mode).

4.3.3 Output Driver Polarity Inversion

The signal polarity may be inverted at the outputs through the **CTRL_OUTPUT<n>_DATA_ INVERT** parameters in register 0x7348. This may be useful to compensate for an inverted upstream signal or to facilitate board signal routing.

To invert the polarity of either of the two output drivers, write 1_b to control parameter **CTRL_OUTPUT<n>_DATA_ INVERT**.

4.3.4 Amplitude and Pre-emphasis Control

Each output signal pair can be configured in ≈20mV_{p-p} increments to drive up to 1200V_{p-p} into an external 75Ω single-ended load.

In some applications there may be significant high frequency loss associated with long traces between the GS12181 output and the BNC. With low to moderate loss, ISI jitter will be generated, which will reduce the output jitter compliance budget.

At 11.88Gb/s, the pre-emphasis can compensate for up to 8" of 10-mil microstrip in standard FR4. The default setting on power-up can compensate for approximately 2" of 10-mil microstrip.

Some cable drivers that operate at high data rates offer some amount of pre-emphasis to compensate for trace. However, the GS12181 allows the user to control the pre-emphasis pulse amplitude and the pre-emphasis pulse width. This extra flexibility provides a mechanism to better shape the pre-emphasis gain to match the frequency loss response of an interconnect composed of trace, connector and via losses.

The output driver swing, pre-emphasis pulse amplitude, and pre-emphasis pulse width can be optimized for SD/MADI, HD/3G, and 6G/12G through the **CFG_OUTPUT<n>_*** parameters in registers 0x7328 through 0x7333, where <n> is the output number and * is the specific control.

The DS (Driver Swing) parameter has 50 settings, where the default power-up value is 25 (approximately 800mV_{p-p}). The effective range over which the voltage increment between each setting is tightly controlled to ~20mV is 15 to 35 (600mV_{p-p} to 1000mV_{p-p}).

For maximum output swing and pre-emphasis headroom, it is recommended that the device VCCO_0 and VCCO_1 supply pins be connected to a 3.3V supply. However, for most applications where 800mV_{p-p} is the target swing amplitude and the trace length is under 5", 2.5V supply is sufficient.

The PPA (pre-emphasis pulse amplitude) has 25 settings, while the PPW (pre-emphasis pulse width) has 15. The default power-up value for each is 0 and that combination can compensate for approximately 2" of 10-mil microstrip in FR4 between the device output and BNC. Together, the PPA and PPW can be configured to provide optimum insertion loss compensation to exceed the SMPTE output jitter requirement and maximize the link jitter margin to the receiving equipment. The following section will provide a procedure of optimizing pre-emphasis setting on the GS12181.

4.3.4.1 Pre-emphasis Optimization

The goal of pre-emphasis is to open the eye at the BNC as much as possible. This means minimizing ISI jitter, while meeting the SMPTE output eye specification.

The GS12181 has a HIGH level of precision for pre-emphasis control, which allows for fine optimization of any loss channel. Pre-emphasis compensation of the GS12181 output channel is a two step process. The first step is coarse optimization, while the second step is fine optimization. However, the first step alone may meet the designers targets.

Coarse Optimization Procedure:

Given a single ended trace length tl, where tl has a 5.94GHz loss profile of 0.7dB/Inch ±20%, the following equations provide a starting point for HD-3G and 6G-12G optimized pre-emphasis settings:

$$\mathbf{PPA_{HD}} = \mathbf{int}((\mathbf{tl}), \mathbf{tl} \leq 15)$$

Equation 4-1: HD and 3G Pre-emphasis Amplitude Optimization Setting

$$\mathbf{PPW_{HD}} = \mathbf{int}((\mathbf{tl}), \mathbf{tl} \leq 15)$$

Equation 4-2: HD and 3G Pre-emphasis Width Optimization Setting

$$\mathbf{PPA_{UHD}} = \mathbf{int}(3(\mathbf{tl} - 1)), 2 \leq \mathbf{tl} \leq 7$$

Equation 4-3: 6G and 12G Pre-emphasis Amplitude Optimization Setting

$$\mathbf{PPW_{UHD}} = \mathbf{int}(2.2 \cdot \mathbf{tl}), \mathbf{tl} \leq 7$$

Equation 4-4: 6G and 12G Pre-emphasis Width Optimization Setting

Note: Int(x) is the integer of x

Pre-emphasis pulse amplitude has a direct impact on swing amplitude. After solving the above equations and implementing the settings, it may be necessary to readjust the driver swing until the swing amplitude design target is met.

In most cases, the settings calculated from these equations may be good enough. However, a better eye may be obtained by the following the Fine Optimization procedure.

Fine Optimization:

With the Hardware designed with the GS12181 connected through 1m of cable to a high bandwidth scope follow the next two steps:

1. The first step is to set the PPA and PPW to the values obtained by solving the optimization equations, and then measure the downstream jitter. While keeping PPW constant, increment the PPA by 1. If the jitter is lower after the first increment, continue to increment by 1 until the jitter begins increasing or a setting of 56 is reached. If there was a setting which resulted in a lower jitter measurement than the initial setting, that is the Optimized Pre-emphasis Amplitude setting: $PPA_{Optimal}$, and the PPA optimization procedure is complete.

   However, if the jitter increased after the first increment, decrement the setting by 1 below the initial value. If the jitter is lower after the first decrement, continue to decrement by 1 until the jitter begins increasing or a setting of 0 is reached. If there was a setting which resulted in a lower jitter measurement than the initial setting, that is the Optimized Pre-emphasis Amplitude setting: $PPA_{Optimal}$, and the PPA optimization procedure is complete.

   If incrementing the PPA or decrementing the PPA did not result in a setting with lower jitter, then the initial setting derived from the equation is the PPA optimized Pre-emphasis Amplitude setting: $PPA_{Optimal}$.

2. The second step is to set the PPA to the optimized setting $PPA_{Optimal}$ determined in step 1 and PPW to the values obtained by solving the optimization equation, then measure the downstream jitter. While keeping PPA constant, increment the PPW by 1. If the jitter is lower after the first increment, continue to increment by 1 until the jitter begins increasing or a setting of 15 is reached. If there was a setting which resulted in a lower jitter measurement than the initial setting, that is the Optimized Pre-emphasis Width setting: $PPW_{Optimal}$, and the optimization procedure is complete.

   However, if the jitter increased after the first increment, decrement the setting by 1 below the initial value. If the jitter is lower after the first decrement, continue to decrement by 1 until the jitter begins increasing or a value of 0 is reached. If there was a setting which resulted in a lower jitter measurement than the initial setting, that is the Optimized Pre-emphasis Width setting: $PPW_{Optimal}$, and the optimization procedure is complete.

   If incrementing the PPW or decrementing the PPW did not result in a setting with lower jitter, then the initial setting derived from the equation is the optimized Pre-emphasis Width setting: $PPW_{Optimal}$.

3. Pre-emphasis pulse amplitude has a direct impact on swing amplitude. The third and final step is to readjust the driver swing until the swing amplitude design target is met. The fine optimization procedure maybe repeated to ensure that the $PPA_{Optimal}$ and $PPW_{Optimal}$ settings previously determined still hold with the new DS setting.

Steps 1 and 2 are illustrated in the following two flow charts:

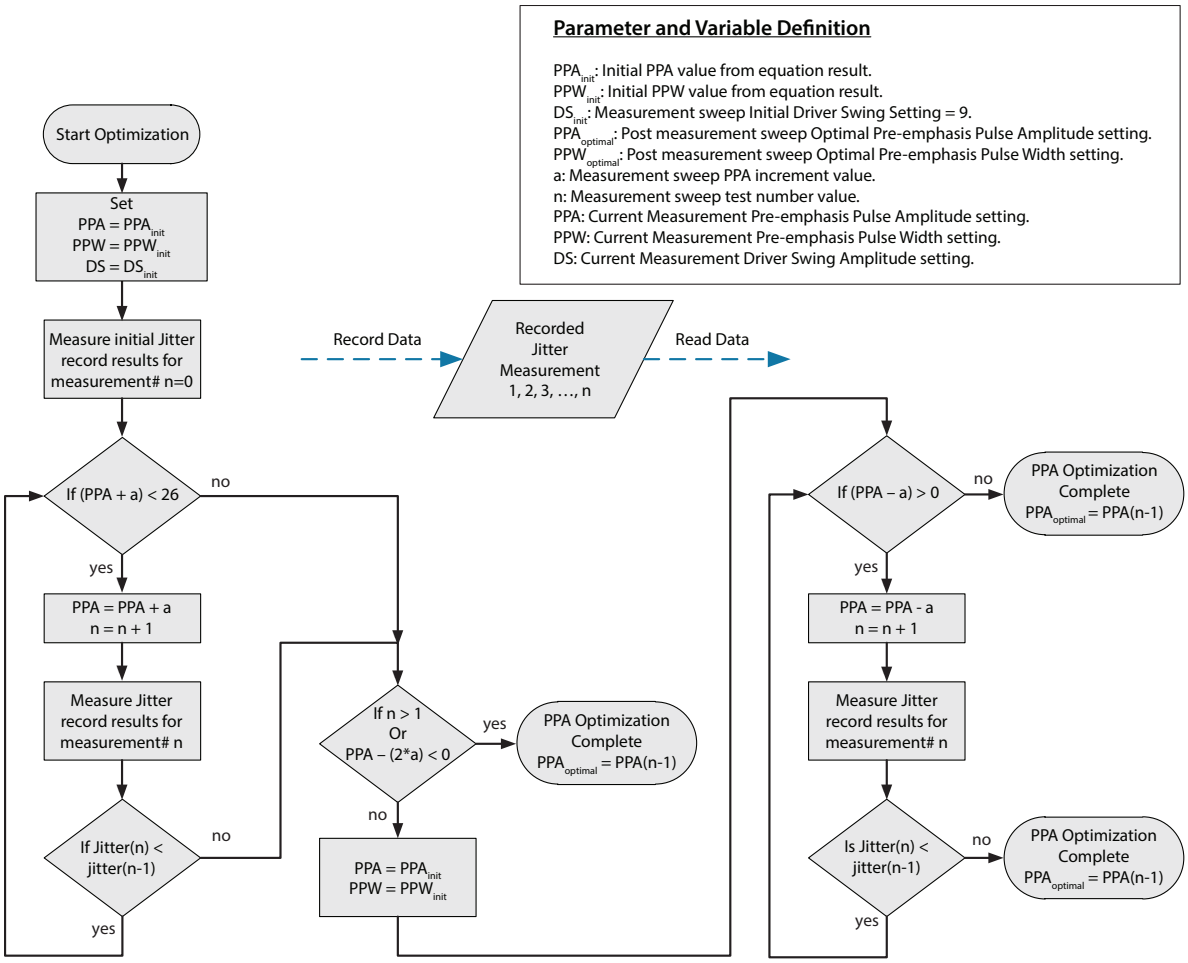


Figure 4-3: PPA Optimization Flow Chart

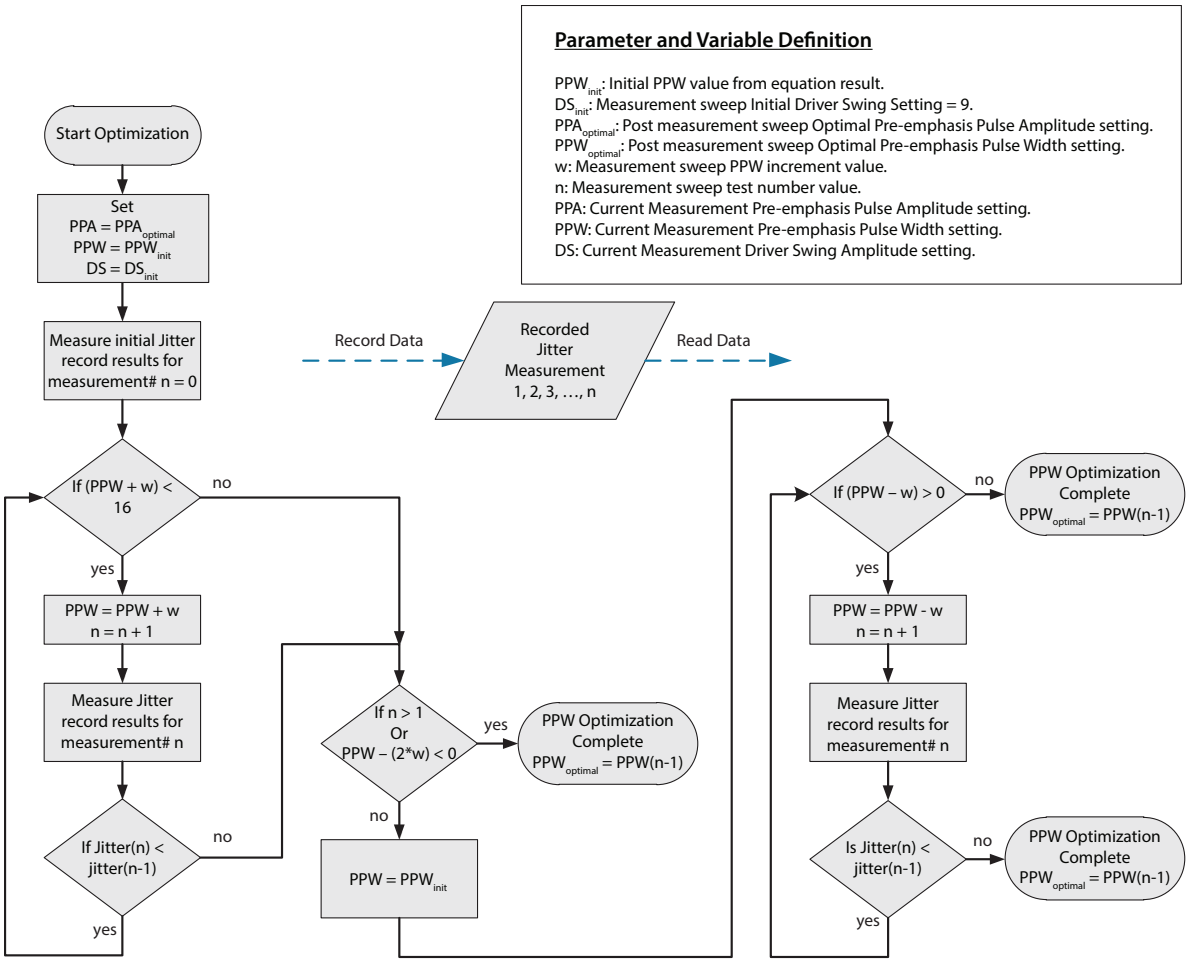


Figure 4-4: PPW Optimization Flow Chart

4.3.5 Output State Control Modes

The GS12181 provides several output state control modes to meet specific application requirements. The Outputs can be put in low power and muted, either manually, or on LOS (Loss of Signal), or on LOS and Loss of Lock. The outputs can also be completely powered sown and disabled, either manually, or on LOS. Lastly, the outputs can be put into balanced mode for powered ORL measurements. The mode priorities from highest to lowest are as follows: Balanced Mode, Disable Mode, and Mute mode. Please see Section 4.3.5.1 through Section 4.3.5.3 for more details.

4.3.5.1 Output Mute Mode

Each of the outputs on the GS12181 also have independent mute controls, which can be configured through the host interface.

The following are the four modes of output mute:

1. Auto mute on LOS (default)
2. Auto mute on LOS and during rate search
3. Outputs always operational
4. Outputs always muted

The default setting on power-up sets the output drivers in the first mode, where the outputs automatically mute on the assertion of LOS. In addition to mute on LOS, with auto mode enabled, setting control parameter **CTRL_OUTPUT<n>_AUTO _MUTE_DURING_RATE_SEARCH** to 1_b sets the outputs to mute when the device loses lock and begins to rate search.

The outputs can be set to never mute by setting the control parameters **CTRL_OUTPUT<n>_AUTO_MUTE** and **CTRL_OUTPUT<n>_ MANUAL_MUTE** to 0_b. Alternatively, the outputs can be forced to always be muted by setting the control parameters **CTRL_OUTPUT<n>_AUTO_MUTE** and **CTRL_OUTPUT<n>_ MANUAL_MUTE** to 0_b and 1_b respectively.

Note: The <n> in the control parameter names refers to the output number.

4.3.5.2 Output Disable Mode

Each of the outputs on the GS12181 also have independent disable controls, which can be configured through the host interface.

The following are the three modes of Output Disable:

1. Outputs defer to mute settings
2. Auto Disable
3. Outputs always disabled

Mode 1 is the default setting on power-up (parameter **CTRL_OUTPUT<n>_AUTO _DISABLE** is set to 0_b).By setting control parameter **CTRL_OUTPUT<n>_AUTO _DISABLE** to 1_b, the output will power down on LOS. This includes LOS as a result of setting up Squelch Adjust (see Section 4.2.1 for more details). This mode takes precedence over any active output mute mode.

By leaving parameter **CTRL_OUTPUT<n>_AUTO_DISABLE** set to 0_b and setting parameter **CTRL_OUTPUT<n>_MANUAL_DISABLE** to 1_b, forces the output to be disabled. This mode takes precedence over any active output mute mode. Alternatively, the second output can be powered down by applying a signal to GPIO3 (SDO1 disable). SDO1 disable is the default mode for GPIO3 at power-up.

Note: The <n> in the control parameter names refers to the output number.

4.3.5.3 Output Balanced Mode

The GS12181 has a feature designed to facilitate reliable output return loss (ORL) measurement while the device is still powered. The device can be put into a BALANCE mode which prevents the outputs from toggling while ORL is being measured.

BALANCE mode can be enabled through the host interface, by setting control parameter **CTRL_OUTPUT<n>_ BALANCED** in register 734D to 1_b, where <n> is the output number.

4.3.5.4 Output Control and Status Registers Summary

The following two tables list the most commonly used control and status parameters of the Output blocks. For a complete list of registers and functions, please see Section 5.

Table 4-7: Re-timer Bypass Control Parameters

Address$_h$	Bit Slice	Parameter Name	Description
0x734C	3:3	CTRL_OUTPUT1_RETIMER_MANUAL _BYPASS	Enables manual CDR bypass signal when CTRL_OUTPUT1_RETIMER_AUTO_BYPASS is 0_b.
	2:2	CTRL_OUTPUT1_RETIMER_AUTO _BYPASS	Sets or disables the automatic CDR bypass signal mode.
	1:1	CTRL_OUTPUT0_RETIMER_AUTO _BYPASS	Enables manual CDR bypass signal when CTRL_OUTPUT0_RETIMER_AUTO_BYPASS is 0_b.
	0:0	CTRL_OUTPUT0_RETIMER_MANUAL _BYPASS	Sets or disables the automatic CDR bypass signal mode.

Table 4-8: Output Swing and Pre-emphasis Control Parameters

Address$_h$	Bit Slice	Parameter Name	Description
0x732B/0x7329	13:8	CFG_OUTPUT<n>_CD_SD_TD_DRIVER_SWING	Output <n> main output driver amplitude configuration parameter for SD and MADI.
0x732A/0x7328	12:8	CFG_OUTPUT<n>_CD_SD_TD_ PREEMPH_WIDTH	Output <n> pre-emphasis pulse width configuration parameter for SD and MADI.
	6:6	CFG_OUTPUT<n>_CD_SD_TD_ PREEMPH_PWRDWN	Output <n> pre-emphasis power down parameter for SD and MADI.
	5:0	CFG_OUTPUT<n>_CD_SD_TD_ PREEMPH_AMPL	Output <n> pre-emphasis pulse amplitude configuration parameter for SD and MADI.
0x732D/0x732F	13:8	CFG_OUTPUT<n>_CD_HD_DRIVER_SWING	Output <n> main output driver amplitude configuration parameter for HD and 3G.
0x732C/0x732E	12:8	CFG_OUTPUT<n>_CD_HD_ PREEMPH_WIDTH	Output <n> pre-emphasis pulse width configuration parameter for HD and 3G.
	6:6	CFG_OUTPUT<n>_CD_HD_ PREEMPH_PWRDWN	Output <n> pre-emphasis power down parameter for HD and 3G.
	5:0	CFG_OUTPUT<n>_CD_HD_ PREEMPH_AMPL	Output <n> pre-emphasis pulse amplitude configuration parameter for HD and 3G.
0x7331/0x7333	13:8	CFG_OUTPUT<n>_CD_UHD_DRIVER_SWING	Output <n> main output driver amplitude configuration parameter for 6G and 12G.
0x7330/0x7332	12:8	CFG_OUTPUT<n>_CD_UHD_ PREEMPH_WIDTH	Output <n> pre-emphasis pulse width configuration parameter for6G and 12G
	6:6	CFG_OUTPUT<n>_CD_UHD_ PREEMPH_PWRDWN	Output <n> pre-emphasis power down parameter for 6G and 12G
	5:0	CFG_OUTPUT<n>_CD_UHD_ PREEMPH_AMPL	Output <n> pre-emphasis pulse amplitude configuration parameter for 6G and 12G
0x7348	3:3	CTRL_OUTPUT0_DATA_ INVERT	Controls optional signal polarity inversion on SDO0.
	2:2	CTRL_OUTPUT1_DATA_ INVERT	Controls optional signal polarity inversion on SDO1.
	0:0	CTRL_OUTPUT1_SIGNAL_SEL	Sets the Clock/Data mode of SDO1. 0_b = Data 1_b = Clock

Table 4-9: Mute and Disable Control Parameters

Parameter Name (<n>: Output Number)	GS12181 Output Modes							
	Balanced Mode	Output Disabled on LOS	Output Disabled on LOS Muted during Rate Search	Output is Always Disabled	Output is Muted on LOS, including LOS from Squelch Adjust	Output is Muted on Rate Search and on LOS, including LOS from Squelch Adjust	Output is Always On	Output Always Muted
	Parameter Value							
CTRL_OUTPUT<n>_BALANCED	1	0	0	0	0	0	0	0
CTRL_OUTPUT<n>_AUTO_DISABLE	X	1	1	0	0	0	0	0
CTRL_OUTPUT<n>_MANUAL_DISABLE	X	X	X	1	0	0	0	0
CTRL_OUTPUT<n>_AUTO_MUTE	X	1	1	X	1	1	0	0
CTRL_OUTPUT<n>_AUTO_MUTE_DURING_RATE_SEARCH	X	0	1	X	0	1	X	X
CTRL_OUTPUT<n>_MANUAL_MUTE	X	X	X	X	X	X	0	1

Table 4-10: Output Status Parameters

$Address_h$	Bit Slice	Parameter Name	Description
0x7386	7:4	STAT_OUTPUT<n>_MODE	Provides the status of the output driver.
0x7387	15:15	STAT_OUTPUT<n>_DISABLE	Indicates if disable mode is enabled for the output in the control priority hierarchy.
	13:13	STAT_OUTPUT<n>_MUTE	Indicates if mute mode is enabled for the output in the control priority hierarchy.
	11:11	STAT_OUTPUT<n>_RETIMER_BYPASS	Indicates the re-timed status of signal available at the output.

As can be seen in Table 4-9, there is a hierarchy in the control modes. If Balanced mode is selected, no active signal will be present on the output regardless if there is a valid signal at the input. If Balanced mode is off and both disable and mute modes are configured, disable mode takes priority over mute mode. The **STAT_OUTPUT<n>_MODE** parameter indicates the active mode of each output driver, whereas the **STAT_OUTPUT<n>_DISABLE** and **STAT_OUTPUT<n>_DISABLE** parameters indicate potential active modes if that particular mode is the highest enabled in the hierarchy.

Note: The <n> in the control parameter names refers to the output number.

4.4 GPIO Controls

There are four configurable GPIO pins that can be programmed for any of the following functions:

Output:

- Output driven LOW
- Output driven HIGH
- PLL Lock Status (Default signal option) (Default GPIO1)
- LOS (Los of Signal, inverse of Carrier Detect) (Default GPIO0)
- CD (Carrier Detect)
- SH/$\overline{\text{HD}}$ Status
- Rate Detected [0]
- Rate Detected [1]
- Rate Detected [2]
- Reference Clock (Only available on GPIO1)

Input:

- Output 1 Disable Control (Default GPIO3)

Note: If there is a conflict between the internal register configuration of a given device function and the logic-level applied to a GPIO pin that is configured to control that same device function, the GPIO logic-level takes precedence over the internal register configuration. Also, the default signal option for GPIO2 is not active on this version of the device, but will be Sleep control on future devices.

The logic HIGH and LOW levels of the GPIO[3:0] pin to which LOS is connected are specified by the EIA/JESD8-5A standard for 1.8V operation.

For detailed information on configuring GPIO[3:0], refer to Section 5.

4.5 GSPI Host Interface

The GS12181 is configured via the Gennum Serial Peripheral Interface (GSPI).

The GSPI host interface is comprised of a serial data input signal (SDIN pin), serial data output signal (SDOUT pin), an active-low chip select ($\overline{\text{CS}}$ pin) and a burst clock (SCLK pin).

The GS12181 is a slave device, so the SCLK, SDIN and $\overline{CS}$ signals must be sourced by the application host processor.

All read and write access to the device is initiated and terminated by the application host processor.

The user can manually select the appropriate mode of operation required.

4.5.1 $\overline{CS}$ Pin

The Chip Select pin ($\overline{CS}$) is an active-low signal provided by the host processor to the GS12181.

The high-to-low transition of this pin marks the start of serial communication to the GS12181.

The low-to-high transition of this pin marks the end of serial communication to the GS12181.

Each device may use its own separate Chip Select signal from the host processor or up to 32 devices may be connected to a single Chip Select when making use of the Unit Address feature.

Only those devices whose Unit Address matches the UNIT ADDRESS in GSPI Command Word 1 will respond to communication from the host processor (unless the B'CAST ALL bit in GSPI Command Word 1 is set to 1).

4.5.2 SDIN Pin

The SDIN pin is the GSPI serial data input pin of the GS12181.

The 16-bit Command and Data Words from the host processor or from the SDOUT pin of other devices are shifted into the device on the rising edge of SCLK when the $\overline{CS}$ pin is LOW.

4.5.3 SDOUT Pin

The SDOUT pin is the GSPI serial data output of the GS12181.

All data transfers out of the GS12181 to the host processor or to the SDIN pin of other connected devices occur from this pin.

By default at power up or after system reset, the SDOUT pin provides a non-clocked path directly from the SDIN pin, regardless of the $\overline{CS}$ pin state, except during the GSPI Data Word portion for read operations from the device. This allows multiple devices to be connected in Loop-Through configuration.

For read operations, the SDOUT pin is used to output data read from an internal Configuration and Status Register (CSR) when $\overline{CS}$ is LOW. Data is shifted out of the device on the falling edge of SCLK, so that it can be read by the host processor or other downstream connected device on the subsequent SCLK rising edge.

4.5.3.1 GSPI Link Disable Operation

It is possible to disable the direct SDIN to SDOUT (Loop-Through) connection by writing a value of 1 to the GSPI_LINK_DISABLE bit in HOST_CONFIG. When disabled, any data appearing at the SDIN pin will not appear at the SDOUT pin and the SDOUT pin is HIGH.

Note: Disabling the Loop-Through operation is temporarily required when initializing the Unit Address for up to 32 connected devices.

The time required to enable/disable the Loop-Through operation from assertion of the register bit is less than the GSPI configuration command delay as defined by the parameter $t_{cmd\_GSPI\_config}$ (4 SCLK cycles).

Table 4-11: GSPI_LINK_DISABLE Bit Operation

Bit State	Description
0	SDIN pin is looped through to the SDOUT pin.
1	Data appearing at SDIN does not appear at SDOUT, and SDOUT pin is HIGH.

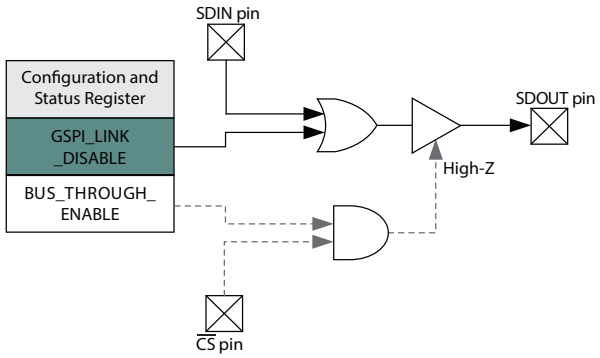


Figure 4-5: GSPI_LINK_DISABLE Operation

4.5.3.2 GSPI Bus-Through Operation

Using GSPI Bus-Through operation, the GS12181 can share a common PCB trace with other GSPI devices for SDOUT output.

When configured for Bus-Through operation, by setting GSPI_BUS_THROUGH_ENABLE bit to 1, the SDOUT pin will be high-impedance when the $\overline{CS}$ pin is HIGH.

When the $\overline{CS}$ pin is LOW, the SDOUT pin will be driven and will follow regular read and write operation as described in Section 4.5.3.

Multiple chains of GS12181 devices can share a single SDOUT bus connection to host by configuring the devices for Bus-Through operation. In such configuration, each chain requires a separate Chip Select ($\overline{CS}$).

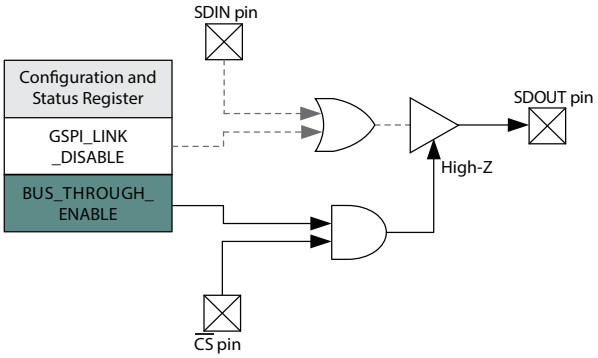


Figure 4-6: GSPI_BUS_THROUGH_ENABLE Operation

4.5.4 SCLK Pin

The SCLK pin is the GSPI serial data shift clock input to the device, and must be provided by the host processor.

Serial data is clocked into the GS12181 SDIN pin on the rising edge of SCLK. Serial data is clocked out of the device from the SDOUT pin on the falling edge of SCLK (read operation). SCLK is ignored when $\overline{CS}$ is HIGH.

The maximum interface clock rate is 27MHz.

4.5.5 Command Word 1 Description

All GSPI accesses are a minimum of 48 bits in length (two 16-bit Command Words followed by a 16-bit Data Word) and the start of each access is indicated by the high-to-low transition of the chip select ($\overline{CS}$) pin of the GS12181.

The format of the Command Words and Data Word are shown in Figure 4-8.

Data received immediately following this high-to-low transition will be interpreted as a new Command Word.

4.5.5.1 R/$\overline{W}$ bit—B15 Command Word 1

This bit indicates a read or write operation.

When R/$\overline{W}$ is set to 1, a read operation is indicated, and data is read from the register specified by the ADDRESS field of the Command Word.

When R/$\overline{W}$ is set to 0, a write operation is indicated, and data is written to the register specified by the ADDRESS field of the Command Word.

4.5.5.2 B'CAST ALL—B14 Command Word 1

This bit is used in write operations to configure all devices connected in Loop-Through and Bus-Through configuration with a single command.

When B'CAST ALL is set to 1, the following Data Word (AUTOINC = 0) or Data Words (AUTOINC = 1) are written to the register specified by the ADDRESS field of the Command Words (and subsequent addresses when AUTOINC = 1), regardless of the setting of the UNIT ADDRESS(es).

When B'CAST ALL is set to 0, a normal write operation is indicated. Only those devices that have a Unit Address matching the UNIT ADDRESS field of Command Word 1 write the Data Word to the register specified by the ADDRESS field of the Command Words.

4.5.5.3 EMEM—B13 Command Word 1

The EMEM bit must be set to 1 in Command Word 1. When EMEM is set to 1, a 23-bit address split between Command Word 1 and Command Word 2 is used to access the registers in this device.

4.5.5.4 AUTOINC—B12 Command Word 1

When AUTOINC is set to 1, Auto-Increment read or write access is enabled.

In Auto-Increment Mode, the device automatically increments the register address for each contiguous read or write access, starting from the address defined in the ADDRESS field of the Command Word.

The internal address is incremented for each 16-bit read or write access until a low-to-high transition on the $\overline{CS}$ pin is detected.

When AUTOINC is set to 0, single read or write access is required.

Auto-Increment write must not be used to update values in HOST_CONFIG.

4.5.5.5 UNIT ADDRESS—B11:B7 Command Word 1

The 5 bits of the UNIT ADDRESS field of the Command Word are used to select one of 32 devices connected on a single chip select in Loop-Through or Bus-Through configurations.

Read and write accesses are only accepted if the UNIT ADDRESS field matches the programmed DEVICE_UNIT_ADDRESS in HOST_CONFIG.

By default at power-up or after a device reset, the DEVICE_UNIT_ADDRESS is set to 00_h.

4.5.5.6 ADDRESS—B6:B0 Command Word 1 and B15:B0 Command Word 2

The Command and Data Word formats are shown in Figure 4-7 and Figure 4-8 below.

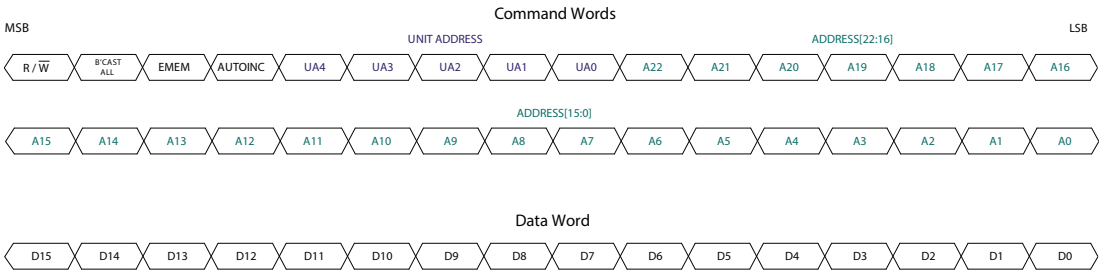


Figure 4-7: Command and Data Word Format

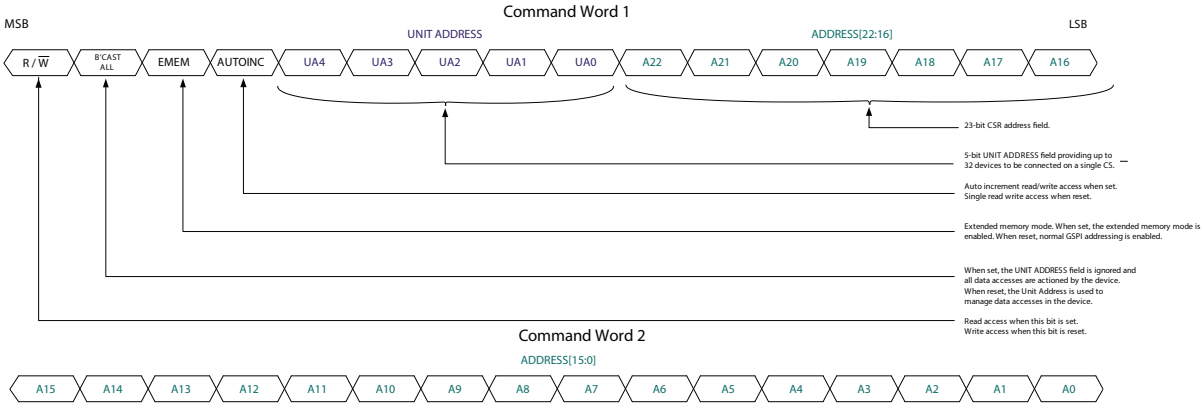


Figure 4-8: Command Word 1 and Command Word 2 Details

4.5.6 GSPI Transaction Timing

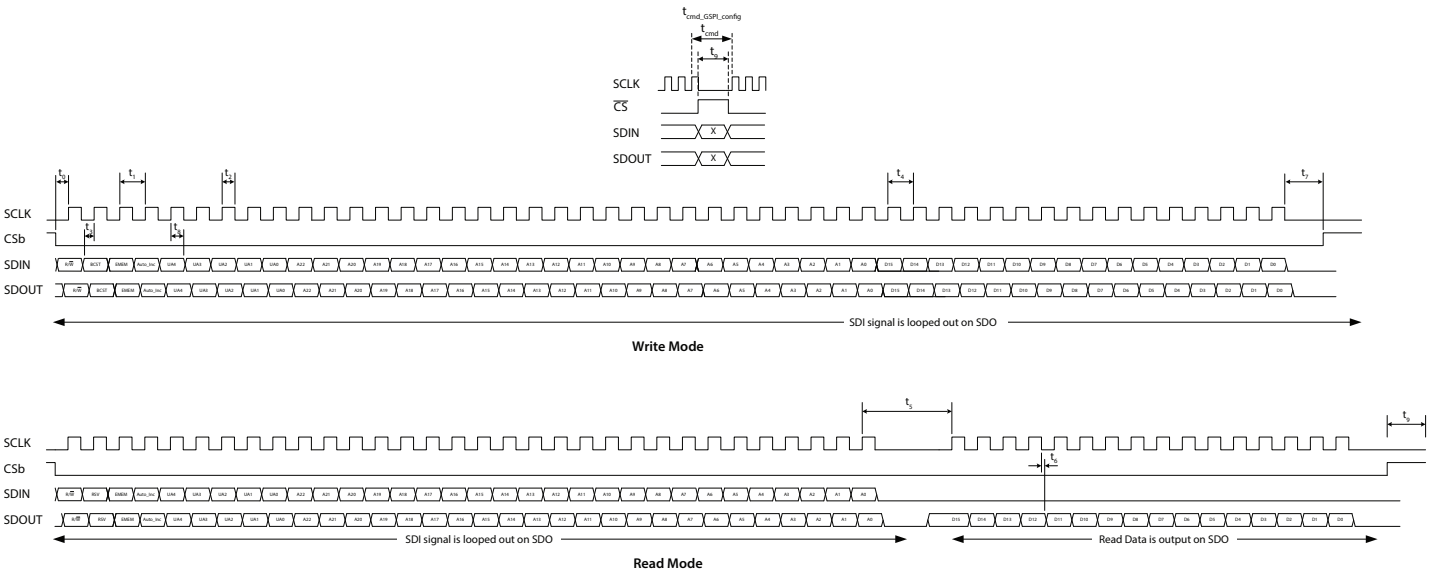


Figure 4-9: GSPI External Interface Timing

Table 4-12: GSPI Timing Parameters

Parameter	Symbol	Equivalent SCLK Cycles	Min	Typ	Max	Units
SCLK Frequency	—	—	—	—	27	MHz
CS Low Before SCLK Rising Edge	t_0	—	1.7	—	—	ns
SCLK Period	t_1	—	37	—	—	ns
SCLK Duty Cycle	t_2	—	40	50	60	%
Input Data Setup Time	t_3	—	2.3	—	—	ns
SCLK Idle Time – Write	t_4	1	38.5[1]	—	—	ns
SCLK Idle Time – Read	t_5	—	138	—	—	ns
Inter–Command Delay Time	t_{cmd}	3	115	—	—	ns
Inter–Command Delay Time (after GSPI configuration write)	$t_{cmd\_GSPI\_conf}$[2]	4	139	—	—	ns
SDOUT After SCLK Falling Edge	t_6	—	1.3	—	6.4	ns
$\overline{CS}$ High After Final SCLK Falling Edge	t_7	—	0	—	—	ns
Input Data Hold Time	t_8	—	1.2	—	—	ns
$\overline{CS}$ High Time	t_9	—	58	—	—	ns
SDIN to SDOUT Combinatorial Delay	—	—	—	—	3.4	ns
Max chips daisy-chained at max SCLK frequency (26 MHz)	When host clocks in SDOUT data on falling edge of SCLK		—	—	8	# of compatible Semtech devices
Max frequency for 32 daisy-chained devices			—	—	7.5	MHz

Note:

1. Parameter is exactly multiple of SCLK periods and scales proportionally.
2. $t_{cmd\_GSPI\_conf}$ inter-command delay must be used whenever modifying HOST_CONFIG register at address 0x00.

4.5.7 Single Read/Write Access

Single read/write access timing for the GSPI interface is shown in Figure 4-10 to Figure 4-14.

When performing a single read or write access, one Data Word is read from/written to the device per access. Each access is a minimum of 48 bits long, consisting of two Command Words and a single Data Word. The read or write cycle begins with a high-to-low transition of the $\overline{CS}$ pin. The read or write access is terminated by a low-to-high transition of the $\overline{CS}$ pin.

The maximum interface clock rate is 27MHz and the inter-command delay time indicated in the figures as t_{cmd}, is a minimum of 3 SCLK clock cycles. After modifying values in HOST_CONFIG, the inter-command delay time, $t_{cmd\_GSPI\_config}$, is a minimum of 4 SCLK clock cycles.

For read access, the time from the last bit of Command Word 2 to the start of the data output, as defined by t_5, corresponds to no less than 4 SCLK clock cycles at 27MHz.

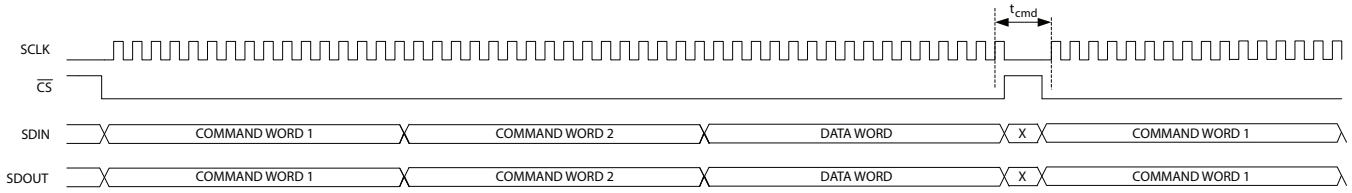


Figure 4-10: GSPI Write Timing—Single Write Access with Loop-through Operation (default)

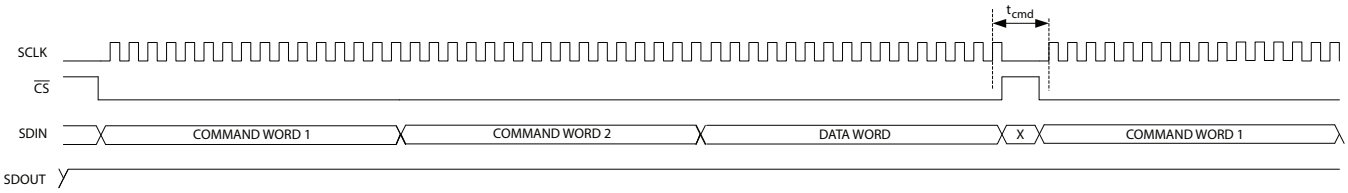


Figure 4-11: GSPI Write Timing—Single Write Access with GSPI Link-disable Operation

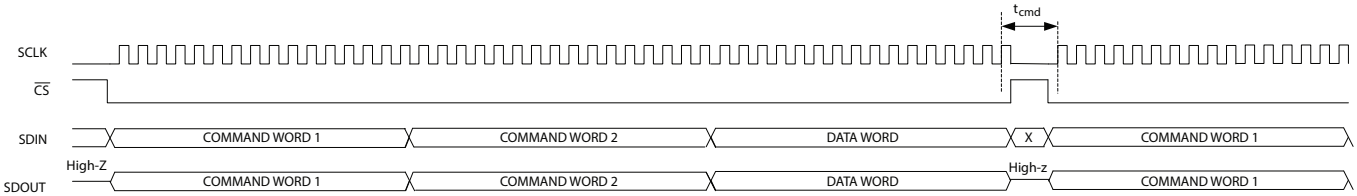


Figure 4-12: GSPI Write Timing—Single Write Access with Bus-through Operation

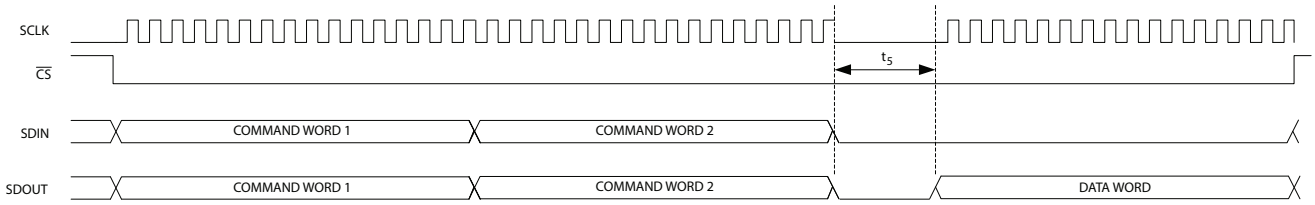


Figure 4-13: GSPI Read Timing—Single Read Access with Loop-through Operation (default)

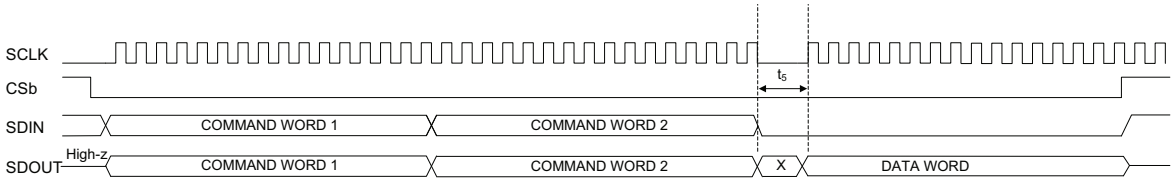


Figure 4-14: GSPI Read Timing—Single Read Access with Bus-through Operation

4.5.8 Auto-increment Read/Write Access

Auto-increment read/write access timing for the GSPI interface is shown in Figure 4-15 to Figure 4-19.

Auto-increment mode is enabled by the setting of the AUTOINC bit of Command Word 1.

In this mode, multiple Data Words can be read from/written to the device using only one starting address. Each access is initiated by a high-to-low transition of the $\overline{CS}$ pin, and consists of two Command Words and one or more Data Words. The internal address is automatically incremented after the first read or write Data Word, and continues to increment until the read or write access is terminated by a low-to-high transition of the $\overline{CS}$ pin.

Note: Writing to HOST_CONFIG using Auto-increment access is not allowed.

The maximum interface clock rate is 27MHz and the inter-command delay time indicated in the diagram as t_{cmd}, is a minimum of 3 SCLK clock cycles.

For read access, the time from the last bit of the second Command Word to the start of the data output of the first Data Word as defined by t_5 will be no less than 4 SCLK cycles at 27MHz. All subsequent read data accesses will not be subject to this delay during an Auto-Increment read.

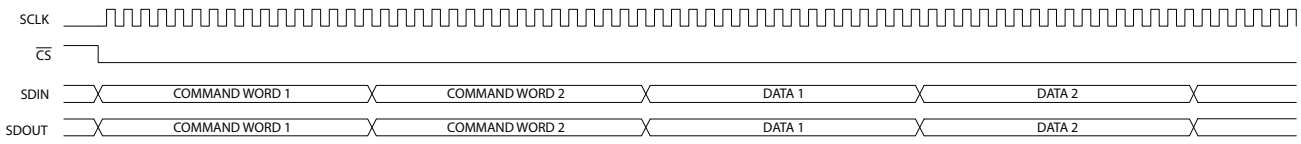


Figure 4-15: GSPI Write Timing—Auto-Increment with Loop-through Operation (default)

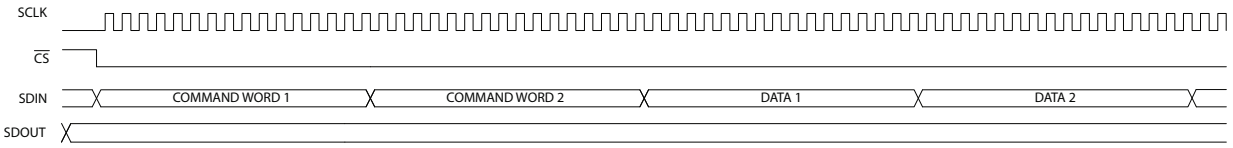


Figure 4-16: GSPI Write Timing—Auto-Increment with GSPI Link Disable Operation

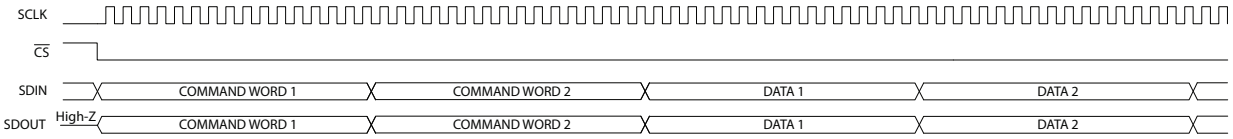


Figure 4-17: GSPI Write Timing—Auto-Increment with Bus-through Operation

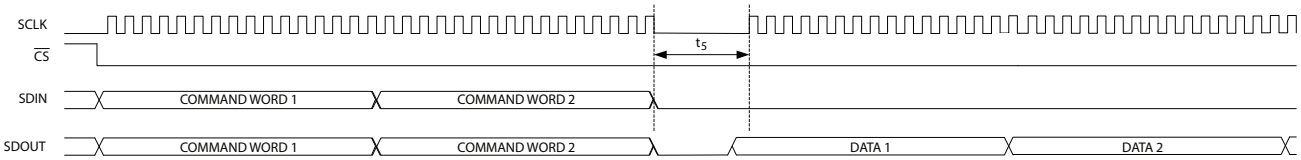


Figure 4-18: GSPI Read Timing—Auto-Increment Read with Loop-through Operation (default)

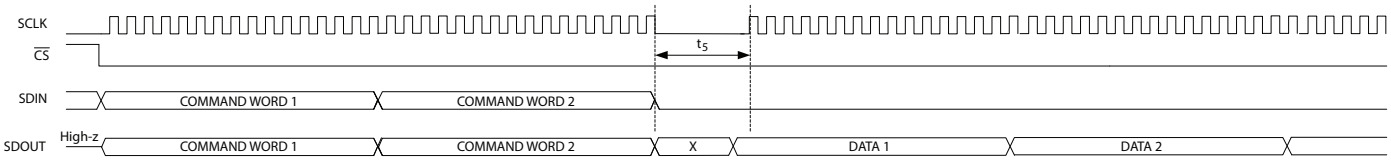


Figure 4-19: GSPI Read Timing—Auto-Increment Read with Bus-through Operation

4.5.9 Setting a Device Unit Address

Multiple (up to 32) GS12181 devices can be connected to a common Chip Select ($\overline{CS}$) in Loop-Through or Bus-Through operation.

To ensure that each device selected by a common $\overline{CS}$ can be separately addressed, a unique Unit Address must be programmed by the host processor at start-up as part of system initialization or following a device reset.

Note: By default at power up or after a device reset, the **DEVICE_UNIT_ADDRESS** of each device is set to 0_h and the SDIN→SDOUT non-clocked loop-through for each device is enabled.

These are the steps required to set the **DEVICE_UNIT_ADDRESS** of devices in a chain to values other than 0:

1. Write to Unit Address 0 selecting **HOST_CONFIG** (ADDRESS = 0), with the **GSPI_LINK_DISABLE** bit set to 1 and the **DEVICE_UNIT_ADDRES**S field set to 0. This disables the direct SDIN→SDOUT non-clocked path for all devices on chip select.

2. Write to Unit Address 0 selecting H**OST_CONFIG** (ADDRESS = 0), with the **GSPI_LINK_DISABLE** bit set to 0 and the **DEVICE_UNIT_ADDRESS** field set to a unique Unit Address. This configures **DEVICE_UNIT_ADDRESS** for the first device in the chain. Each subsequent such write to Unit Address 0 will configure the next device in the chain. If there are 32 devices in a chain, the last (32nd) device in the chain must use **DEVICE_UNIT_ADDRESS** value 0.
3. Repeat step 2 using new, unique values for the **DEVICE_UNIT_ADDRESS** field in **HOST_CONFIG** until all devices in the chain have been configured with their own unique Unit Address value.

Note: $t_{cmd\_GSPI\_conf}$ delay must be observed after every write that modifies **HOST_CONFIG**.

All connected devices receive this command (by default the Unit Address of all devices is 0), and the Loop-Through operation will be re-established for all connected devices.

Once configured, each device will only respond to Command Words with a UNIT ADDRESS field matching the **DEVICE_UNIT_ADDRESS** in **HOST_CONFIG**.

Note: Although the Loop-Through and Bus-Through configurations are compatible with previous generation GSPI enabled devices (backward compatibility), only devices supporting Unit Addressing can share a chip select. All devices on any single chip select must be connected in a contiguous chain with only the last device's SDOUT connected to the application host processor. Multiple chains configured in Bus-Through mode can have their final SDOUT outputs connected to a single application host processor input.

4.5.10 Default GSPI Operation

By default at power up or after a device reset, the GS12181 is set for Loop-Through Operation and the internal **DEVICE_UNIT_ADDRESS** field of the device is set to 0.

Figure 4-20 shows a functional block diagram of the Configuration and Status Register (CSR) map in the GS12181.

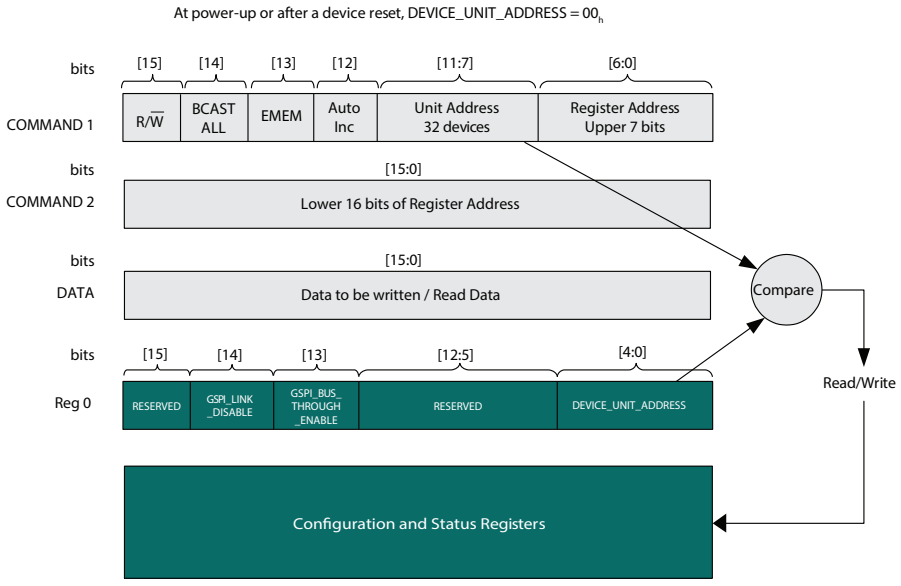


Figure 4-20: Internal Register Map Functional Block Diagram

The steps required for the application host processor to write to the Configuration and Status Registers via the GSPI, are as follows:

1. Set Command Word 1 for write access (R/$\overline{W}$ = 0); set Auto Increment; set the Unit Address field in the Command Word 1 to match the configured **DEVICE_UNIT_ADDRESS** which will be zero after power-up. Set the Register Address bits in Command Word 1 to match the upper 7 bits of the register address to be accessed. Set the bits in Command Word 2 to match the lower 16 bits of the register address to be accessed. Write Command Word 1 and Command Word 2.
2. Write the Data Word to be written to the first register.
3. Write the Data Word to be written to the next register in Auto Increment mode, etc.

Read access is the same as the above with the exception of step 1, where the Command Word 1 is set for read access (R/$\overline{W}$ = 1).

Note: The UNIT ADDRESS field of Command Word 1 must always match **DEVICE_UNIT_ADDRESS** for an access to be accepted by the device. Changing **DEVICE_UNIT_ADDRESS** to a value other than 0 is only required if multiple devices are connected to a single chip select (in Loop-Through or Bus-Through configuration).

5. Register Map

The host interface on the GS12181 provides users complete control of key features such as GPIO configuration, PLL loop bandwidth settings, re-time parameters, trace equalization, bypass modes, output swing controls, output disable, pre-emphasis control and many others.

Note: Values of registers at addresses not listed in Table 5-3 should not be changed.

5.1 Control Registers

Table 5-1: Control Registers

GSPI $Address_h$	Register Name	R/W
00	CONTROL _REG	RW
01 to 7E	RSVD	RW
7F	RESET_REG_0	RW
Device Configuration		
7304	MISC_CTRL	RW
7305	RSVD	RW
7306	RATE _DETECT _MODE	RW
7307	RSVD	RW
CDR Configuration		
7308	REF_CLK_ MODE	RW
7309	RSVD	RW
730A	PLL_LOOP_ BANDWIDTH _UHD	RW
730B	PLL_LOOP_ BANDWIDTH_ HD	RW
730C	PLL_LOOP_ BANDWIDTH_ SD_MADI	RW
730D to 730F	RSVD	RW
GPIO Configuration		
7310	GPIO0_CFG	RW
7311	GPIO1_CFG	RW
7312	GPIO2_CFG	RW
7313	GPIO3_CFG	RW

Table 5-1: Control Registers (Continued)

GSPI Address$_h$	Register Name	R/W
Equalizer Configuration		
7314 to 731D	RSVD	RW
731E	TREQ_INPUT_ BOOST	RW
731F	TREQ_CD_ HYSTERESIS	RW
7320 to 7325	RSVD	RW
Output Configuration		
7326	OUTPUT_CFG	RW
7327	RSVD	RW
7328	OUTPUT_ PARAM_CD_ SD_TD_0	RW
7329	OUTPUT_ PARAM_CD_ SD_TD_1	RW
732A	OUTPUT_ PARAM_CD_ SD_TD_2	RW
732B	OUTPUT_ PARAM_CD_ SD_TD_3	RW
732C	OUTPUT_ PARAM_CD_ HD_0	RW
732D	OUTPUT_ PARAM_CD_ HD_1	RW
732E	OUTPUT_ PARAM_CD_ HD_2	RW
732F	OUTPUT_ PARAM_CD_ HD_3	RW
7330	OUTPUT_ PARAM_CD_ UHD_0	RW
7331	OUTPUT_ PARAM_CD_ UHD_1	RW
7332	OUTPUT_ PARAM_CD_ UHD_2	RW
7333	OUTPUT_ PARAM_CD_ UHD_3	RW
7334 to 7347	RSVD	RW
7348	OUTPUT_SIG_ SELECT	RW
7349	CONTROL _OUTPUT _MUTE	RW
734A	CONTROL_ OUTPUT_ DISABLE	RW
734B	CONTROL_ OUTPUT_ RATE_MODE	RW
734C	CONTROL_ RETIMER_ BYPASS	RW
734D	CONTROL_ BALANCED_ MODE	RW
734E to 737F	RSVD	RW

5.2 Status Registers

Table 5-2: Status Registers

GSPI Address$_h$	Register Name	R/W
7380 to 7382	RSVD	RW
7383	DEVICE_ID	RW
7384	STICKY_ COUNTS_0	RW
7385	STICKY_ COUNTS_1	RW
7386	CURRENT_ STATUS_0	RW
7387	CURRENT_ STATUS_1	RW
7388 to 7390	RSVD	RW

5.3 Register Descriptions

Table 5-3: Register Descriptions

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
00	CONTROL _REG	RSVD	15:15	RW	0	Reserved — do not modify.
		GSPI_LINK_DISABLE	14:14	RW	0	GSPI loop-through disable.
		GSPI_BUS_THROUGH_ ENABLE	13:13	RW	0	GSPI bus-through enable.
		DEV_UNIT_ADDRESS	4:0	RW	0	Device address programmed by application.
01 to 7E	RSVD	RSVD	15:0	RW	—	Do not access these registers. It is not permitted to perform a read/write function on these registers. If data is written, any of the registers device performance is not guaranteed, and a device Reset must be applied.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
7F	RESET_REG_0	RESET_CONTROL	15:0	RW	DD00	Device Reset, Reverts all internal logic and register values to defaults. Write Values: AA00 = Asserts device reset DD00 = De-assert device reset AD00 = Assert/de-assert device reset in a single write Read Values: $AA00_h$ = User-initiated reset is asserted $DD00_h$ = User-initiated reset is de-asserted
7304	MISC_CTRL	RSVD	15:1	RW	0	Reserved — do not modify.
		CTRL_CLEAR_COUNTS	0:0	RW	0	0 = No action 1 = Clear sticky counts Part of a four way handshake with STAT_CLEAR_COUNTS_STATUS (register 85). Ensure STAT_CLEAR_COUNTS _STATUS = 0 (idle), before setting CTRL_CLEAR_COUNTS = 1 (clear sticky counts). Once the device reports STAT_CLEAR_COUNTS _STATUS = 2 (cleared), reset CTRL_CLEAR_COUNTS to 0. The device will now reset STAT_CLEAR_COUNTS_STATUS to 0 (idle) and the clearing process can be repeated at any time.
7305	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
7306	RATE _DETECT _MODE	RSVD	15:14	RW	0	Reserved — do not modify.
		CFG_RATE_ENA_12G	13:13	RW	1	12G auto rate detection enable: 0 = Disable rate 1 = Enable rate
		CFG_RATE_ENA_6G	12:12	RW	1	6G auto rate detection enable: 0 = Disable rate 1 = Enable rate
		CFG_RATE_ENA_3G	11:11	RW	1	3G auto rate detection enable: 0 = Disable rate 1 = Enable rate
		CFG_RATE_ENA_HD	10:10	RW	1	HD auto rate detection enable: 0 = Disable rate 1 = Enable rate
		CFG_RATE_ENA_SD	9:9	RW	1	SD auto rate detection enable: 0 = Disable rate 1 = Enable rate
		CFG_RATE_ENA_MADI	8:8	RW	0	MADI auto rate detection enable: 0 = Disable rate 1 = Enable rate
		RSVD	7:5	RW	0	Reserved — do not modify.
		CFG_MANUAL_RATE	4:1	RW	0	0 = Reserved 1 = MADI 2 = SD 3 = HD 4 = 3G 5 = 6G 6 = 12G 7 = Reserved Manual rate selection. The CDR will only lock to the selected rate.
		CFG_AUTO_RATE_ DETECT_INA	0:0	RW	1	0 = Disable auto rate detection 1 = Enable auto rate detection When automatic rate detection is disabled, the rate is set by CFG_MANUAL_RATE. The auto rate detection mask (CFG_RATE_ENA_*) only when auto rate detection is enabled.
7307	RSVD	RSVD	15:0	RW	0	Do not modify these registers.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
CDR Configuration						
7308	REF_CLK_ MODE	RSVD	15:2	RW	0	Reserved — do not modify.
		CFG_REF_CLK_MODE_ MANUAL	1:1	RW	1	0 = External reference clock mode 1 = Reference-less mode
		RSVD	0:0	RW	0	Reserved — do not modify.
7309	RSVD	RSVD	15:0	RW	73	Reserved — do not modify.
730A	PLL_LOOP_ BANDWIDTH _UHD	RSVD	15:13	RW	0	Reserved — do not modify.
		CFG_PLL_LBW_12G	12:8	RW	8	11.88Gb/s (12G) loop bandwidth setting: 00 = Reserved 01 = 0.0625x 02 = 0.125x 03 = Reserved 04 = 0.25x 05 to 07 = Reserved 08 = 0.5x 09 to 1B = Reserved 1C = 1.0x 1D to 1F = Reserved
		RSVD	7:5	RW	0	Reserved — do not modify.
		CFG_PLL_LBW_6G	4:0	RW	8	5.94Gb/s (6G) loop bandwidth setting. See CFG_PLL_LBW_12G.
730B	PLL_LOOP_ BANDWIDTH_ HD	RSVD	15:13	RW	0	Reserved — do not modify.
		CFG_PLL_LBW_3G	12:8	RW	8	2.97Gb/s (3G) loop bandwidth setting. See CFG_PLL_LBW_12G.
		RSVD	7:5	RW	0	Reserved — do not modify.
		CFG_PLL_LBW_HD	4:0	RW	8	1.485Gb/s (HD) loop bandwidth setting. See CFG_PLL_LBW_12G.
730C	PLL_LOOP_ BANDWIDTH_ SD_MADI	RSVD	15:13	RW	0	Reserved — do not modify.
		CFG_PLL_LBW_SD	12:8	RW	1C	270Mb/s (SD) loop bandwidth setting. See CFG_PLL_LBW_12G.
		RSVD	7:5	RW	0	Reserved — do not modify.
		CFG_PLL_LBW_MADI	4:0	RW	8	125Mb/s (MADI) loop bandwidth setting. See CFG_PLL_LBW_12G.
730D to 730F	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
GPIO Configuration						
7310	GPIO0_CFG	RSVD	15:9	RW	0	Reserved — do not modify.
		CFG_GPIO0_OUTPUT_ENA	8:8	RW	1	0 = Output disabled (tri-stated/ high impedance); GPIO pin is configured as an input. 1 = Output enabled.
		CFG_GPIO0_FUNCTION	7:0	RW	80	Function select for GPIO 0 pin. GPIO0 Output Functions: 00 = Output driven LOW 01 = Output driven HIGH 02 = PLL lock status 03 to 7F = Reserved 80 = LOS (Loss of Signal, inverse of Carrier Detect) 81 = CD (Carrier Detect) 82 = Reserved 83 = SD/$\overline{HD}$ status 84 = Rate detected [0] 85 = Rate detected [1] 86 = Rate detected [2] 87 = Reference clock (Only applicable to GPIO_1) 88 to FF = Reserved GPIO0 Input Functions: 00 to 81 = Reserved 82 = Output 1 disable control 83 to FF = Reserved
7311	GPIO1_CFG	RSVD	15:9	RW	0	Reserved — do not modify.
		CFG_GPIO1_OUTPUT_ENA	8:8	RW	1	See GPIO0_CFG.
		CFG_GPIO1_FUNCTION	7:0	RW	2	
7312	GPIO2_CFG	RSVD	15:9	RW	0	Reserved — do not modify.
		CFG_GPIO2_OUTPUT_ENA	8:8	RW	0	See GPIO0_CFG.
		CFG_GPIO2_FUNCTION	7:0	RW	86	
7313	GPIO3_CFG	RSVD	15:9	RW	0	Reserved — do not modify.
		CFG_GPIO3_OUTPUT_ENA	8:8	RW	0	See GPIO0_CFG.
		CFG_GPIO3_FUNCTION	7:0	RW	82	
Equalizer Configuration						
7314	RSVD	RSVD	15:0	RW	102	Reserved — do not modify.
7315	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
7316	RSVD	RSVD	15:0	RW	42	Reserved — do not modify.
7317	RSVD	RSVD	15:0	RW	1	Reserved — do not modify.
7318	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
7319	RSVD	RSVD	15:0	RW	1	Reserved — do not modify.
731A	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
731B	RSVD	RSVD	15:0	RW	1	Reserved — do not modify.
731C to 731D	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
731E	TREQ_INPUT_BOOST	RSVD	15:4	RW	0	Reserved — do not modify.
		CFG_TREQ_BOOST	3:1	RW	0	Trace equalizer boost setting: 0 to 6, where 0 is minimum boost setting and 6 is maximum boost setting. Settings correspond to the following equalizer gain values: TBD
		CFG_TREQ_CD_BOOST	0:0	RW	0	Select Trace Equalizer carrier detection boost setting: 0 = Set to maximum 1 = Use CFG_TREQ_BOOST setting
731F	TREQ_CD_HYSTERESIS	RSVD	15:8	RW	0	Reserved — do not modify.
		CFG_TREQ_CD_ASSERT_THRESH	7:4	RW	4	Sets assert threshold for trace equalizer carrier detect. 0 to 15, where 0 is minimum threshold and 15 is maximum threshold.
		CFG_TREQ_CD_DEASSERT_THRESH	3:0	RW	3	Sets de-assert threshold for trace equalizer carrier detect. 0 to 15 where 0 is minimum threshold and 15 is maximum threshold.
7320	RSVD	RSVD	15:0	RW	3	Reserved — do not modify.
7321	RSVD	RSVD	15:0	RW	F	Reserved — do not modify.
7322	RSVD	RSVD	15:0	RW	3FF	Reserved — do not modify.
7323 to 7325	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
Output Configuration						
7326	OUTPUT_CFG	RSVD	15:3	RW	0	Reserved — do not modify.
		CFG_OUTPUT1_ 3.3V_SUPPLY_MODE	2:2	RW	0	0 = 2.5V output supply 1 = 3.3V output supply Host must configure this setting based on the power supply connected to the cable driver for output 1.
		RSVD	1:1	RW	0	Reserved — do not modify.
		CFG_OUTPUT0_ 3.3V_SUPPLY_MODE	0:0	RW	0	0 = 2.5V output supply 1 = 3.3V output supply Host must configure this setting based on the power supply connected to the cable driver for output 0.
7327	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
7328	OUTPUT_ PARAM_CD_ SD_TD_0	RSVD	15:13	RW	0	Reserved — do not modify.
		CFG_OUTPUT1_CD_ SD_TD_PREEMPH_ WIDTH	12:8	RW	0	Configure pre-emphasis pulse width for MADI and SD data rates on SDO1. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse width to better match the channel loss response.
		RSVD	7:7	RW	0	Reserved — do not modify.
		CFG_OUTPUT1_CD_ SD_TD_PREEMPH_ PWRDWN	6:6	RW	1	Pre-emphasis power-down control for MADI and SD data rates on SDO1: 0 = Pre-emphasis driver powered-up (pre-emphasis enabled) 1 = Pre-emphasis driver powered-down (pre-emphasis disabled)
		CFG_OUTPUT1_CD_ SD_TD_PREEMPH_ AMPL	5:0	RW	0	Configure pre-emphasis pulse amplitude for MADI and SD data rates on SDO1. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse amplitude to better match the channel loss response.
7329	OUTPUT_ PARAM_CD_ SD_TD_1	RSVD	15:14	RW	0	Reserved — do not modify.
		CFG_OUTPUT1_CD_ SD_TD_DRIVER_ SWING	13:8	RW	12_d	Configure output swing for MADI and SD data rates on SDO1. Range: 0 to 50 decimal. Default value results in 800mVpp.
		RSVD	7:0	RW	80	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
732A	OUTPUT_PARAM_CD_SD_TD_2	RSVD	15:13	RW	0	Reserved — do not modify.
		CFG_OUTPUT0_CD_SD_TD_PREEMPH_WIDTH	12:8	RW	0	Configure pre-emphasis pulse width for MADI and SD data rates on SDO0. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse width to better match the channel loss response.
		RSVD	7:7	RW	0	Reserved — do not modify.
		CFG_OUTPUT0_CD_SD_TD_PREEMPH_PWRDWN	6:6	RW	1	Pre-emphasis power-down control for MADI and SD data rates on SDO0: 0 = Pre-emphasis driver powered-up (pre-emphasis enabled) 1 = Pre-emphasis driver powered-down (pre-emphasis disabled)
		CFG_OUTPUT0_CD_SD_TD_PREEMPH_AMPL	5:0	RW	0	Configure pre-emphasis pulse amplitude for MADI and SD data rates on SDO0. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse amplitude to better match the channel loss response.
732B	OUTPUT_PARAM_CD_SD_TD_3	RSVD	15:14	RW	0	Reserved — do not modify.
		CFG_OUTPUT0_CD_SD_TD_DRIVER_SWING	13:8	RW	12_d	Configure output swing for MADI and SD data rates on SDO0. Range: 0 to 50 decimal. Default value results in 800mVpp.
		RSVD	7:0	RW	80	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
732C	OUTPUT_PARAM_CD_HD_0	RSVD	15:13	RW	0	Reserved — do not modify.
		CFG_OUTPUT1_CD_HD_PREEMPH_WIDTH	12:8	RW	0	Configure pre-emphasis pulse width for HD and 3G data rates on SDO1. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse width to better match the channel loss response.
		RSVD	7:7	RW	0	Reserved — do not modify.
		CFG_OUTPUT1_CD_HD_PREEMPH_PWRDWN	6:6	RW	0	Pre-emphasis power-down control for HD and 3G data rates on SDO1: 0 = Pre-emphasis driver powered-up (pre-emphasis enabled) 1 = Pre-emphasis driver powered-down (pre-emphasis disabled).
		CFG_OUTPUT1_CD_HD_PREEMPH_AMPL	5:0	RW	0	Configure pre-emphasis pulse amplitude for HD and 3G data rates on SDO1. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse amplitude to better match the channel loss response.
732D	OUTPUT_PARAM_CD_HD_1	RSVD	15:14	RW	0	Reserved — do not modify.
		CFG_OUTPUT1_CD_HD_DRIVER_SWING	13:8	RW	25_d	Configure output swing for HD and 3G data rates on SDO1. Range: 0 to 50 decimal. Default value results in 800mVpp.
		RSVD	7:0	RW	20	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
732E	OUTPUT_ PARAM_CD_ HD_2	RSVD	15:13	RW	0	Reserved — do not modify.
		CFG_OUTPUT0_CD_HD_ PREEMPH_WIDTH	12:8	RW	0	Configure pre-emphasis pulse width for HD and 3G data rates on SDO0. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse width to better match the channel loss response.
		RSVD	7:7	RW	0	Reserved — do not modify.
		CFG_OUTPUT0_CD_HD_ PREEMPH_PWRDWN	6:6	RW	0	Pre-emphasis power-down control for HD and 3G data rates on SDO0: 0 = Pre-emphasis driver powered-up (pre-emphasis enabled) 1 = Pre-emphasis driver powered-down (pre-emphasis disabled).
		CFG_OUTPUT0_CD_HD_ PREEMPH_AMPL	5:0	RW	0	Configure pre-emphasis pulse amplitude for HD and 3G data rates on SDO0. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse amplitude to better match the channel loss response.
732F	OUTPUT_ PARAM_CD_ HD_3	RSVD	15:14	RW	0	Reserved — do not modify.
		CFG_OUTPUT0_CD_HD_ DRIVER_SWING	13:8	RW	25_d	Configure output swing for HD and 3G data rates on SDO0. Range: 0 to 50 decimal. Default value results in 800mVpp.
		RSVD	3:0	RW	20	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
7330	OUTPUT_PARAM_CD_UHD_0	RSVD	15:13	RW	0	Reserved — do not modify.
		CFG_OUTPUT1_CD_UHD_PREEMPH_WIDTH	12:8	RW	0	Configure pre-emphasis pulse width for 6G and 12G data rates on SDO1. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse width to better match the channel loss response.
		RSVD	7:7	RW	0	Reserved — do not modify.
		CFG_OUTPUT1_CD_UHD_PREEMPH_PWRDWN	6:6	RW	0	Pre-emphasis power-down control for 6G and 12G data rates on SDO1: 0 = Pre-emphasis driver powered up (pre-emphasis enabled) 1 = Pre-emphasis driver powered down (pre-emphasis disabled)
		CFG_OUTPUT1_CD_UHD_PREEMPH_AMPL	5:0	RW	0	Configure pre-emphasis pulse amplitude for 6G and 12G data rates on SDO1. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse amplitude to better match the channel loss response.
7331	OUTPUT_PARAM_CD_UHD_1	RSVD	15:14	RW	0	Reserved — do not modify.
		CFG_OUTPUT1_CD_UHD_DRIVER_SWING	13:8	RW	25_d	Configure output swing for 6G and 12G data rates on SDO1. Range: 0 to 50 decimal. Default value results in 800mVpp.
		RSVD	3:0	RW	30	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
7332	OUTPUT_PARAM_CD_UHD_2	RSVD	15:13	RW	0	Reserved — do not modify.
		CFG_OUTPUT0_CD_UHD_PREEMPH_WIDTH	12:8	RW	0	Configure pre-emphasis pulse width for 6G and 12G data rates on SDO0. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse width to better match the channel loss response.
		RSVD	7:7	RW	0	Reserved — do not modify.
		CFG_OUTPUT0_CD_UHD_PREEMPH_PWRDWN	6:6	RW	0	Pre-emphasis power-down control for 6G and 12G data rates on SDO0: 0 = Pre-emphasis driver powered up (pre-emphasis enabled) 1 = Pre-emphasis driver powered down (pre-emphasis disabled)
		CFG_OUTPUT0_CD_UHD_PREEMPH_AMPL	5:0	RW	0	Configure pre-emphasis pulse amplitude for 6G and 12G data rates on SDO0. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse amplitude to better match the channel loss response.
7333	OUTPUT_PARAM_CD_UHD_3	RSVD	15:14	RW	0	Reserved — do not modify.
		CFG_OUTPUT0_CD_UHD_DRIVER_SWING	13:8	RW	25_d	Configure output swing for 6G and 12G data rates on SDO0. Range: 0 to 50 decimal. Default value results in 800mVpp.
		RSVD	7:0	RW	30	Reserved — do not modify.
7334	RSVD	RSVD	15:0	RW	24	Reserved — do not modify.
7335	RSVD	RSVD	15:0	RW	112	Reserved — do not modify.
7336	RSVD	RSVD	15:0	RW	24	Reserved — do not modify.
7337	RSVD	RSVD	15:0	RW	112	Reserved — do not modify.
7338	RSVD	RSVD	15:0	RW	24	Reserved — do not modify.
7339	RSVD	RSVD	15:0	RW	112	Reserved — do not modify.
733A	RSVD	RSVD	15:0	RW	24	Reserved — do not modify.
733B	RSVD	RSVD	15:0	RW	112	Reserved — do not modify.
733C	RSVD	RSVD	15:0	RW	3AE	Reserved — do not modify.
733D	RSVD	RSVD	15:0	RW	FC	Reserved — do not modify.
733E	RSVD	RSVD	15:0	RW	3AE	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
733F	RSVD	RSVD	15:0	RW	FC	Reserved — do not modify.
7340	RSVD	RSVD	15:0	RW	2E	Reserved — do not modify.
7341	RSVD	RSVD	15:0	RW	D0	Reserved — do not modify.
7342	RSVD	RSVD	15:0	RW	2E	Reserved — do not modify.
7343	RSVD	RSVD	15:0	RW	D0	Reserved — do not modify.
7344	RSVD	RSVD	15:0	RW	3AE	Reserved — do not modify.
7345	RSVD	RSVD	15:0	RW	FA	Reserved — do not modify.
7346	RSVD	RSVD	15:0	RW	3AE	Reserved — do not modify.
7347	RSVD	RSVD	15:0	RW	FA	Reserved — do not modify.
7348	OUTPUT_SIG_SELECT	RSVD	15:4	RW	1	Reserved — do not modify.
		CTRL_OUTPUT0_DATA_INVERT	3:3	RW	0	Controls optional signal polarity inversion on output 0.
		CTRL_OUTPUT1_DATA_INVERT	2:2	RW	0	Controls optional signal polarity inversion on output 1.
		RSVD	1:1	RW	0	Reserved — do not modify.
		CTRL_OUTPUT1_SIGNAL_SEL	0:0	RW	0	Output 1 data/clock select: 0 = Data 1 = Clock (CDR recovered clock) Clock output is half rate of the recovered clock.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
7349	CONTROL _OUTPUT _MUTE	RSVD	15:6	RW	0	Reserved — do not modify.
		CTRL_OUTPUT1_AUTO _MUTE_DURING_RATE _SEARCH	5:5	RW	0	Auto mode control: 0 = Disable auto mode 1 = Enable auto mode during rate search When enabled, the output is muted during rate search or loss of signal.
		CTRL_OUTPUT0_AUTO _MUTE_DURING_RATE _SEARCH	4:4	RW	0	Auto mode control: 0 = Disable auto mode 1 = Enable auto mode during rate search When enabled, the output is muted during rate search or loss of signal.
		CTRL_OUTPUT1_ MANUAL_MUTE	3:3	RW	0	0 = Unmute 1 = Mute Controls mute for output 1 when CTRL_OUTPUT1_AUTO _MUTE is disabled.
		CTRL_OUTPUT1_AUTO _MUTE	2:2	RW	1	0 = Disable auto mode 1 = Enable auto mode Selects between auto or manual mute control for output 1.
		CTRL_OUTPUT0_ MANUAL_MUTE	1:1	RW	0	0 = Unmute 1 = Mute Controls mute for output 0when CTRL_OUTPUT0_AUTO _MUTE is disabled
		CTRL_OUTPUT0_AUTO _MUTE	0:0	RW	1	0 = Disable auto mode 1 = Enable auto mode Selects between auto or manual mute control for output 0.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
734A	CONTROL_ OUTPUT_ DISABLE	RSVD	15:4	RW	0	Reserved — do not modify.
		CTRL_OUTPUT1_ MANUAL_DISABLE	3:3	RW	0	0 = Enable output driver. 1 = Disable (power-down) output driver. Controls output disable for output 1 when CTRL_OUTPUT1_AUTO _DISABLE is disabled.
		CTRL_OUTPUT1_AUTO _DISABLE	2:2	RW	0	0 = Disable auto output disable mode. 1 = Enable auto output disable mode. Selects between auto or manual output disable for output 1. Disable mode overrides Mute mode.
		CTRL_OUTPUT0_ MANUAL_DISABLE	1:1	RW	0	0 = Enable output driver. 1 = Disable (power-down) output driver. Controls output disable for output 0 when CTRL_OUTPUT0_AUTO _DISABLE is disabled.
		CTRL_OUTPUT0_AUTO _DISABLE	0:0	RW	0	0 = Disable auto output disable mode. 1 = Enable auto output disable mode. Selects between auto or manual output disable for output 0. Disable mode overrides Mute mode.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
734B	CONTROL_ OUTPUT_ RATE_MODE	RSVD	15:11	RW	0	Reserved — do not modify.
		CTRL_OUTPUT1_ MANUAL_RATE_MODE	10:9	RW	2	0 = SD 1 = HD 2 = UHD Rate-specific control to enable compliant slew rate and optimal eye quality when CTRL_OUTPUT1_AUTO _RATE_MODE is disabled.
		CTRL_OUTPUT1_AUTO _RATE_MODE	8:8	RW	1	0 = Disable auto rate mode selection 1 = Enable auto rate mode selection Selects between auto or manual slew rate and eye quality selection for output 1.
		RSVD	7:3	RW	0	Reserved — do not modify.
		CTRL_OUTPUT0_ MANUAL_RATE_MODE	2:1	RW	2	0 = SD 1 = HD 2 = UHD Rate-specific control to enable compliant slew rate and optimal eye quality when CTRL_OUTPUT0_AUTO_ RATE_MODE is disabled.
		CTRL_OUTPUT0_ AUTO_RATE_MODE	0:0	RW	1	0 = Disable auto rate mode selection 1 = Enable auto rate mode selection Selects between auto or manual slew rate and eye quality selection for output 0.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
734C	CONTROL_ RETIMER_ BYPASS	RSVD	15:4	RW	0	Reserved — do not modify.
		CTRL_OUTPUT1_ RETIMER_MANUAL_ BYPASS	3:3	RW	0	0 = Disable re-timer bypass 1 = Enable re-timer bypass Controls re-timer bypass for output 1 when CTRL_OUTPUT1_ RETIMER_AUTO_BYPASS is disabled.
		CTRL_OUTPUT1_ RETIMER_AUTO_BYPASS	2:2	RW	1	0 = Disable auto mode 1 = Enable auto mode Selects between auto and manual control of re-timer bypass for output 1.
		CTRL_OUTPUT0_ RETIMER_MANUAL_ BYPASS	1:1	RW	0	0 = Disable re-timer bypass 1 = Enable re-timer bypass Controls re-timer bypass for output 0 when CTRL_OUTPUT0_ RETIMER_AUTO_BYPASS is disabled.
		CTRL_OUTPUT0_ RETIMER_AUTO_BYPASS	0:0	RW	1	0 = Disable auto mode 1 = Enable auto mode Selects between auto and manual control of re-timer bypass for output 0.
734D	CONTROL_ BALANCED_ MODE	RSVD	15:2	RW	0	Reserved — do not modify.
		CTRL_OUTPUT1_ BALANCED	1:1	RW	0	0 = Disable 1 = Enable Enable output balanced mode for SMPTE compliant return loss measurement. When enabled, Balanced mode overrides mute and disable settings.
		CTRL_OUTPUT0_ BALANCED	0:0	RW	0	0 = Disable 1 = Enable Enable output balanced mode for SMPTE compliant return loss measurement. When enabled, Balanced mode overrides mute and disable settings.
734E to 734F	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
7350	RSVD	RSVD	15:0	RW	C	Reserved — do not modify.
7351	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
7352	RSVD	RSVD	15:0	RW	180	Reserved — do not modify.
7353 to 7356	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
7357	RSVD	RSVD	15:0	RW	40	Reserved — do not modify.
7358 to 7359	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
735A	RSVD	RSVD	15:0	RW	3F8	Reserved — do not modify.
735B	RSVD	RSVD	15:0	RW	A	Reserved — do not modify.
735C	RSVD	RSVD	15:0	RW	2FE	Reserved — do not modify.
735D to 737C	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
737D	RSVD	RSVD	15:0	RW	C8	Reserved — do not modify.
737E to 737F	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.

Table 5-4: Status Descriptions

The registers in Table 5-4 are status registers and should not be written to, otherwise the status data will be invalid.

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Description
7380 to 7382	RSVD	RSVD	15:0	RW	Reserved — do not modify.
7383	DEVICE_ID	DEVICE_ID_REG	15:12	RW	Device Identification: 0 = GS12181 1 = GS12141
		RSVD	11:0	RW	Reserved — do not modify.
7384	STICKY_ COUNTS_0	STAT_CNT_PRI_CD_CHANGES	15:8	RW	Count of primary carrier detection status changes.
		RSVD	7:0	RW	Reserved — do not modify.
7385	STICKY_ COUNTS_1	STAT_CNT_RATE _CHANGES	15:8	RW	Count of rate changes.
		STAT_CNT_PLL_LOCK_CH ANGES	7:0	RW	Count of PLL lock status changes since last cleared.

Table 5-4: Status Descriptions (Continued)

The registers in Table 5-4 are status registers and should not be written to, otherwise the status data will be invalid.

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Description
7386	CURRENT_ STATUS_0	RSVD	15:15	RW	Reserved — do not modify.
		STAT_CLEAR_COUNTS_ST ATUS	14:13	RW	0 = Idle 1 = Reserved 2 = Indicates device has cleared the sticky counts 3 = Reserved Part of a four way handshake with CTRL_CLEAR_COUNTS (register 4). When STAT_CLEAR_COUNTS _STATUS = 0 (idle), host may clear sticky counts by setting CTRL_CLEAR_COUNTS = 1. Once the device reports STAT_CLEAR _COUNTS_STATUS = 2 (cleared), the host must reset CTRL_CLEAR _COUNTS to 0 for the device to reset STAT_CLEAR_COUNTS _STATUS to 0 (idle).
		STAT_LOCK	12:12	RW	0 = PLL is unlocked 1 = PLL is locked
		RSVD	11:8	RW	Reserved — do not modify.
		STAT_OUTPUT1_MODE	7:4	RW	00 = Cable Driver SD rate mode/all Trace Driver rates 01 = Cable Driver HD rate mode 02 = Cable Driver UHD rate mode 03 = Reserved 04 = Reserved 05 = Balanced 06 = Muted 07 = Disabled
		STAT_OUTPUT0_MODE	3:0	RW	See STAT_OUTPUT1_MODE.

Table 5-4: Status Descriptions (Continued)

The registers in Table 5-4 are status registers and should not be written to, otherwise the status data will be invalid.

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Description
7387	CURRENT_ STATUS_1	STAT_OUTPUT1_ DISABLE	15:15	RW	0 = Output 1 is not disabled 1 = Output 1 is disabled
		STAT_OUTPUT0_ DISABLE	14:14	RW	0 = Output 1 is not disabled 1 = Output 1 is disabled
		STAT_OUTPUT1_MUTE	13:13	RW	0 = Output 1 is not muted 1 = Output 1 is muted
		STAT_OUTPUT0_MUTE	12:12	RW	0 = Output 1 is not muted 1 = Output 1 is muted
		STAT_OUTPUT1_ RETIMER_BYPASS	11:11	RW	0 = Re-timer path to output 1 is not bypassed 1 = Re-timer path to output 1 is bypassed
		STAT_OUTPUT0_ RETIMER_BYPASS	10:10	RW	0 = Re-timer path to output 1 is not bypassed 1 = Re-timer path to output 1 is bypassed
		RSVD	9:9	RW	Reserved — do not modify.
		STAT_PRI_CD	8:8	RW	0 = Primary carrier is not detected 1 = Primary carrier is detected Primary carrier detection status.
		RSVD	7:7	RW	Reserved — do not modify.
		STAT_OUTPUT1_ RATE_MODE	6:5	RW	0 = SD rate mode 1 = HD rate mode 2 = UHD rate mode
		STAT_OUTPUT0_ RATE_MODE	4:3	RW	0 = SD rate mode 1 = HD rate mode 2 = UHD rate mode
7387	CURRENT_ STATUS_1	STAT_DETECTED_RATE	2:0	RW	0 = Unlocked 1 = MADI (125Mb/s) 2 = SD (270Mb/s) 3 = HD (1.485Gb/s) 4 = 3G (2.97Gb/s) 5 = 6G (5.94Gb/s) 6 = 12G (11.88Gb/s) 7 = Reserved
7388 to 7390	RSVD	RSVD	15:0	RW	Reserved — do not modify.

6. Application Information

6.1 Typical Application Circuit

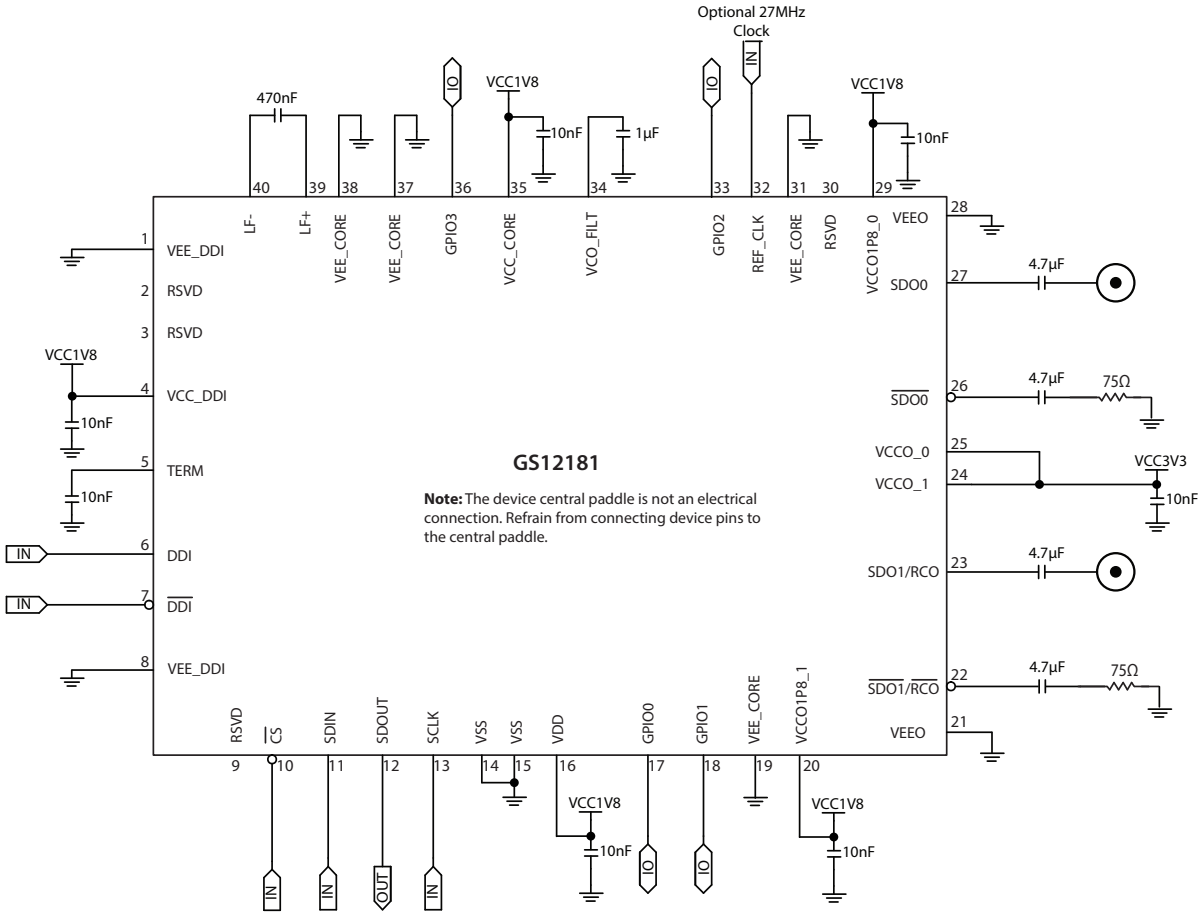


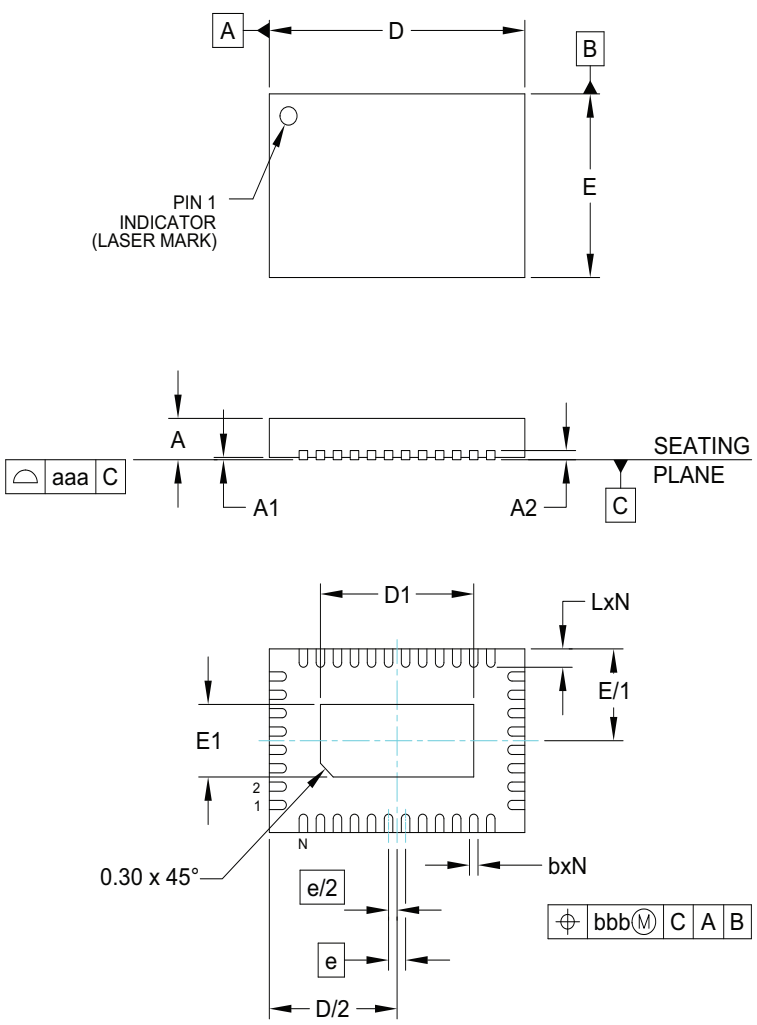
Figure 6-1: Typical Application Circuit

Note 1: 4.7µF AC-coupling capacitors are required on DDI and $\overline{\text{DDI}}$ when the upstream IC has an output common mode range that is incompatible with the input common mode range of the GS12181. Otherwise, DC-coupling may be used.

Note 2:VCCO_0 and VCCO_1 can be tied to two independent supplies running different voltages.

7. Package & Ordering Information

7.1 Package Dimensions



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		(0.02)	
b	0.15	0.20	0.25
D	5.95	6.00	6.05
D1	3.45	3.60	3.70
E	3.95	4.00	4.05
E1	1.43	1.58	1.68
e	0.40 BSC		
L	0.30	0.40	0.50
N	40		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DIMENSION OF LEAD WIDTH APPLIES TO TERMINAL AND IS MEASURED BETWEEN 0.15 to 0.30mm FROM THE TERMINAL TIP.

Figure 7-1: Package Dimensions

7.2 Recommended PCB Footprint

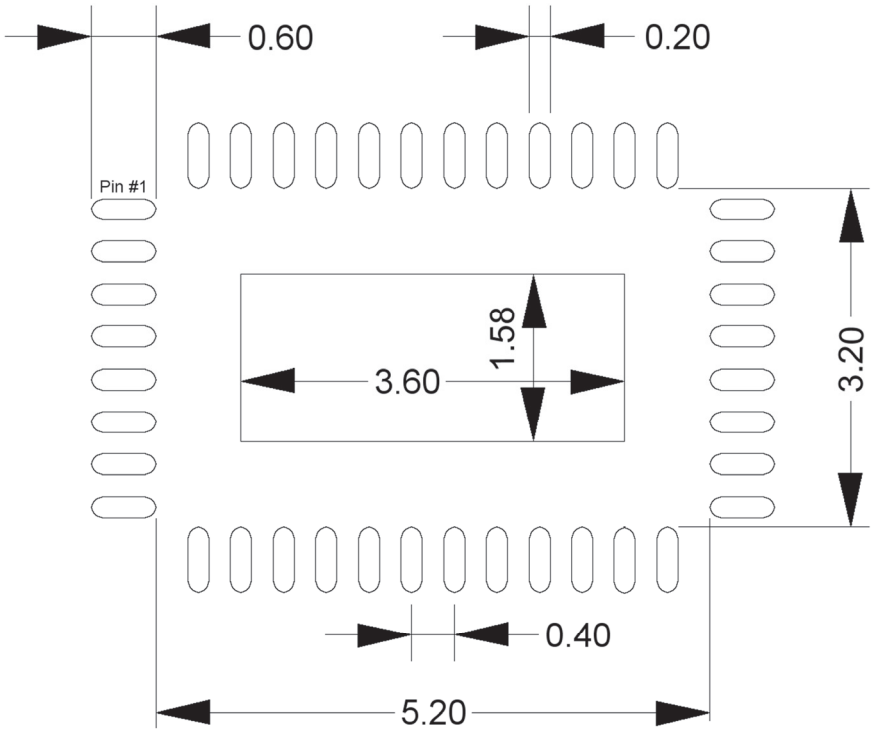


Figure 7-2: Recommended PCB Footprint

7.3 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	6mm x 4mm 40-pin QFN
Moisture Sensitivity Level	3
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	40.0°C/W
Junction to Board Thermal Resistance, θ_{j-b}	32.0°C/W
Junction to Case Thermal Resistance, θ_{j-c}	36.0°C/W
Psi, Ψ – Junction-to-Top Characterization Parameter	<1.0°C/W
Pb-free and RoHS compliant	Yes

7.4 Marking Diagram

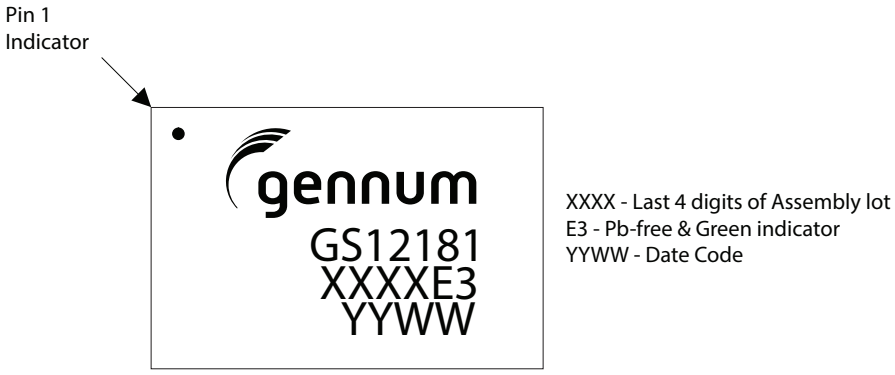


Figure 7-3: Marking Diagram

7.5 Solder Reflow Profiles

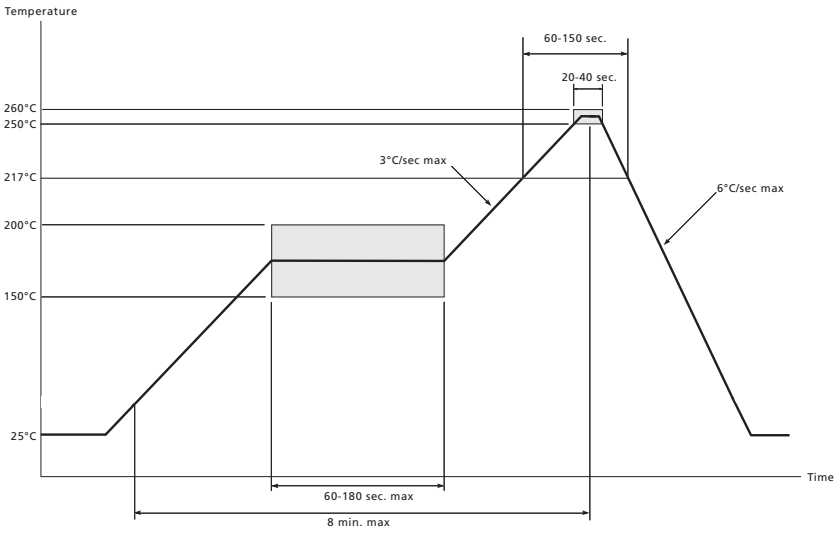


Figure 7-4: Maximum Pb-free Solder Reflow Profile

7.6 Ordering Information

Table 7-2: Ordering Information

Part Number	Minimum Order Quantity	Format
GS12181-INE3	490	Tray

Contact Information

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