CYPRESS SEMICONDUCTOR

Cascadeable 512 x 9 FIFO
Cascadeable 1024 x 9 FIFO
Cascadeable 2048 x 9 FIFO

Features

- **512 x 9, 1024 x 9, 2048 x 9 FIFO buffer memory**
- **Dual port RAM cell**
- **Asynchronous read/write**
- **High speed 25 MHz read/write independent of depth/width**
- **Low operating power**
  I_{CC} (max.) = 100 mA commercial
  I_{CC} (max.) = 120 mA military
- **Lower standby power**
  I_{CC} (max.) = 8 mA commercial
  I_{CC} (max.) = 15 mA military
- **Automatic power down**
- **Half full flag in standalone**
- **Empty and full flags**
- **Automatic retransmit in standalone**
- **Expandable in width and depth**
- **Parallel Cascade minimizes bubblethrough**
- **5V ±10% supply**
- **TTL compatible**
- **Three-state outputs**
- **CY7C412 pin compatible and functional equivalent to MK4501**

Functional Description

The CY7C412, CY7C424, and CY7C429 are, respectively, 512, 1024, and 2048 words by 9-bit wide first-in first-out (FIFO) memories organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent over-run and under-run. Three additional pins are also provided to facilitate expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays so that throughput is not reduced. Data is steered in a similar manner.

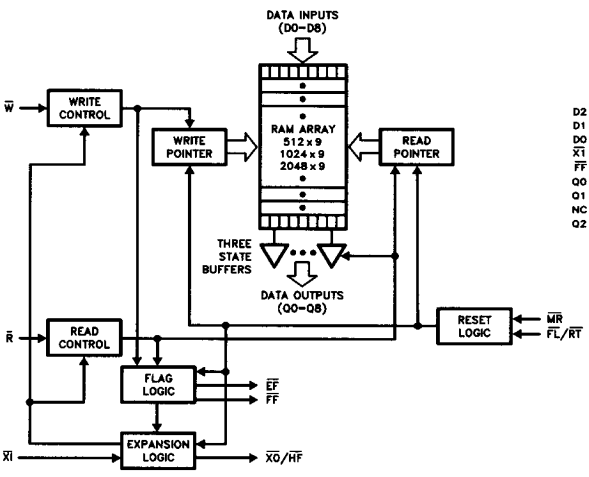
The read and write operations may be asynchronous; each can occur at a rate of 25 MHz. The write operation occurs when the Write ($\overline{W}$) signal is LOW and Read ($\overline{R}$) is HIGH. Read occurs when Read ($\overline{R}$) goes LOW and Write ($\overline{W}$) is HIGH. The 9 data outputs go to the high impedance state when $\overline{R}$ is HIGH.

A Half-Full ($\overline{HF}$) output flag is provided that is valid in the standalone and parallel expansion configurations. In the depth expansion configuration this pin is used to tell the next FIFO that it will be receiving data.

In the standalone and parallel expansion configurations a LOW on the Retransmit ($\overline{RT}$) input causes the FIFO's to retransmit the data. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must both be HIGH during retransmit.

The CY7C412, CY7C424, and CY7C429 are fabricated using an advanced 1.2 micron N-well CMOS technology. Input ESD protection is greater than 2000V and latchup is prevented by careful layout, guard rings and a substrate bias generator.

Logic Block Diagram



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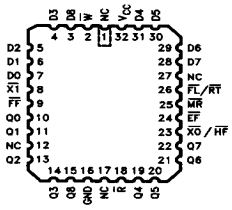
Pin Configurations

LCC
Top View



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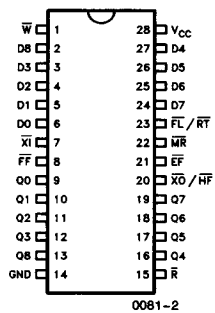
DIP
Top View



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Selection Guide

		7C412-30 7C424-30 7C429-30	7C412-40 7C424-40 7C429-40	7C412-65 7C424-65 7C429-65
Address Access Time (ns)		30	40	65
Maximum Operating Current (mA)	Commercial	100	100	100
	Military	120	120	120

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883 Method 3015.2)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		CY7C412 CY7C424 CY7C429 Min.	Max.	Units
V_{OH}	Output HIGH Voltgage	V_{CC} = Min., I_{OH} = −2 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, f = 25 MHz	Commercial		100	mA
			Military		120	mA
I_{SB}	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		8	mA
			Military		15	mA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−90	mA

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC} = 4.5V	7	

Notes:

1. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Load and Waveform

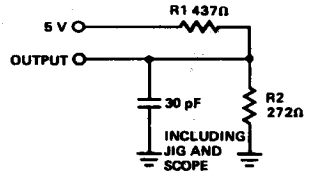

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Figure 1

Equivalent to: THÉVENIN EQUIVALENT

0081–6

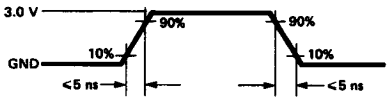

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Figure 2. All Input Pulses

Switching Characteristics Over the Operating Range[1]

Parameter	Description	7C412-30 7C424-30 7C429-30		7C412-40 7C424-40 7C429-40		7C412-65 7C424-65 7C429-65		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	40		50		80		ns
t_{AA}	Address to Data Valid		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		15		ns
t_{PR}	Read Pulse Width	30		40		65		ns
t_{LZR}	Read LOW to Low Z	5		5		10		ns
t_{DVR}	Read HIGH to Data Valid	5		5		5		ns
t_{HZR}	Read HIGH to High Z		20		25		30	ns
t_{WC}	Write Cycle Time	40		50		80		ns
t_{PW}	Write Pulse Width	30		40		65		ns
t_{LZW}	Write LOW to Low Z	10		10		15		ns
t_{WR}	Write Recovery Time	10		10		15		ns
t_{SD}	Data Set-Up Time	18		20		30		ns
t_{HD}	Data Hold Time	0		0		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	40		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	30		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		15		ns
t_{RTC}	Retransmit Cycle Time	40		50		80		ns
t_{PRT}	Retransmit Pulse Width	30		40		65		ns
t_{RTR}	Retransmit Recovery Time	10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		40		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		40		50		80	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		40		50		80	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		30		35		60	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		30		35		60	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		30		35		60	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		30		35		60	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		40		50		80	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		40		50		80	ns

Switching Characteristics Over the Operating Range[1] (Continued)

Parameter	Description	7C412-30 7C424-30 7C429-30		7C412-40 7C424-40 7C429-40		7C412-65 7C424-65 7C429-65		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RAE}	Effective Read from Write HIGH		30		35		60	ns
t_{RPE}	Effective Read Pulse Width after $\overline{EF}$ HIGH		30		40		65	ns
t_{WAF}	Effective Write from from Read HIGH		30		35		60	ns
t_{PWF}	Effective Write Pulse Width after $\overline{FF}$ HIGH		30		40		65	ns
t_{XOL}	Expansion Out LOW Delay from Clock		25		35		55	ns
t_{XOH}[2]	Expansion Out HIGH Delay from Clock		25		35		60	ns
t_{XCH}	Expansion Out HIGH Delay from Clock		35		35		60	ns
t_{PXF}	$\overline{XI}$ Pulse Width	30		40		60		ns
t_{XIR}	$\overline{XI}$ Recovery Time	10		10		15		ns
t_{XIS}	$\overline{XI}$ Set-Up to Write or Clock	15		15		25		ns

Notes:

1. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in *Figure 1a.*
2. t_{XOH} is guaranteed to be greater than or equal to t_{XOL} under all conditions.

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Architecture

The CY7C412/24/29 FIFOs consist of an array of 512/1024/2048 words of 9-bits each (implemented by a dual port RAM cell), a read pointer, a write pointer, control signals ($\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{XO}$, $\overline{FL}$, $\overline{RT}$, $\overline{MR}$) and Full, Half Full, and Empty flags.

Dual Port RAM

The dual port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Resetting the FIFO

Upon power up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half-Full ($\overline{HF}$) and Full flag ($\overline{FF}$) resetting to HIGH. Read ($\overline{R}$) and Write ($\overline{W}$) must be HIGH t_{RPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle.

Writing Data to the FIFO

The availability of an empty location is indicated by the HIGH state of the Full Flag ($\overline{FF}$). A falling edge of Write ($\overline{W}$) initiates a write cycle. Data appearing at the inputs (D0–D8) t_{DS} before and t_{DH} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The Empty flag ($\overline{EF}$) LOW to HIGH transition occurs t_{WEF} after the first write into an empty FIFO. The Half-Full flag ($\overline{HF}$) will go LOW on the falling edge of the write operation following the occurrence of half full. $\overline{HF}$ will remain LOW while the difference between the values of the read and write pointers is less than one half of the total memory of this device. The LOW to HIGH transition of the $\overline{HF}$ flag occurs on the rising edge of Read ($\overline{R}$). $\overline{HF}$ is available in Single Device Mode only. The Full flag ($\overline{FF}$) goes low on the falling edge of $\overline{W}$ after the last available location in the FIFO is written, prohibiting overflow. $\overline{FF}$ goes HIGH t_{RFF} after the completion of a valid read.

Reading Data from the FIFO

The falling edge of Read ($\overline{R}$) initiates a read cycle if the Empty flag ($\overline{EF}$) is not LOW. Data outputs (Q0–Q8) are in a high impedance condition between read operations ($\overline{R}$ HIGH), when the FIFO is empty, or when the FIFO is in the Depth Expansion Mode but is not the active device.

Architecture (Continued)

The falling edge of the last read before empty triggers a HIGH to LOW transition of $\overline{EF}$, prohibiting any further read operations until t_{WEF} after a valid write.

Retransmit

The Retransmit ($\overline{RT}$) input is active in the Single Device Mode only. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. The write pointer is unaffected. $\overline{R}$ and $\overline{W}$ must both be HIGH during a retransmit cycle.

Single Device/Width Expansion Modes

Single Device and Width Expansion Modes are entered by grounding $\overline{XI}$ during a $\overline{MR}$ cycle. During these modes the $\overline{HF}$ and $\overline{RT}$ features are available. FIFOs can be expanded in width to provide word widths greater than 9 in increments of 9. During Width Expansion Mode all control line inputs are common to all devices and flag outputs from any device can be monitored.

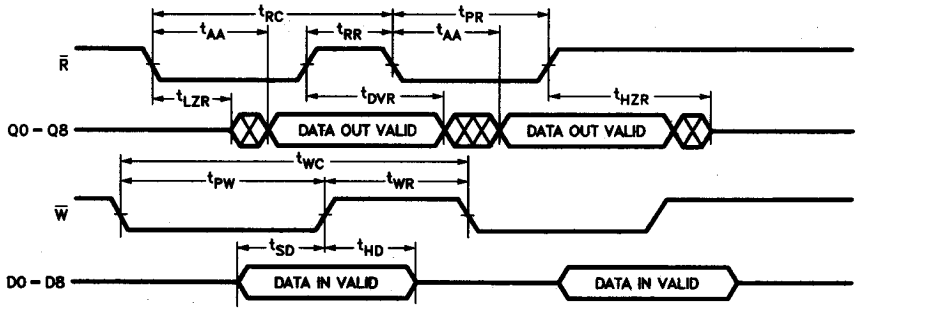
Depth Expansion Mode

Depth Expansion Mode is entered when, during a $\overline{MR}$ cycle, Expansion Out ($\overline{XO}$) of one device is connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the Depth Expansion Mode the First Load ($\overline{FL}$) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of a FIFO is written to and is pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one is enabled for write at any given time, all other devices are disabled.

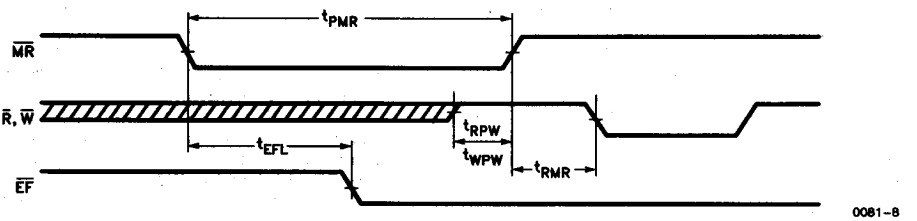
FIFOs can also be expanded simultaneously in depth and width to provide word widths greater than 9 in increments of 9. Consequently, any depth or width FIFO can be created. When expanding in depth, a composite $\overline{FF}$ must be created by OR-ing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by OR-ing the $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in Depth Expansion Mode.

Switching Waveforms

Asynchronous Read and Write Timing Diagram



Master Reset Timing Diagram

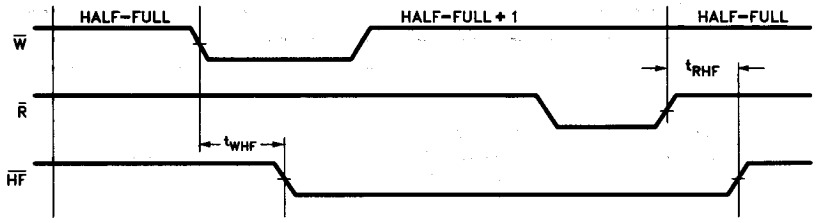


Notes:

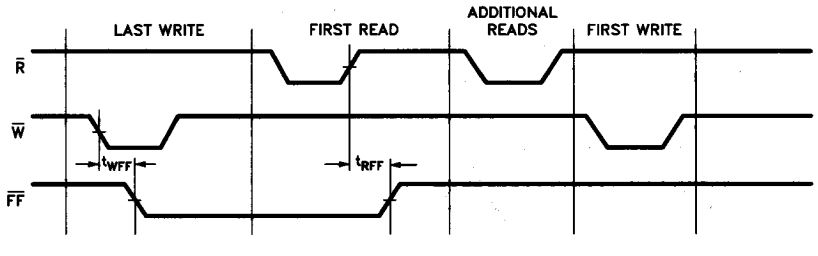
1. $t_{MRSC} = t_{PMR} + t_{RMR}$.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{MR}$.

Switching Waveforms (Continued)

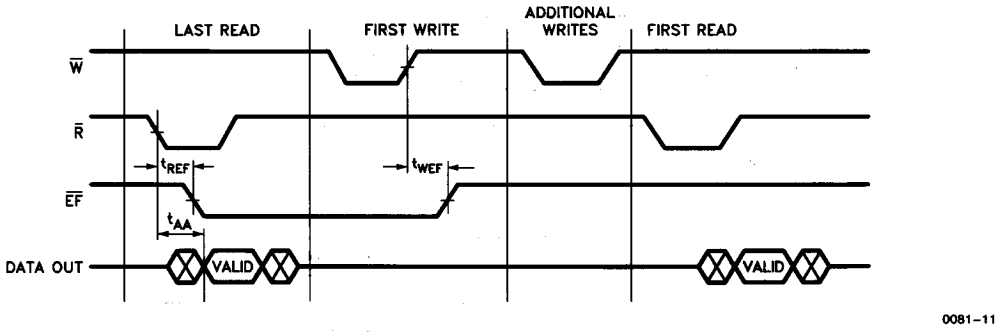
Half-Full Flag Timing Diagram



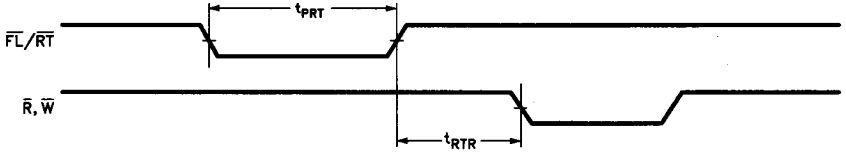
Last WRITE to First READ Full Flag Timing Diagram



Last READ to First WRITE Empty Flag Timing Diagram



Retransmit Timing Diagram

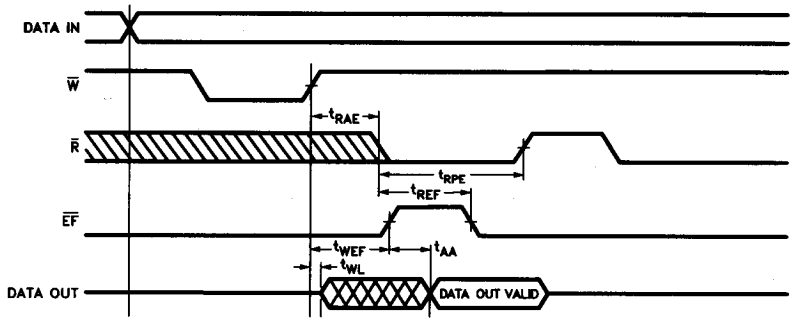


Notes:

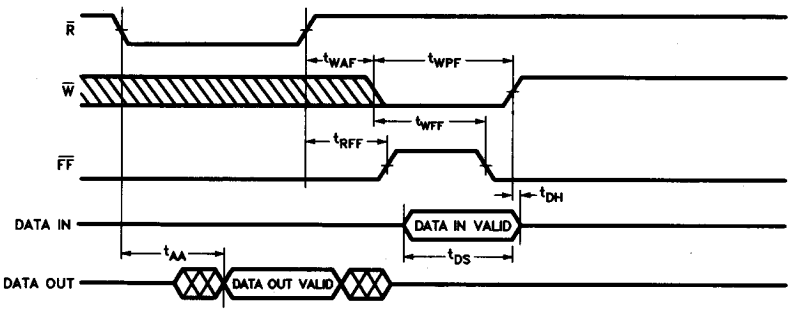
1. $t_{RTC} = t_{RT} + t_{RTR}$.
2. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Switching Waveforms (Continued)

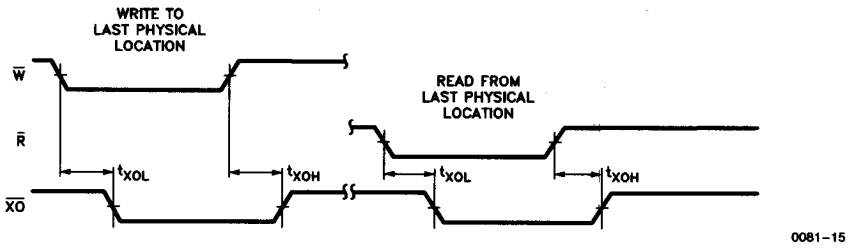
Empty Flag and Read Bubble-Through Mode Timing Diagram



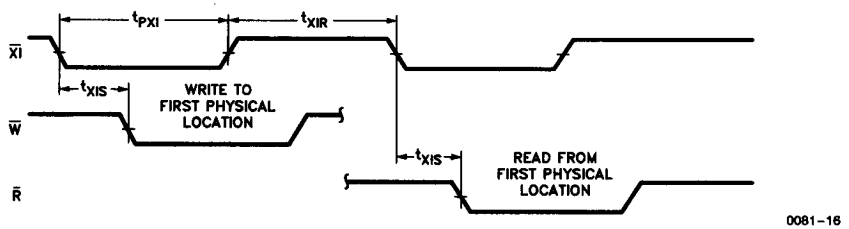
Full Flag and Write Bubble-Through Mode Timing Diagram



Expansion-Out Timing Diagram



Expansion-In Timing Diagram



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C412-30 PC	P15	Commercial
	CY7C412-30 JC	J65	
	CY7C412-30 DC	D16	
	CY7C412-30 LC	L55	
	CY7C412-30 DMB	L16	Military
	CY7C412-30 LMB	L55	
40	CY7C412-40 PC	P15	Commercial
	CY7C412-40 JC	J65	
	CY7C412-40 DC	D16	
	CY7C412-40 LC	L55	
	CY7C412-40 DMB	D16	Military
	CY7C412-40 LMB	L55	
65	CY7C412-65 PC	P15	Commercial
	CY7C412-65 JC	J65	
	CY7C412-65 DC	D16	
	CY7C412-65 LC	L55	
	CY7C412-65 DMB	D16	Military
	CY7C412-65 LMB	L55	

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C424-30 PC	P15	Commercial
	CY7C424-30 JC	J65	
	CY7C424-30 DC	D16	
	CY7C424-30 LC	L55	
	CY7C424-30 DMB	D16	Military
	CY7C424-30 LMB	L55	
40	CY7C424-40 PC	P15	Commercial
	CY7C424-40 JC	J65	
	CY7C424-40 DC	D16	
	CY7C424-40 LC	L55	
	CY7C424-40 DMB	D16	Military
	CY7C424-40 LMB	L55	
65	CY7C424-65 PC	P15	Commercial
	CY7C424-65 JC	J65	
	CY7C424-65 DC	D16	
	CY7C424-65 LC	L55	
	CY7C424-65 DMB	D16	Military
	CY7C424-65 LMB	L55	

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C429-30 PC	P15	Commercial
	CY7C429-30 JC	J65	
	CY7C429-30 DC	D16	
	CY7C429-30 LC	L55	
	CY7C429-30 DMB	D16	Military
	CY7C429-30 LMB	L55	
40	CY7C429-40 PC	P15	Commercial
	CY7C429-40 JC	J65	
	CY7C429-40 DC	D16	
	CY7C429-40 LC	L55	
	CY7C429-40 DMB	D16	Military
	CY7C429-40 LMB	L55	
65	CY7C429-65 PC	P15	Commercial
	CY7C429-65 JC	J65	
	CY7C429-65 DC	D16	
	CY7C429-65 LC	L55	
	CY7C429-65 DMB	D16	Military
	CY7C429-65 LMB	L55	

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