# ROHM
## SEMICONDUCTOR

STRUCTURE        Silicon Monolithic Integrated Circuit

TYPE        8 Channel Switching Regulator Controller and 1 Series Regulator for DVC

PRODUCT SERIES    **BD9833KV**

FEATURES
- ・ 8 DC/DC controller,1 Series Regulator
- ・ DC/DC controller: FET direct driver (Pch driver:7ch, Nch driver:1ch)
- ・ Series Regulator: Variable output voltage

    stable with Ceramic  Output Capacitor
- ・ Package: VQFP48C(0.5mm pitch)

○Absolute maximum ratings（Ta=25℃）

| Parameter | Symbol | Limits | Units |
|---|---|---|---|
| Power Supply Voltage1 | VCC,VIN2345,VIN6789 | 12 | V |
| Power Supply Voltage2 | VIN1 | 12 | V |
| Power Dissipation | Pd | 600(*1) | mW |
|  |  | 950(*2) | mW |
| Operating Temperature | Topr | -25～+85 | ℃ |
| Storage Temperature | Tstg | -55～+125 | ℃ |

(*1) Without external heat sink, the power dissipation degrades by 6.0mW/℃ above 25℃.

(*2) Power dissipation degrades by 9.5mW/℃ above 25℃, when mounted on a PCB (70.0mm×70.0mm×1.6mm).

○Recommended operating conditions（Ta=-25～+75℃）

| Parameter | Symbol | Spec. | Units |
|---|---|---|---|
| Power Supply Voltage | VCC,VIN2345,VIN6789 | 4.0～10 | V |
|  | VIN1 | 2.8～10 |  |
| Oscillator Frequency | fosc | 100kHz～1.2MHz |  |

Status of this document

○Electrical characteristics（Ta=25℃, VCC=7V, VIN1=7V STB=3V, unless otherwise specified）

| Parameter | Symbol | Spec. | | | Units | Conditions. |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max | | |
| **■DC/DC controller** | | | | | | |
| 【Reference Voltage】 | | | | | | |
| Reference Voltage | Vref | 2.475 | 2.500 | 2.525 | V | |
| Line Regulation | DVLi | - | - | 10 | mV | Vcc=4.0V~10V |
| Load Regulation | DVLo | - | - | 10 | mV | Iref=-0.1mA~ -1.0mA |
| Short-Circuit Output Current | Ios | -40 | -12 | -5 | mA | Vref=0V |
| 【Load Regulation】 | | | | | | |
| Short-Circuit Output Current1(VCC) | Vstd1 | 3.55 | 3.65 | 3.75 | V | VCC monitor Sweep down |
| Hysteresis width (VCC) | ΔVst1 | 0.6 | 0.11 | 0.16 | V | |
| Threshold Voltage 2(VREF) | Vstd2 | 2.2 | 2.3 | 2.4 | V | VREF monitor |
| 【Soft start】 | | | | | | |
| Soft standby voltage | Vsso1 | - | 10 | 100 | mV | |
| Input Source Current | ISOFT1 | -2.0 | -1.0 | -0.5 | μA | |
| 【Protection Circuit】 | | | | | | |
| INV Threshold Voltage | Vscpth | 0.65 | 0.75 | 0.85 | V | CH2,3,4,5,6,7, INV Voltage"L" detect |
| SCP Output Current | Iscp | -3.0 | -2.0 | -1.5 | μA | VSCP=0.75V |
| SCP Threshold Voltage | Vtsc | 1.4 | 1.5 | 1.6 | V | |
| SCP Standby Voltage | Vssc | - | 10 | 100 | mV | |
| 【Triangular wave oscillator】 | | | | | | |
| Oscillator Frequency | fosc | 580 | 680 | 780 | kHz | RT=11kohm,CT=180pF |
| Frequency Stability (Vcc) | Df | - | 0.3 | 2 | % | VCC=4.0~10V |
| RT Output Voltage | VRT | 0.95 | 1.00 | 1.05 | V | |
| **■DC/DC controller** | | | | | | |
| 【Reference Voltage】 | Vthea | 0.980 | 1.00 | 1.020 | V | CH2,3,4,5,6,7 |
| Reference Voltage | VOFST | - | - | 10 | mV | CH8,9 |
| Line Regulation | Ibias1 | -150 | 0 | 150 | nA | CH2,3,4,5,6,7 INV pin |
| Load Regulation | Ibias2 | -170 | -40 | - | nA | CH8,9 INV pin |
| Short-Circuit Output Current | Ibias3 | -170 | -40 | - | nA | CH8,9 NON pin |
| 【Load Regulation】 | AV | 50 | 65 | 80 | dB | DC Design Guarantee |
| Short-Circuit Output Current1(VCC) | BW | 0.5 | 1 | 2 | MHz | AV=0dB Design Guarantee |
| Hysteresis width (VCC) | Vfbh | Vref -0.1 | - | - | V | |
| Threshold Voltage 2(VREF) | Vfbl | - | - | 0.1 | V | |
| 【Soft start】 | Isink1 | 1.3 | 2.6 | 3.9 | mA | |
| Soft standby voltage | Isink2 | 3.4 | 6.7 | 10 | mA | |
| Input Source Current | Isource1 | -240 | -150 | -90 | μA | |
| 【Protection Circuit】 | Isource2 | -280 | -190 | -130 | μA | |
| INV Threshold Voltage | VCM | 0 | - | VCC-2 | V | |
| 【PWM Comparator】 | | | | | | |
| Input Threshold Voltage 2,3,4,5,6,7,8,9 | Vt0 | 1.730 | 1.820 | 1.910 | V | DUTY0% |
| | Vt100 | 2.090 | 2.180 | 2.270 | V | DUTY100% |
| 【FET Driver】 | | | | | | |
| ON Resistance | RonHI1 | 7 | 14 | 21 | Ω | VG2, 3, 4, 5, 6, 7, 8, 9 VG="H" |
| | RonLO1 | 6 | 12 | 18 | Ω | VG2, 3, 4, 5, 6, 7, 8, 9 VG="L" |
| Current Ability | Isink1 | 70 | 170 | 250 | mA | VG2, 3, 4, 5, 6, 7, 8, 9 VG="L" |
| | Isource1 | -240 | -160 | -80 | mA | VG2, 3, 4, 5, 6, 7, 8, 9 VG="H" |
| 【Control】 | | | | | | |
| STB Threshold Voltage | Vstb | 1.0 | 1.5 | 2.0 | V | |
| STB Input Current | Istb | - | - | 30 | μA | STB=3V |
| STB5,6 Threshold Voltage | Vstb5,6 | 1.0 | 1.5 | 2.0 | V | |
| STB5,6 Input Current | Istb5,6 | - | - | 30 | μA | STB5, 6=3V |
| 【Circuit Current】 | | | | | | |
| Standby Current | Iccs | - | 0 | 5 | μA | STB=0V |
| Circuit Current on Driving | Icc | 1 | 5 | 10 | mA | |
| 【Series Regulator】 | | | | | | |
| Output Voltage | Vo1 | 2.94 | 3.00 | 3.06 | V | R1=200KΩ, R2=100KΩRefer to below figure |
| Reference Voltage | VFB1 | 0.98 | 1.00 | 1.02 | V | |
| Output Current Ability | Io1 | 300 | - | - | mA | |
| The Difference between Input voltage and output voltage | DV1 | 70 | 120 | 250 | mV | VIN1=VOUT1x0.97, IOUT1=20mA |
| Line Regulation11 | DVLi11 | - | 4 | 10 | mV | VIN1=4V to10V IOUT1=100mA |
| Line Regulation12 | DVLi12 | - | 4 | 10 | mV | VIN1=3.5V to10V IOUT1=10mA |
| Load Regulation1 | DVLo1 | - | 10 | 30 | mV | IOUT1=1mA to 100mA |
| Load Regulation2 | DVLo2 | - | 30 | 90 | mV | IOUT1=1mA to 300mA |
| Short-Circuit Output Current | Ios1 | -140 | -70 | -35 | mA | VOUT1=0V |
| Circuit Current | IVIN1 | 40 | 80 | 160 | μA | IOUT1=0mA |
| VOUT1 pin Connect Capacitor | COUT | 2.2 | - | - | μF | |

REV. B

○Package Dimensions



BD9833KV

LOT No.
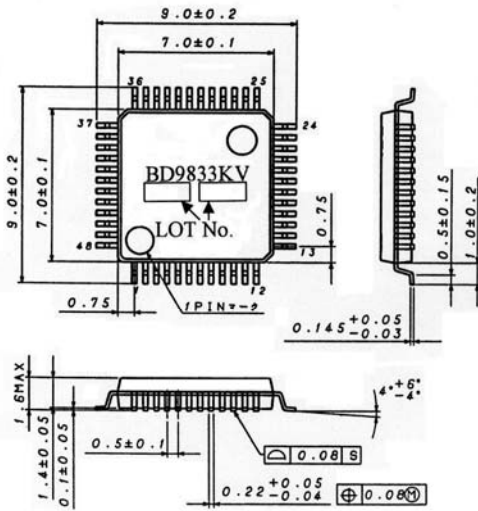
VQFP48C （Unit:mm）

○Block Diagram
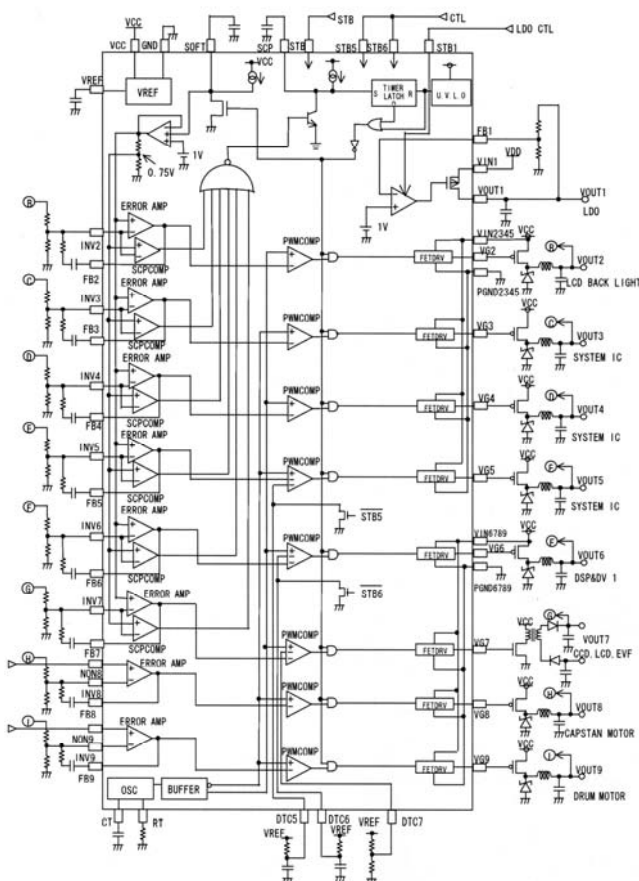


○Pin Description

| 番号 | 端子名 | 機能 |
|---|---|---|
| 1 | INV5 | Error Amp inverted input（CH5） |
| 2 | FB5 | Error Amp output (CH5) |
| 3 | INV6 | Error Amp inverted input（CH6） |
| 4 | FB6 | Error Amp output (CH6) |
| 5 | INV7 | Error Amp inverted input（CH7） |
| 6 | FB7 | Error Amp output (CH7) |
| 7 | NON8 | Error Amp non-inverted input（CH8） |
| 8 | INV8 | Error Amp inverted input（CH8） |
| 9 | FB8 | Error Amp output (CH8) |
| 10 | NON9 | Error Amp non-inverted input（CH9） |
| 11 | INV9 | Error Amp inverted input（CH9） |
| 12 | FB9 | Error Amp output (CH9) |
| 13 | VG9 | FET Driver Output (CH9) |
| 14 | VG8 | FET Driver Output (CH8) |
| 15 | VIN6789 | Power supply for the output circuit (CH6,7,8,9) |
| 16 | PGND6789 | Power Ground for the output circuit (CH6,7,8,9) |
| 17 | VG7 | FET Driver Output (CH7) |
| 18 | VG6 | FET Driver Output (CH6) |
| 19 | VG5 | FET Driver Output (CH5) |
| 20 | VG4 | FET Driver Output (CH4) |
| 21 | VIN2345 | Power supply for the output circuit (CH2,3,4,5) |
| 22 | PGND2345 | Power Ground for the output circuit (CH2,3,4,5) |
| 23 | VG3 | FET Driver Output (CH3) |
| 24 | VG2 | FET Driver Output (CH2) |
| 25 | FB2 | Error Amp output (CH2) |
| 26 | INV2 | Error Amp inverted input（CH2） |
| 27 | FB3 | Error Amp output (CH3) |
| 28 | INV3 | Error Amp inverted input（CH3） |
| 29 | STB | SW for CH2〜9, Hi：Operating |
| 30 | GND | Ground |
| 31 | FB4 | Error Amp output (CH4) |
| 32 | INV4 | Error Amp inverted input（CH4） |
| 33 | STB5 | SW for CH5, Hi：Operating |
| 34 | STB6 | SW for CH6, Hi：Operating |
| 35 | STB1 | SW for CH1, Hi：Operating |
| 36 | VOUT1 | Series Regulator Output |
| 37 | VIN1 | Power supply for Series Regulator |
| 38 | FB1 | Amp inverted input |
| 39 | N. C. | Non-Connected pin |
| 40 | SCP | A capacitor is placed to set up the delay time of the SCP |
| 41 | SOFT | Soft start/This pin connects to a capacitor to set up the start-up time |
| 42 | VREF | Reference Voltage Output pin |
| 43 | VCC | Power supply for DC/DC |
| 44 | CT | A capacitor is to set up the triangular-wave frequency |
| 45 | RT | A resistor is to set up the triangular-wave frequency |
| 46 | DTC5 | Dead time control pin for CH5 |
| 47 | DTC6 | Dead time control pin for CH6 |
| 48 | DTC7 | Dead time control pin for CH7.And this pin connects to a capacitor to set up the start-up time. |

## ○Operation Notes

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC deterioration or damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions. In addition, ensure that no pins other than the GND pin carry a voltage lower than or equal to the GND pin, including during actual transient phenomena.

3) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pin caused by the presence of a foreign object may result in damage to the IC.

5) Operation in a strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6) Thermal shutdown circuit (TSD circuit)

This IC incorporates a built-in thermal shutdown circuit (TSD circuit). The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of the thermal shutdown circuit is assumed.

7) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

8) Common impedance

Power supply and ground wiring should reflect consideration of the need to lower common impedance and minimize ripple as much as possible (by making wiring as short and thick as possible or rejecting ripple by incorporating inductance and capacitance).

9) Applications with modes that reverse VCC and pin potentials may cause damage to internal IC circuits.

For example, such damage might occur when VCC is shorted with the GND pin while an external capacitor is charged. It is recommended to insert a diode for preventing back current flow in series with VCC or bypass diodes between VCC and each pin.
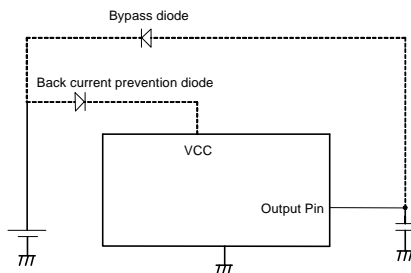


10) Timing resistor

Timing resistor connected between RT and GND, has to be placed near RT terminal (45pin). With the connection must be as short as possible.

11) IC pin input

This monolithic IC contains P+ isolation and PCB layers between adjacent elements in order to keep them isolated.
P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.
For example, when a resistor and transistor are connected to pins as shown in follow chart,

○ the P/N junction functions as a parasitic diode when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).

○ Similarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (PCB) voltage to input and output pins.



REV. B
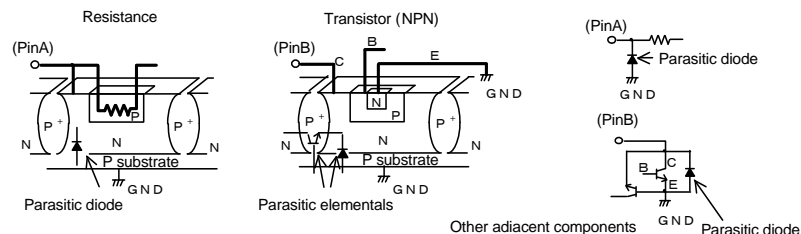
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