MN4052B / MN4052BS

Dual 4-Channel Analog Multiplexers

■ Description

The MN4052B/S are dual 4-channel analog multiplexer/demultiplexers which enable selection of digital or analog signals and their complexes.
Each channel is established by controlling signals of the enable input (E). The inputs/outputs can swing between V_{DD} and V_{EE} ($\leqq$ 15V) even if the amplitude of control signals is below V_{DD}.
It can be controlled to low impedance circuit because the impedance of the switch is very low. The MN4052B/S are equivalent to MOTOROLA MC14052B and RCA CD4052B.

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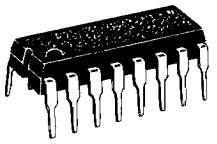


16-Pin • Plastic DIL Package

P- 4

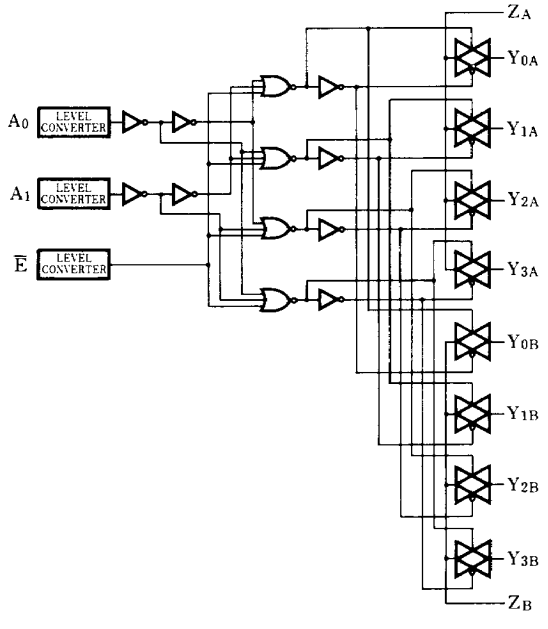
16-Pin • Panaflat Package (SO-16D)

■ Truth Table

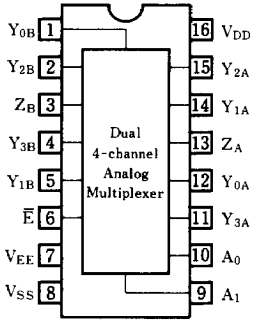
Input			Channel ON
$\overline{E}$	A_1	A_0	
L	L	L	$Y_{0A}-Z_A$; $Y_{0B}-Z_B$
L	L	H	$Y_{1A}-Z_A$; $Y_{1B}-Z_B$
L	H	L	$Y_{2A}-Z_A$; $Y_{2B}-Z_B$
L	H	H	$Y_{3A}-Z_A$; $Y_{3B}-Z_B$
H	×	×	All OFF

Note) × : don't care

■ Logic Diagram



Pin Configuration



Pin Explanation

Y_{0A}~Y_{3A} : Analog input/output
Y_{0B}~Y_{3B} : Analog input/output
A_0, A_1 : Address input
$\overline{E}$: Enable input
Z_A, Z_B : Common input/output

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■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

■ DC Characteristics (Ta=25℃, V_{SS}=0V)

Item	$V_{DD}-V_{EE}$ (V)	Symbol	Conditions	min.	typ.	max.	Unit
On Resistance	5	R_{ON}	V_I=5V	—	200	800	Ω
			V_I=2.5V	—	550	1300	
			V_I=0.25V	—	200	800	
On Resistance	10	R_{ON}	V_I=10V	—	80	300	Ω
			V_I=5V	—	100	350	
			V_I=0.25V	—	80	300	
On Resistance	15	R_{ON}	V_I=15V	—	60	200	Ω
			V_I=7.5V	—	80	250	
			V_I=0.25V	—	60	200	

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■ Switching Characteristics (Ta=25℃, V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions	min.	typ.	max.	Unit
Propagation Delay Time (Fig. 1) Vis→V_{OS} (H→L)	5	t_{PHL}	R_L=10kΩ, C_L=50pF, $\overline{E}$=V_{SS}	—	10	30	ns
	10			—	5	15	
	15			—	5	15	
Propagation Delay Time (Fig. 1) Vis→V_{OS} (L→H)	5	t_{PLH}		—	10	30	ns
	10			—	5	15	
	15			—	5	15	
Propagation Delay Time (Fig. 1) An→V_{OS} (H→L)	5	t_{PHL}	R_L=10kΩ, C_L=50pF, $\overline{E}$=V_{SS}	—	150	450	ns
	10			—	65	195	
	15			—	50	150	
Propagation Delay Time (Fig. 1) An→V_{OS} (L→H)	5	t_{PLH}		—	75	225	ns
	10			—	35	105	
	15			—	30	90	
Output Disable Time (Fig. 1) $\overline{E}$→V_{OS} (H)	5	t_{PHZ}	R_L=10kΩ, C_L=50pF, $\overline{E}$=V_{DD}	—	100	300	ns
	10			—	90	270	
	15			—	90	270	
Output Disable Time (Fig. 1) $\overline{E}$→V_{OS} (L)	5	t_{PLZ}		—	95	285	ns
	10			—	90	270	
	15			—	90	270	
Output Enable Time (Fig. 1) $\overline{E}$→V_{OS} (H)	5	t_{PZH}	R_L=10kΩ, C_L=50pF, $\overline{E}$=V_{DD}	—	130	390	ns
	10			—	55	165	
	15			—	45	135	
Output Enable Time (Fig. 1) $\overline{E}$→V_{OS} (L)	5	t_{PZL}		—	120	360	ns
	10			—	50	150	
	15			—	35	105	
Sine Wave Distortion (Fig. 2)	5		R_L=10kΩ, C_L=15pF, fis=1 kHz, Vis=$\frac{1}{2}V_{DD(P\text{-}P)}$	—	0.25	—	%
	10			—	0.04	—	
	15			—	0.04	—	
Crosstalk (Fig. 3) (Between 2 Channels)	5		R_L=1 kΩ, Vis=$\frac{1}{2}V_{DD(P\text{-}P)}$	—	—	—	MHz
	10			—	1	—	
	15			—	—	—	
Crosstalk (Fig. 1) (Address Input→Output)	5		R_L=10kΩ, C_L=15pF, $\overline{E}$ or An=V_{DD}	—	—	—	mV
	10			—	50	—	
	15			—	—	—	
Propagation Frequency (Fig. 2) (Note 2)	5		R_L=1 kΩ, C_L=5 pF, Vis=$\frac{1}{2}V_{DD(P\text{-}P)}$	—	—	—	MHz
	10			—	1	—	
	15			—	—	—	
Feedthrough (Fig. 2) (Note 1) (OFF)	5		R_L=1 kΩ, C_L=5 pF, Vis=$\frac{1}{2}V_{DD(P\text{-}P)}$	—	13	—	MHz
	10			—	40	—	
	15			—	70	—	
Input Capacitance		C_I		—	—	7.5	pF

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Fig. 1 Propagation Delay Time, Output Disable/Enable Time, Crosstalk Test Circuit

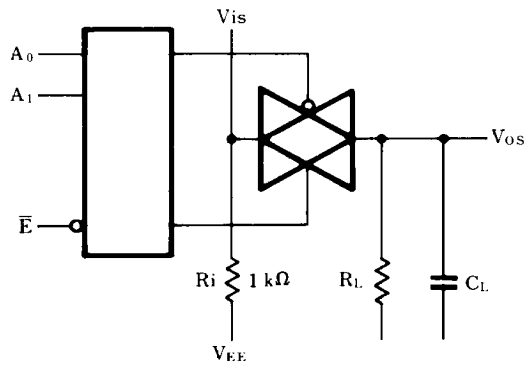
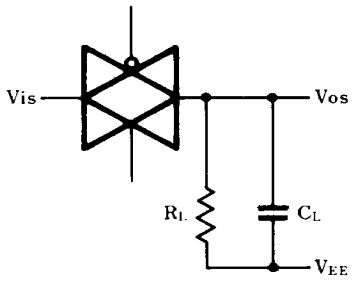


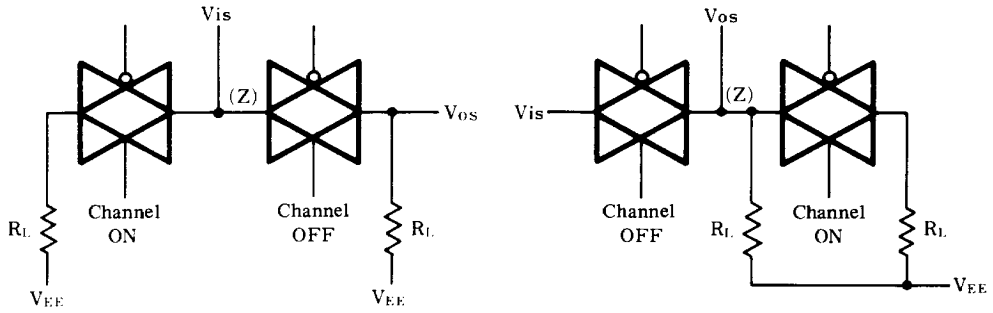
Fig. 2 Sine Wave Distortion, Feedthrough, Frequency Response, Test Circuit



(注1) $20 \log \frac{Vos}{Vis} = -50\,dB$

(注2) $20 \log \frac{Vos}{Vis} = -3\,dB$

Fig. 3 Crosstalk Test Circuit



$$20 \log \frac{V_{OS}}{Vis} = -50\,dB$$

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