# MN3101

## CLOCK GENERATOR/DRIVER CMOS LSI FOR BBD

#### Description

The MN3101 is a CMOS LSI generating two phase clock signal of low output impedance to drive MN3000 series BBD. Built-in  $V_{\rm GG}$  power supply circuit for the MN3000 series BBD\* provides most suitable  $V_{\rm GG}$  voltage for the BBD when the MN3101 is used with the same power source as BBD. Oscillation is abled by external resistors and capacitors, and also oscillation drive is possible by the separate excitation oscillation.

Clock signal frequency is 1/2 of oscillation frequency.

\* MN3000 series BBDs

MN3001, MN3002, MN3003, MN3004, MN3005, MN3006 MN3007, MN3008, MN3009, MN3010, MN3011, MN3012.

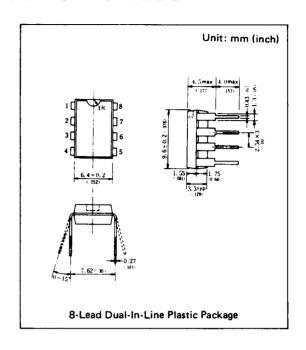
Note) Clock signal generator is built-in the MN3003 and MN3012.

#### ■ Features

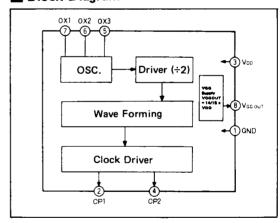
- BBD direct driving capability of up to two MN3005s (equivalent to 8192-stages).
- Self and separate oscillations.
- Two phase clock output (Duty: 1/2).
- V<sub>GG</sub> voltage generator is built-in for the BBD.
- Single power supply: −8 ~ −16V.
- 8-Lead Dual-In-Line Plastic Package.

#### Applications

BBD clock generator/driver.



#### **■** Block Diagram



## ■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Remarks
Drain Supply Voltage	V <sub>DD</sub>	-18~+0.3	V	GND=0V
Input Terminal Voltage	Vı	V <sub>DD</sub> -0.3~+0.3	V	GND=0V
Output Terminal Voltage	Vo	V <sub>DD</sub> -0.3~+0.3	V	GND=0V
Power Dissipation	P <sub>D</sub>	200	mW	
Operating Ambient Temperature	Topr	<del>-10</del> ~+70	Ĉ	
Storage Temperature	Tstg	-30~+125	°	

## **■** Operating Condition (Ta = 25°C)

Item	Symbol	Condition	Min.	Тур.	Max.	Unit
Drain Supply Voltage	V <sub>DD</sub>	GND= 0 V	<b>-8</b>	—15	<b>-16</b>	٧

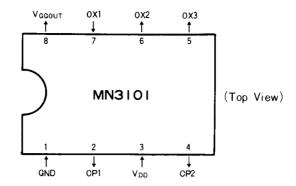
## ■ Electrical Characteristics (Ta = $25^{\circ}$ C, $V_{DD}$ = -15V, GND = 0V)

Item Symbol		Condition	Min.	Тур.	Max.	Unit
Input drain current	I <sub>DD</sub>	No loard		3		mΑ
Total Power Dissipation	P <sub>tot</sub>	Clock output 40kHz		45		mW
OX1 Input Terminal						
Voltage "H" Level	V <sub>iH</sub>		0		-1	٧
Voltage "L" Level	V <sub>IL</sub>		V <sub>DD</sub> + 1		V <sub>DD</sub>	٧
Input Leakage Current	ILK	$V_1 = 0 \sim -15V$			30	μΑ
OX2 Output Terminal	<u> </u>		•		•	
Output Current "H" Level	Іо́н1	V <sub>0</sub> =-1 V	0.6			mA
Output Current "L" Level	I <sub>OL1</sub>	V <sub>0</sub> =-14V	0.5			mA
Output Leakage Current	I <sub>LOL1</sub>	$V_0 = V_{DD}$			30	μΑ
Output Leakage Current	I <sub>LOH1</sub>	V <sub>0</sub> =GND			30	μΑ
OX3 Output Temrinal						
Output Current "H" Level	I <sub>OH2</sub>	V <sub>0</sub> =-1 V	1.5	-		mA
Output Current "L" Level	I <sub>OL2</sub>	V <sub>0</sub> =-14V	2			mA
Output Leakage Current	I <sub>LOL2</sub>	$V_0 = V_{DD}$			30	μΑ
Output Leakage Current		V <sub>0</sub> =GND			30	μΑ
CP1, CP2 Output Terminal			· · · · · · · · · · · · · · · · · · ·			
Output Current "H" Level	Іонз	$V_0 = -1 V$	10			mΑ
Output Current "L" Level	I <sub>OL3</sub>	$V_0 = -14V$	10			mA
Output Leakage Current	I <sub>LOL3</sub>	$V_0 = V_{DD}$			30	μΔ
Output Leakage Current	I <sub>LOH3</sub>	V <sub>0</sub> =GND			30	μΑ
V <sub>GG OUT</sub> Output Terminal (*)						
Output Voltage	V <sub>GG</sub> OUT			-14		٧

<sup>(\*)</sup> This terminal generates  $V_{GG}$  voltage exclusively applied for BBD manufactured by Matsushita Electronics Corporation, therefore, some times it might not be applicable for the device other than the  $V_{GG}$  voltage of MEC's BBD.  $V_{GG\ OUT}$  changes by following formula depending on the value of  $V_{DD}$ .

$$V_{GG\ OUT}\ \doteqdot \frac{14}{15}\ V_{DD}$$

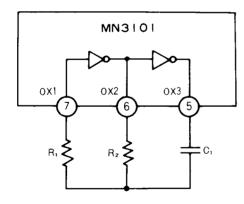
## **■** Terminal Assignments



### Terminal Description

Terminal No.	Symbol	I/O	Terminal Name	Description		
1	GND	Power supply	Ground	Connected to GND of the circuit.		
2	CP1	0	Clock output 1	This terminal outputs clock signal that is a revers phase of CP2 with Duty 1/2, 1/2 frequency of oscillation frequency		
3	V <sub>DD</sub>	Power supply	V <sub>DD</sub> apply	-15V is applied.		
4	CP 2	0	Clock output 2	This terminal outputs clock signal that is a reverse phase of CP 1.		
5	OX 3	0		C, R are connected in case	In case of separate excita-	
6	OX 2	0	C and R is connected.	of selfoscillation. (Refer to oscillation	tion, OX3 and OX2 are	
7	OX 1	1		circuit).	opened and OX1 is set to OSC input.	
8	V <sub>GG</sub> OUT	0	V <sub>GG</sub> voltage output.	$-14V$ is output. $(V_{DD} = -15V) V_{GG OUT} = 14/15V_{DD}$		

## **■ Example of Oscillation Generation Circuit**



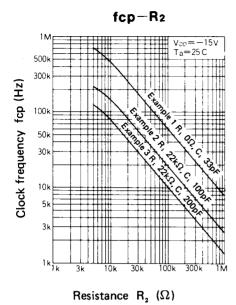
Oscillation circuit of the MN3101 is composed of 2-stage inverter and oscillation frequency is defined by the time constant of C1 and R2 shown left.

Following is an example of C1, R1 and R2. Figure 1 shows  $f_{\mbox{\footnotesize cp}}{}^{*}$  –R2 characteristics.

Example	$R_1$ $(\Omega)$	$R_2$ $(\Omega)$	C <sub>1</sub> (pF)	fosc** (kHz)	f <sub>CP</sub> * (kHz)
Example ①	0	5 k∼1 M	33	15~1500	7.5~750
Example ②	22k	5 k∼ 1 M	100	5.2~440	2.6~220
Example 3	22k	5 k~ 1 M	200	1.4~280	0.7~140

<sup>\*</sup> Clock output frequency of CP1 or CP2 terminals.

<sup>\*\*</sup> Oscillation frequency of OX1, OX2 and OX3.



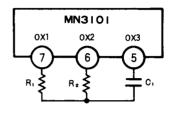


Figure 1 Example of characteristics of clock oscillation frequency.

#### ■ The maximum clock frequency

The upper limit of the value of clock frequency is determined depending on the load capacitance and power consumption.

The permissible dissipation for this LSI is =  $P_D$  = 200mW.

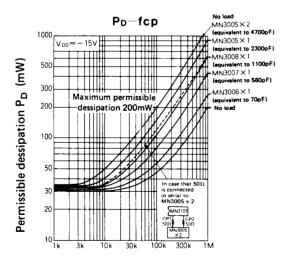
If the clock frequency on the load capacitance is increased, the power consumption will be increased. (Refer to Figure 2.)

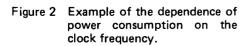
Accordingly, in order to utilize the MN3101 with dissipation less than the permissible value, it is necessary to select adequate values for the clock frequency and load capacitance.

Figure 3 shows an example of the dependence of the maximum clock frequency on the load capacitance in  $P_D = 150 \text{mW}$ .

By connecting a resistance to the clock output terminal, it is made possible to increase the value of the maximum clock frequency without increasing dissipation. (Refer to Figures 2 and 3.)

It is because the dissipation on the LSI side is lessened, as a part of the power consumption required for driving the load capacitance is consumed by the series resistance.





Clock frequency fcp (Hz)

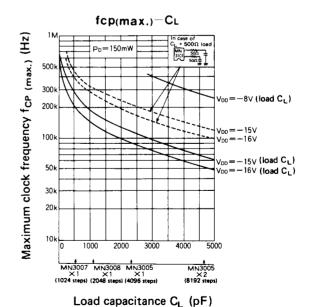


Figure 3 Example of the load capacitance characteristic of the maximum clock frequency in the power consumption of 150mW.