

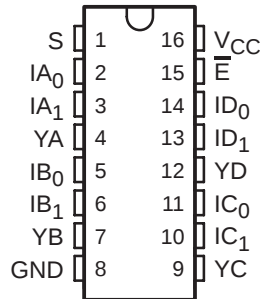
# TS5L100

## QUAD SPDT WIDE-BANDWIDTH LAN SWITCH WITH LOW ON-STATE RESISTANCE

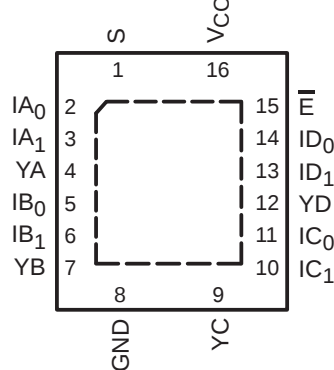
SCDS163A – MAY 2004 – REVISED MAY 2004

- Wide Bandwidth (BW = 300 MHz Min)
- Low Differential Crosstalk ( $X_{TALK} = -60$  dB Typ)
- Low Power Consumption ( $I_{CC} = 3$   $\mu$ A Max)
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance ( $r_{on} = 3$   $\Omega$  Typ)
- $V_{CC}$  Operating Range From 6 V to 6.5 V
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Data and Control Inputs Provide Undershoot Clamp Diode
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Suitable for Both 10 Base-T/100 Base-T Signaling

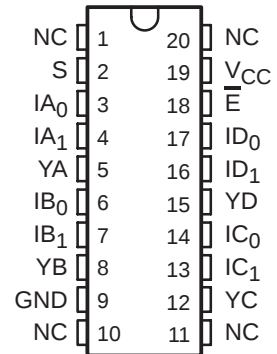
D OR DBQ PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



PW PACKAGE  
(TOP VIEW)



NC – No internal connection

### description/ordering information

The TI TS5L100 LAN switch is a 4-bit 1-of-2 multiplexer/demultiplexer with a single switch-enable ( $\bar{E}$ ) input. When  $\bar{E}$  is low, the switch is enabled and the I port is connected to the Y port. When  $\bar{E}$  is high, the switch is disabled and the high-impedance state exists between the I and Y ports. The select (S) input controls the data path of the multiplexer/demultiplexer.

### ORDERING INFORMATION

| $T_A$       | PACKAGE <sup>†</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|-------------|----------------------|---------------|-----------------------|------------------|
| 0°C to 70°C | QFN – RGY            | Tape and reel | TS5L100RGYR           | TG100            |
|             |                      | Tube          | TS5L100D              | TS5L100          |
|             | SOIC – D             | Tape and reel | TS5L100DR             |                  |
|             |                      | Tape and reel | TS5L100DBQR           | TG100            |
|             | TSSOP – PW           | Tube          | TS5L100PW             | TG100            |
|             |                      | Tape and reel | TS5L100PWR            |                  |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# TS5L100

## QUAD SPDT WIDE-BANDWIDTH LAN SWITCH WITH LOW ON-STATE RESISTANCE

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### description/ordering information (continued)

This device can be used to replace mechanical relays in LAN applications. This device has low  $r_{on}$ , wide bandwidth, and low differential crosstalk, making it suitable for 10 Base-T, 100 Base-T, and various other LAN applications.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\bar{E}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

| INPUTS    |   | INPUT/OUTPUT<br>YX | FUNCTION    |
|-----------|---|--------------------|-------------|
| $\bar{E}$ | S |                    |             |
| L         | L | $IX_0$             | $YX = IX_0$ |
| L         | H | $IX_1$             | $YX = IX_1$ |
| H         | X | Z                  | Disconnect  |

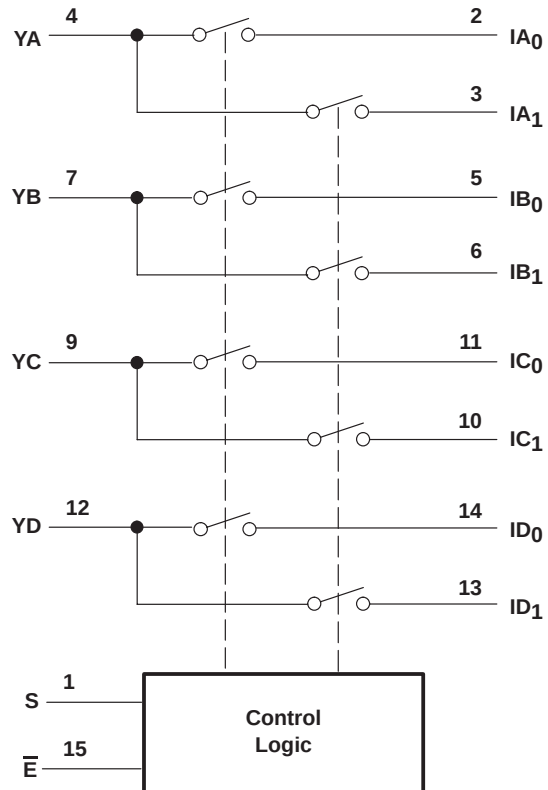
PIN DESCRIPTIONS

| PIN NAME  | DESCRIPTION  |
|-----------|--------------|
| $IAn-IDn$ | Data I/Os    |
| S         | Select input |
| $\bar{E}$ | Enable input |
| $YA-YD$   | Data I/Os    |

**TS5L100**  
**QUAD SPDT WIDE-BANDWIDTH LAN SWITCH**  
**WITH LOW ON-STATE RESISTANCE**

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logic diagram (positive logic)



# TS5L100

## QUAD SPDT WIDE-BANDWIDTH LAN SWITCH WITH LOW ON-STATE RESISTANCE

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                  |                |
|------------------------------------------------------------------|----------------|
| Supply voltage range, $V_{CC}$                                   | –0.5 V to 7 V  |
| Control input voltage range, $V_{IN}$ (see Notes 1 and 2)        | –0.5 V to 7 V  |
| Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)      | –0.5 V to 7 V  |
| Control input clamp current, $I_{IK}$ ( $V_{IN} < 0$ )           | –50 mA         |
| I/O port clamp current, $I_{I/OK}$ ( $V_{I/O} < 0$ )             | –50 mA         |
| ON-state switch current, $I_{I/O}$ (see Note 4)                  | ±128 mA        |
| Continuous current through $V_{CC}$ or GND terminals             | ±100 mA        |
| Package thermal impedance, $\theta_{JA}$ (see Note 5): D package | 73°C/W         |
| (see Note 5): DBQ package                                        | 90°C/W         |
| (see Note 5): PW package                                         | 83°C/W         |
| (see Note 6): RGY package                                        | 39°C/W         |
| Storage temperature range, $T_{stg}$                             | –65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground, unless otherwise specified.
  2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  3.  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
  4.  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
  5. The package thermal impedance is calculated in accordance with JESD 51-7.
  6. The package thermal impedance is calculated in accordance with JESD 51-5.

### recommended operating conditions (see Note 7)

|                                                            | MIN | MAX | UNIT |
|------------------------------------------------------------|-----|-----|------|
| $V_{CC}$ Supply voltage                                    | 6   | 6.5 | V    |
| $V_{IH}$ High-level control input voltage ( $\bar{E}$ , S) | 2.5 | 6.5 | V    |
| $V_{IL}$ Low-level control input voltage ( $\bar{E}$ , S)  | 0   | 0.8 | V    |
| $T_A$ Operating free-air temperature                       | 0   | 70  | °C   |

NOTE 7: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**QUAD SPDT WIDE-BANDWIDTH LAN SWITCH**  
**WITH LOW ON-STATE RESISTANCE**

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**electrical characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 6\text{ V}$  to  $6.5\text{ V}$  (unless otherwise noted)**

| PARAMETER           |                   | TEST CONDITIONS          |                                                      | MIN                                     | TYP <sup>†</sup> | MAX     | UNIT          |
|---------------------|-------------------|--------------------------|------------------------------------------------------|-----------------------------------------|------------------|---------|---------------|
| $V_{IK}$            | $\overline{E}, S$ | $V_{CC} = 6\text{ V},$   | $I_{IN} = -18\text{ mA}$                             |                                         |                  | -1.8    | V             |
| $V_{hys}$           | $\overline{E}, S$ |                          |                                                      |                                         | 150              |         | mV            |
| $V_O$               |                   | $V_I = 4.5\text{ V},$    | $\overline{E} = \text{low},$                         | $R_L = 100\ \Omega,$                    | 3.7              | 4.06    | V             |
| $I_{IH}$            | $\overline{E}, S$ | $V_{CC} = 6.5\text{ V},$ | $V_{IN} = V_{CC}$                                    |                                         |                  | $\pm 1$ | $\mu\text{A}$ |
| $I_{IL}$            | $\overline{E}, S$ | $V_{CC} = 6.5\text{ V},$ | $V_{IN} = \text{GND}$                                |                                         |                  | $\pm 1$ | $\mu\text{A}$ |
| $I_{OZ}^{\ddagger}$ |                   | $V_{CC} = 6.5\text{ V},$ | $V_O = 0\text{ to }6.5\text{ V},$<br>$V_I = 0,$      | Switch OFF                              |                  | $\pm 1$ | $\mu\text{A}$ |
| $I_{OS}^{\S}$       |                   | $V_{CC} = 6.5\text{ V},$ | $V_O = 0\text{ to }0.5\text{ V}_{CC},$<br>$V_I = 0,$ | Switch ON                               | 50               |         | mA            |
| $I_{off}$           |                   | $V_{CC} = 0,$            | $V_O = 0\text{ to }6.5\text{ V},$                    | $V_I = 0$                               |                  | 1       | $\mu\text{A}$ |
| $I_{CC}$            |                   | $V_{CC} = 6.5\text{ V},$ | $I_{IO} = 0,$                                        | Switch ON or OFF                        |                  | 3       | $\mu\text{A}$ |
| $\Delta I_{CC}$     | $\overline{E}, S$ | $V_{CC} = 6.5\text{ V},$ | One input at $3.4\text{ V},$                         | Other inputs at $V_{CC}$ or GND         |                  | 6       | mA            |
| $I_{CCD}$           |                   | $V_{CC} = 6.5\text{ V},$ | I and Y ports open,                                  | $V_{IN}$ input switching 50% duty cycle |                  | 0.35    | mA/<br>MHz    |
| $C_{IN}$            | $\overline{E}, S$ | $f = 1\text{ MHz}$       |                                                      |                                         | 3.5              |         | pF            |
| $C_{OFF}$           | I port            | $V_I = 0,$               | $f = 1\text{ MHz},$<br>Outputs open,                 | Switch OFF                              | 4.5              |         | pF            |
|                     | Y port            |                          |                                                      |                                         | 6.5              |         |               |
| $C_{ON}$            |                   | $V_I = 0,$               | $f = 1\text{ MHz},$<br>Outputs open,                 | Switch ON                               | 14               |         | pF            |
| $r_{on}$            | M1                | $V_I = 4.5\text{ V},$    | Switch ON,                                           | $R_L = 100\ \Omega,$ see Figure 11      | 7.5              | 11.2    | $\Omega$      |
|                     | M2                |                          |                                                      |                                         | 2                | 3       |               |
| $\Delta r_{on}$     |                   | $V_I = 4.5\text{ V},$    | Switch ON                                            |                                         | 1                | 2       | $\Omega$      |

$V_I, V_O, I_I,$  and  $I_O$  refer to I/O pins.  $V_{IN}$  refers to the control inputs.

<sup>†</sup> All typical values are at  $V_{CC} = 6.2\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> For I/O ports,  $I_{OZ}$  includes the input leakage current.

<sup>§</sup> The  $I_{OS}$  test is applicable to only one ON channel at a time. The duration of this test is less than one second.

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 6\text{ V}$  to  $6.5\text{ V}, R_L = 100\ \Omega, C_L = 35\text{ pF}$  (unless otherwise noted) (see Figure 7)**

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | MIN | MAX | UNIT |
|-----------|-----------------|----------------|-----|-----|------|
| $t_{ON}$  | S               | Y              |     | 7   | ns   |
| $t_{OFF}$ | S               | Y              |     | 4   | ns   |

<sup>†</sup> All typical values are at  $V_{CC} = 6.2\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

**dynamic characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 6\text{ V}$  to  $6.5\text{ V}$  (unless otherwise noted)**

| PARAMETER               | TEST CONDITIONS      |                                                               | MIN | TYP <sup>†</sup> | MAX | UNIT |
|-------------------------|----------------------|---------------------------------------------------------------|-----|------------------|-----|------|
| $X_{TALK}(\text{Diff})$ | $R_L = 100\ \Omega,$ | $f = 10\text{ MHz},$ see Figure 12, $t_r = t_f = 2\text{ ns}$ | -40 | -60              |     | dB   |
| $X_{TALK}$              | $R_L = 100\ \Omega,$ | $f = 30\text{ MHz},$ see Figure 9                             |     | -50              |     | dB   |
| $O_{IRR}$               | $R_L = 100\ \Omega,$ | $f = 30\text{ MHz},$ see Figure 10                            |     | -40              |     | dB   |
| BW                      | $R_L = 100\ \Omega,$ | see Figure 8                                                  |     | 350              |     | MHz  |

<sup>†</sup> All typical values are at  $V_{CC} = 6.2\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .



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### WITH LOW ON-STATE RESISTANCE

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#### OPERATING CHARACTERISTICS

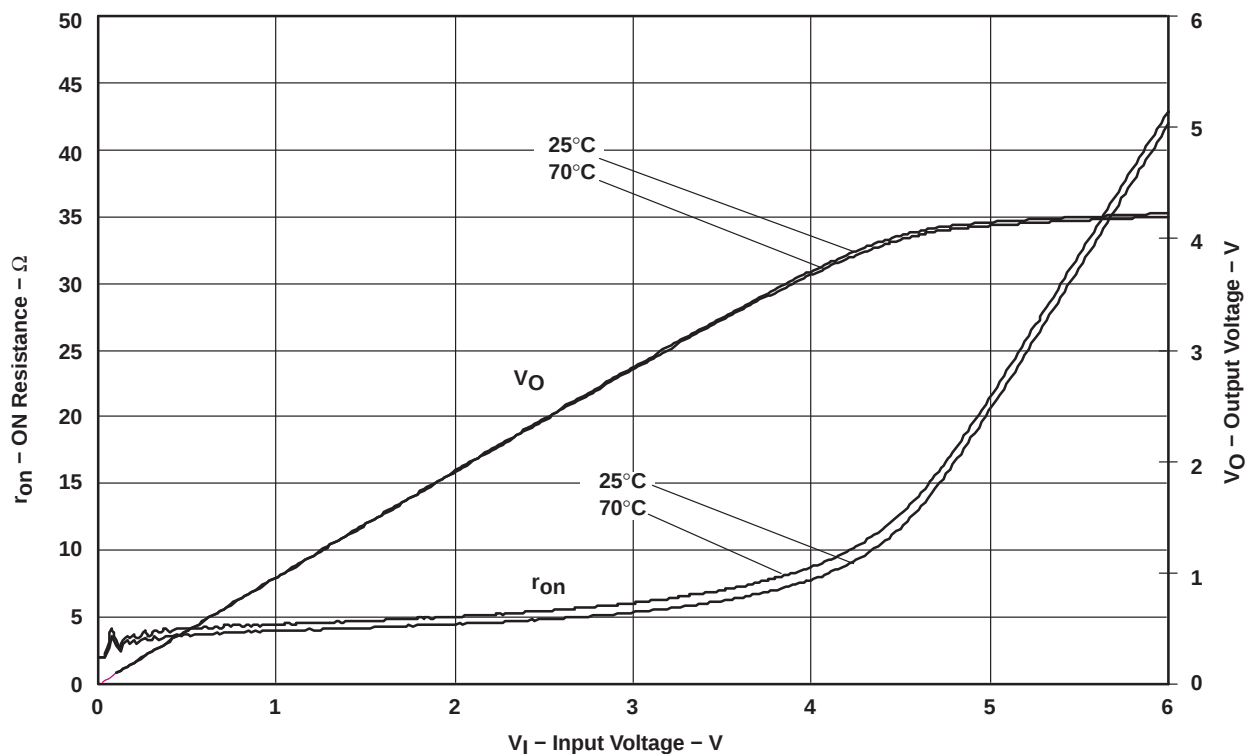


Figure 1.  $r_{on}$  and  $V_O$  vs  $V_I$  Over Temperature ( $V_{CC} = 6$  V)

OPERATING CHARACTERISTICS

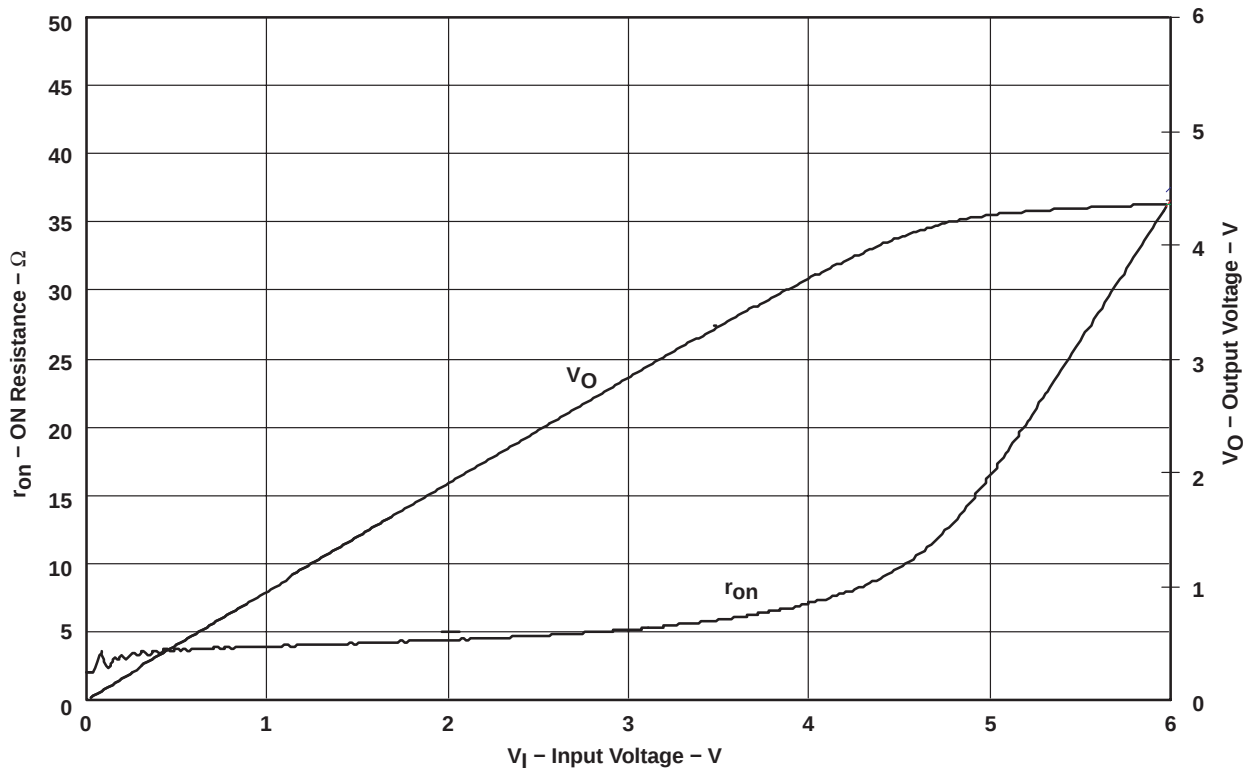


Figure 2.  $r_{on}$  and  $V_O$  vs  $V_I$  ( $V_{CC} = 6.2$  V and  $T_A = 25^\circ\text{C}$ )

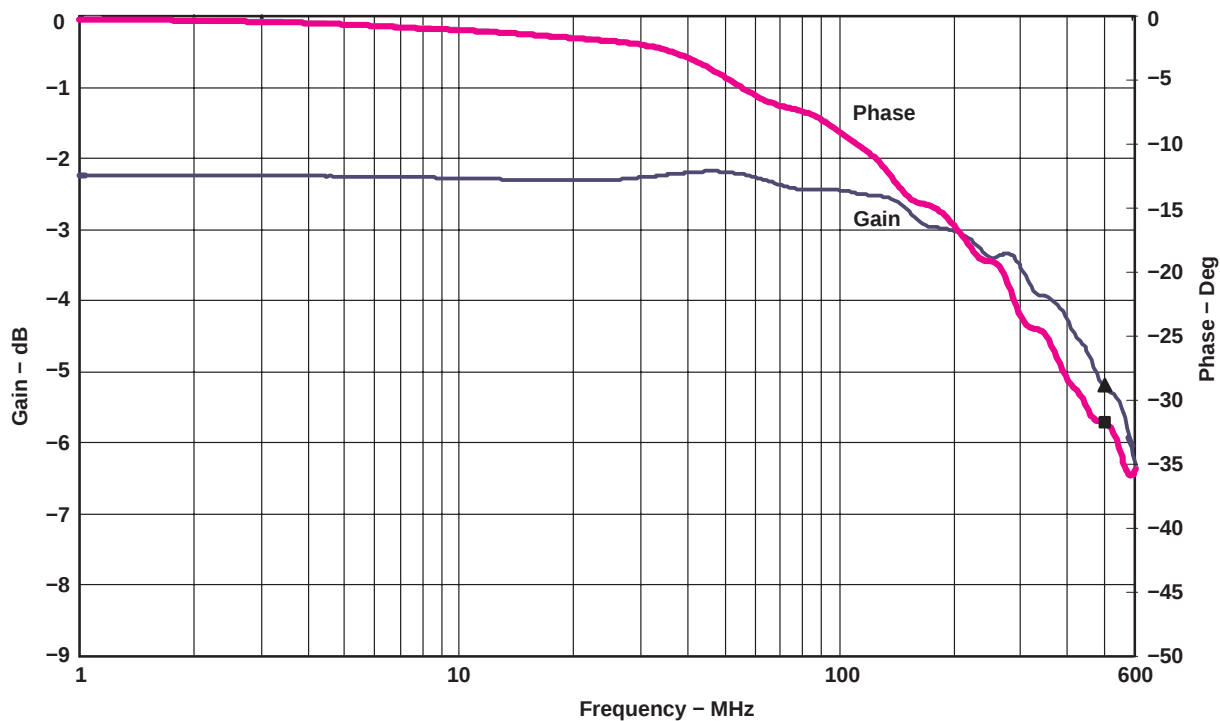
# TS5L100

## QUAD SPDT WIDE-BANDWIDTH LAN SWITCH

### WITH LOW ON-STATE RESISTANCE

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#### OPERATING CHARACTERISTICS



- ▲ Gain -3 dB at 501.2 MHz
- Phase at -3-dB Frequency, -31.7 Degrees

Figure 3. Gain/Phase vs Frequency

# TS5L100 QUAD SPDT WIDE-BANDWIDTH LAN SWITCH WITH LOW ON-STATE RESISTANCE

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## OPERATING CHARACTERISTICS

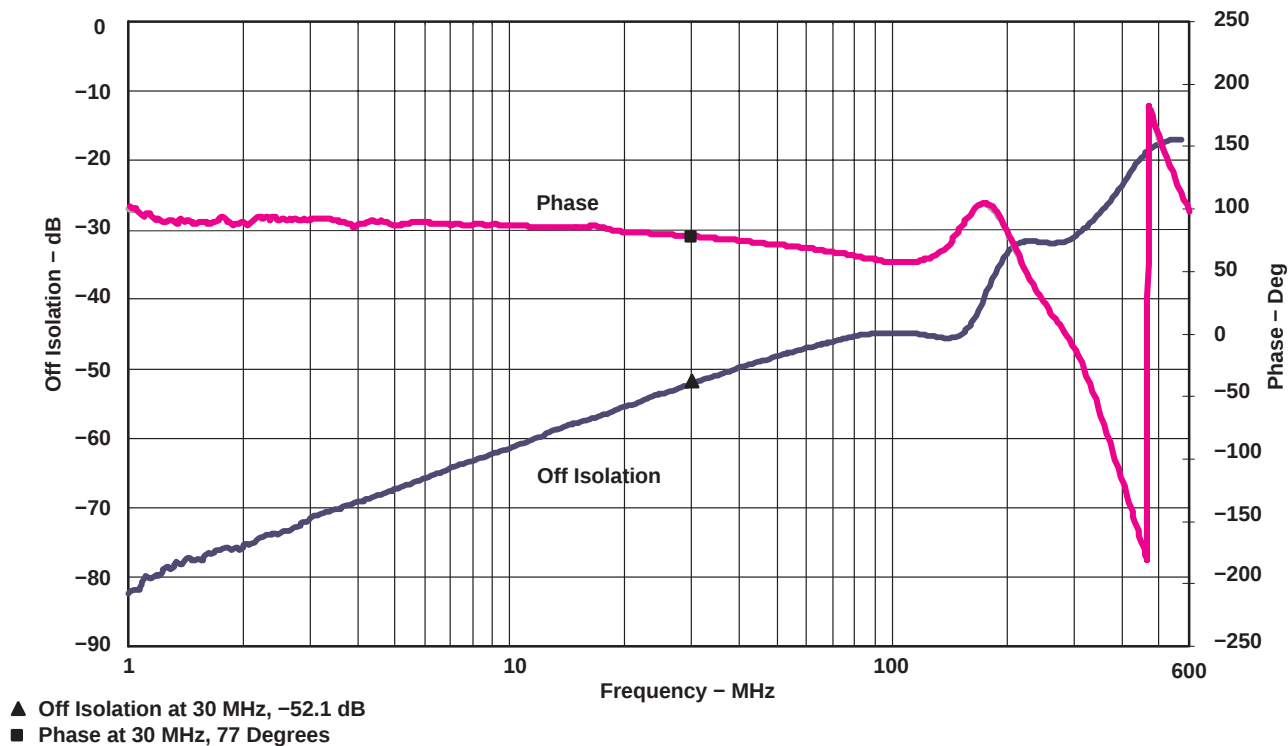


Figure 4. Off Isolation vs Frequency

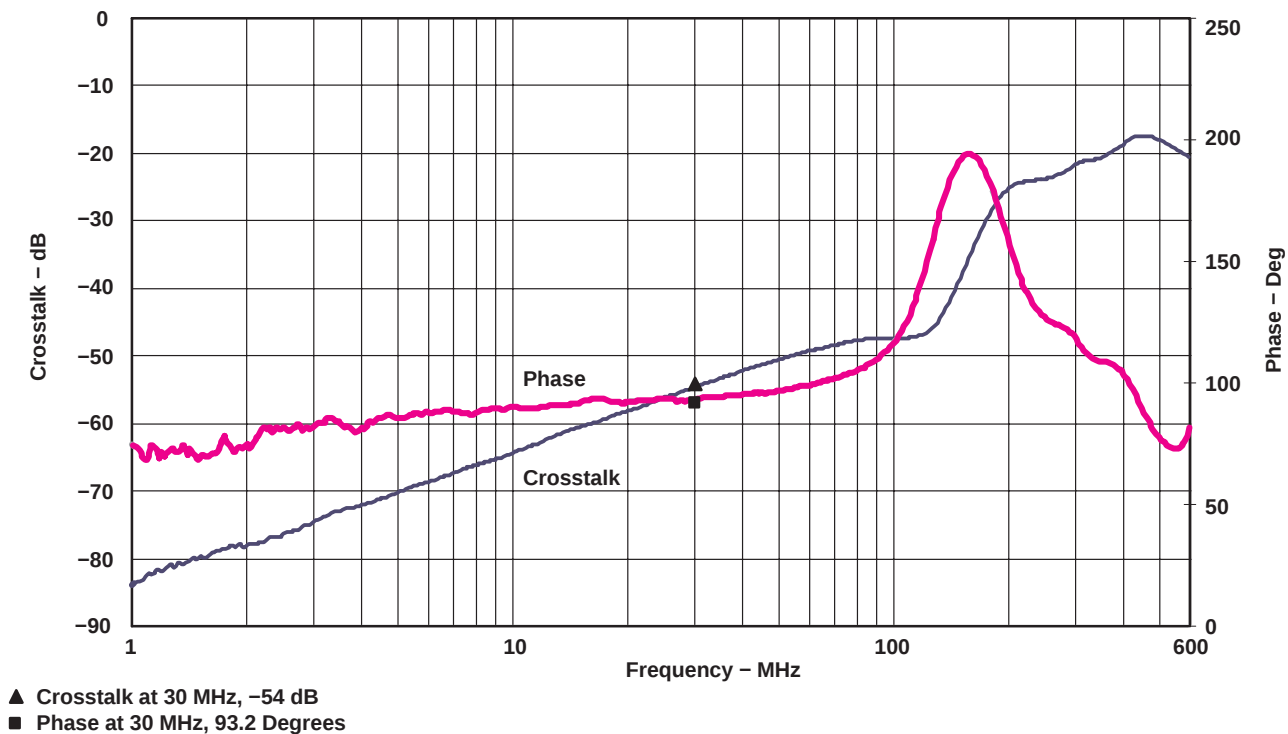


Figure 5. Crosstalk vs Frequency



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#### OPERATING CHARACTERISTICS

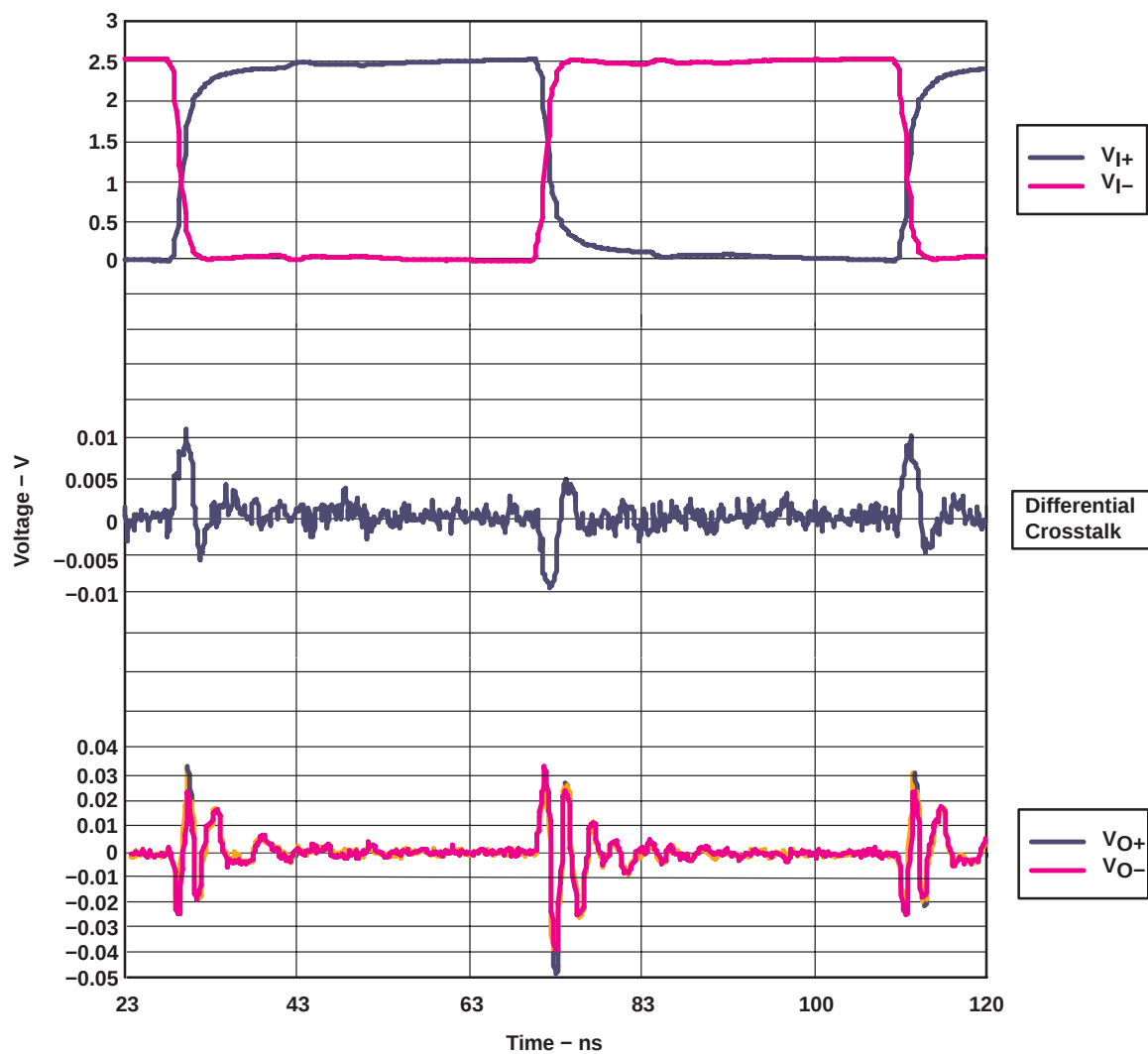


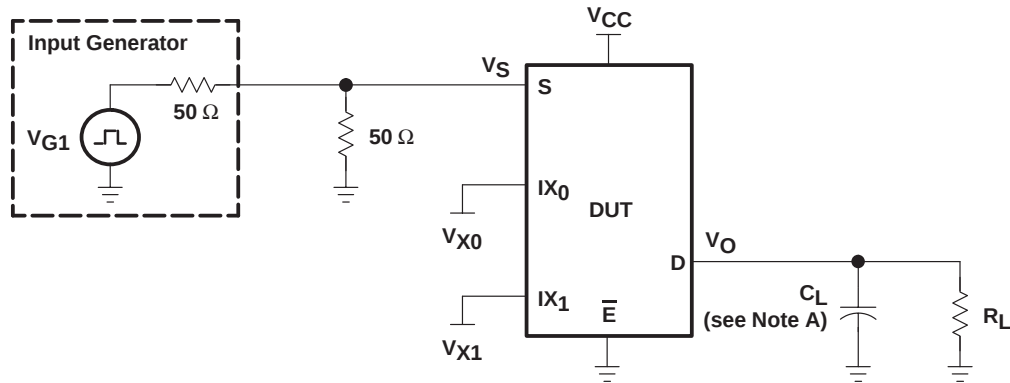
Figure 6. Differential Crosstalk

# TS5L100

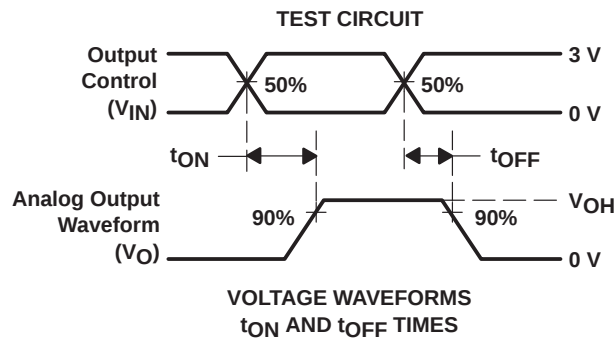
## QUAD SPDT WIDE-BANDWIDTH LAN SWITCH WITH LOW ON-STATE RESISTANCE

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### PARAMETER MEASUREMENT INFORMATION



| TEST             | V <sub>CC</sub> | R <sub>L</sub> | C <sub>L</sub> | V <sub>X0</sub> | V <sub>X1</sub> |
|------------------|-----------------|----------------|----------------|-----------------|-----------------|
| t <sub>ON</sub>  | 6.2 V           | 100 Ω          | 35 pF          | GND             | 4.5 V           |
|                  | 6.2 V           | 100 Ω          | 35 pF          | 4.5 V           | GND             |
| t <sub>OFF</sub> | 6.2 V           | 100 Ω          | 35 pF          | GND             | 4.5 V           |
|                  | 6.2 V           | 100 Ω          | 35 pF          | 4.5 V           | GND             |



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.  
 C. The outputs are measured one at a time, with one transition per measurement.

**Figure 7. Test Circuit and Voltage Waveforms**

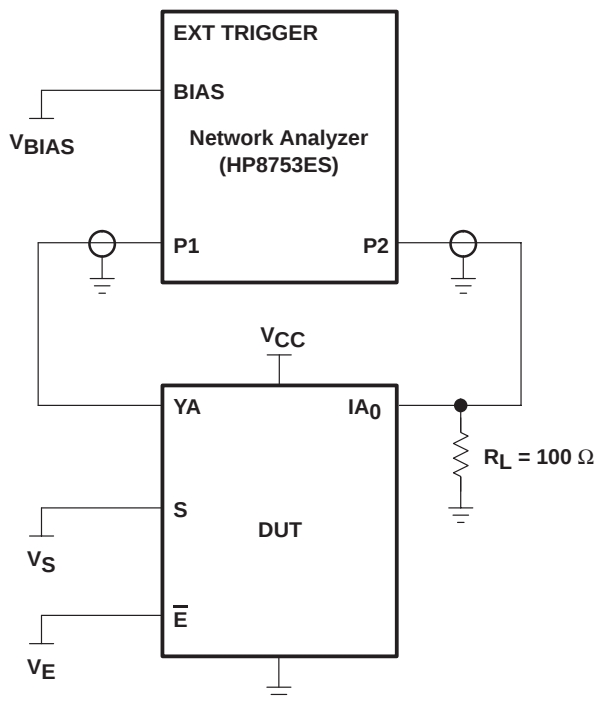
# TS5L100

## QUAD SPDT WIDE-BANDWIDTH LAN SWITCH

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#### PARAMETER MEASUREMENT INFORMATION



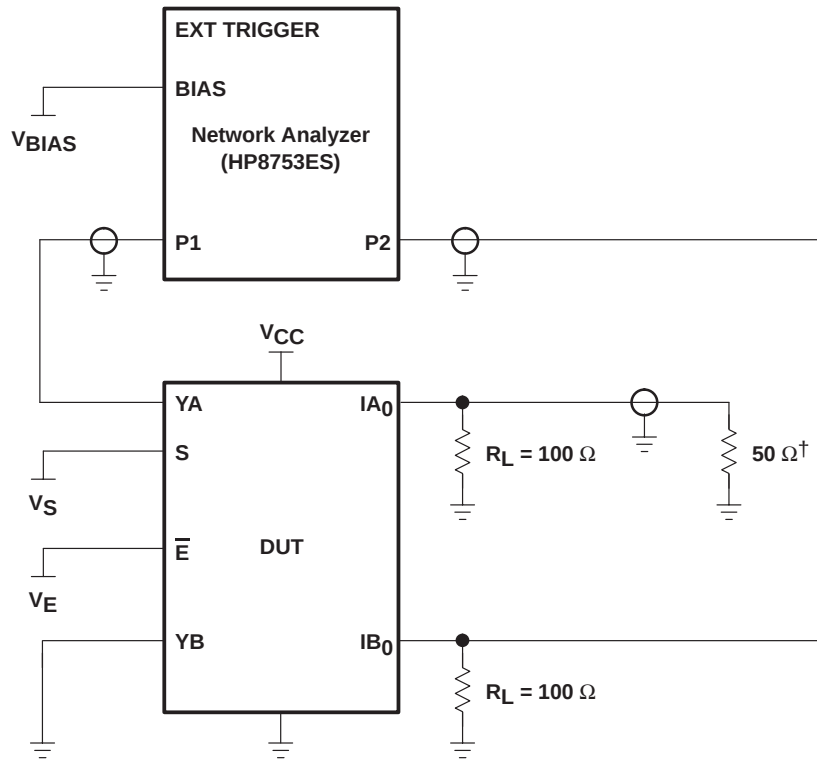
**Figure 8. Test Circuit for Frequency Response (BW)**

Frequency response is measured at the output of the ON channel. For example, when  $V_S = 0$ ,  $V_E = 0$ , and YA is the input, the output is measured at IA<sub>0</sub>. All unused analog I/O ports are left open.

#### HP8753ES setup

Average = 4  
RBW = 3 kHz  
 $V_{BIAS} = 0.35$  V  
ST = 2 s  
P1 = 0 dBm

## PARAMETER MEASUREMENT INFORMATION



† A 50-Ω termination resistor is needed for the network analyzer.

**Figure 9. Test Circuit for Crosstalk ( $X_{TALK}$ )**

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when  $V_S = 0$ ,  $V_E = 0$ , and YA is the input, the output is measured at  $IB_0$ . All unused analog input (Y) ports are connected to GND, and output (A) ports are connected to GND through 50-Ω pulldown resistors.

### HP8753ES setup

Average = 4  
 RBW = 3 kHz  
 $V_{BIAS} = 0.35$  V  
 ST = 2 s  
 P1 = 0 dBm

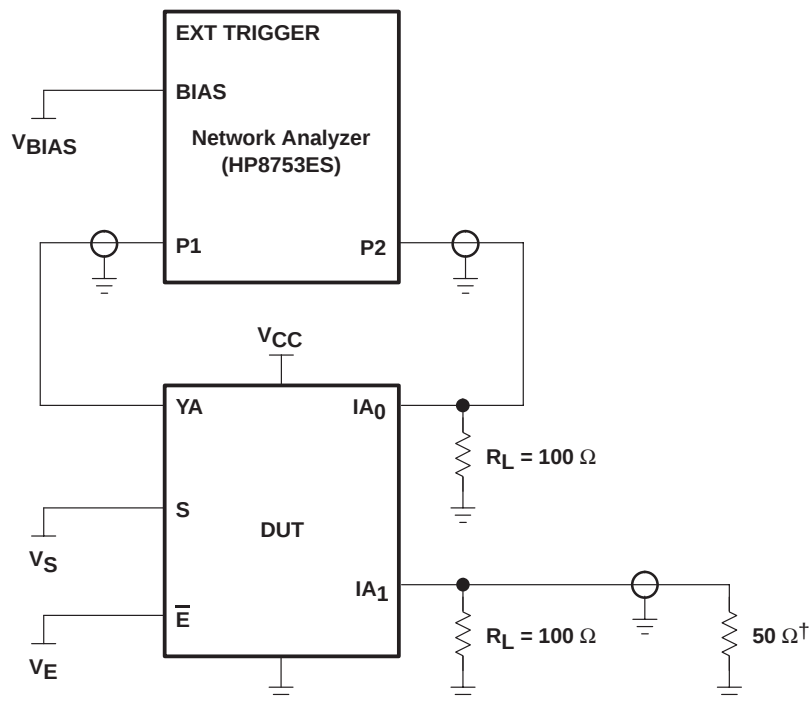
# TS5L100

## QUAD SPDT WIDE-BANDWIDTH LAN SWITCH

### WITH LOW ON-STATE RESISTANCE

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#### PARAMETER MEASUREMENT INFORMATION



† A 50- $\Omega$  termination resistor is needed for the network analyzer.

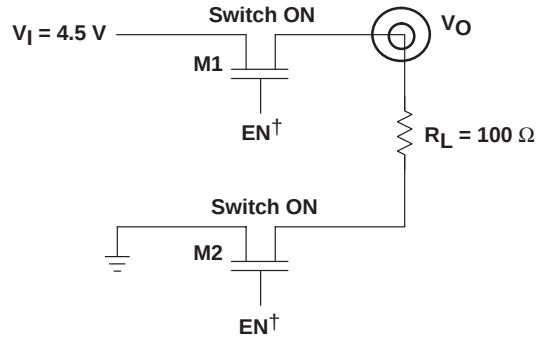
**Figure 10. Test Circuit for Off Isolation ( $O_{IRR}$ )**

Off isolation is measured at the output of the OFF channel. For example, when  $V_S = V_{CC}$ ,  $V_E = 0$ , and YA is the input, the output is measured at IA<sub>0</sub>. All unused analog input (Y) ports are left open, and output (A) ports are connected to GND through 50- $\Omega$  pulldown resistors.

#### HP8753ES setup

Average = 4  
 RBW = 3 kHz  
 $V_{BIAS} = 0.35$  V  
 ST = 2 s  
 P1 = 0 dBm

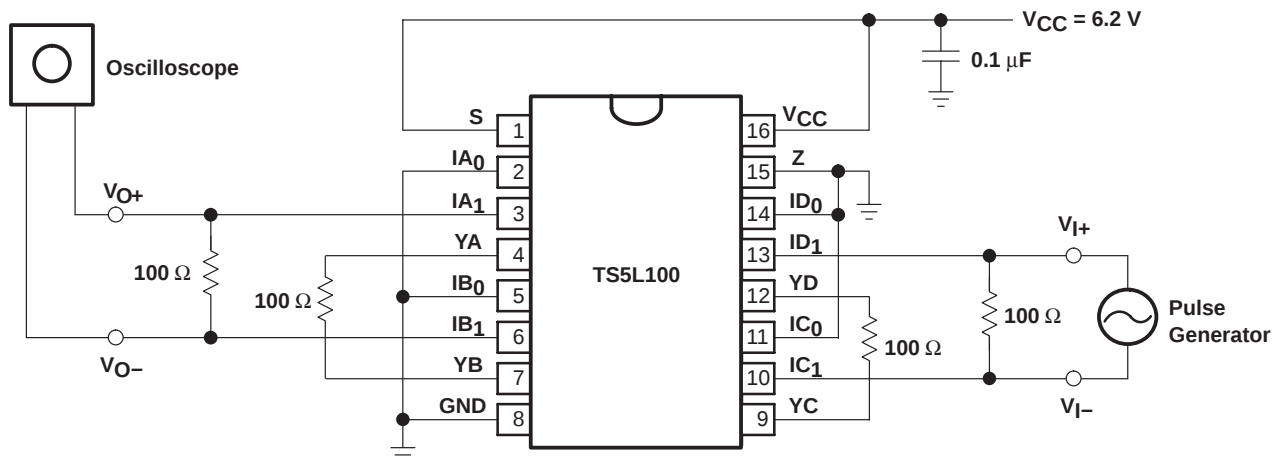
## PARAMETER MEASUREMENT INFORMATION



† EN is the internal enable signal applied to the switch.

NOTE A:  $r_{on}$  (M1) and  $r_{on}$  (M2) are calculated from the voltage drop and current across the two terminals of M1 and M2, respectively.

**Figure 11. Test Circuit for  $V_O$  and  $r_{on}$**



**Figure 12. Differential Crosstalk Measurement**

Differential crosstalk is a measure of coupling noise between a transmit and receive pair in the LAN application. Differential crosstalk depends on the edge rate, frequency, and load. This is calculated from the equation,  $X_{TALK}(Diff)_{db} = 20 \log V_O(Diff)/V_I(Diff)$ , where  $V_O(Diff)$  is the differential output voltage and  $V_I(Diff)$  is the differential input voltage.

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| TS5L100D         | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TS5L100DBQR      | ACTIVE                | SSOP         | DBQ             | 16   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-2-260C-1 YEAR          |                             |
| TS5L100DBQRE4    | ACTIVE                | SSOP         | DBQ             | 16   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-2-260C-1 YEAR          |                             |
| TS5L100DBQRG4    | ACTIVE                | SSOP         | DBQ             | 16   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-2-260C-1 YEAR          |                             |
| TS5L100DE4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TS5L100DG4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TS5L100DR        | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TS5L100DRE4      | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TS5L100DRG4      | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TS5L100PW        | ACTIVE                | TSSOP        | PW              | 20   | 70          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TS5L100PWE4      | ACTIVE                | TSSOP        | PW              | 20   | 70          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TS5L100PWG4      | ACTIVE                | TSSOP        | PW              | 20   | 70          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TS5L100PWR       | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TS5L100PWRE4     | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TS5L100PWRG4     | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

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**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

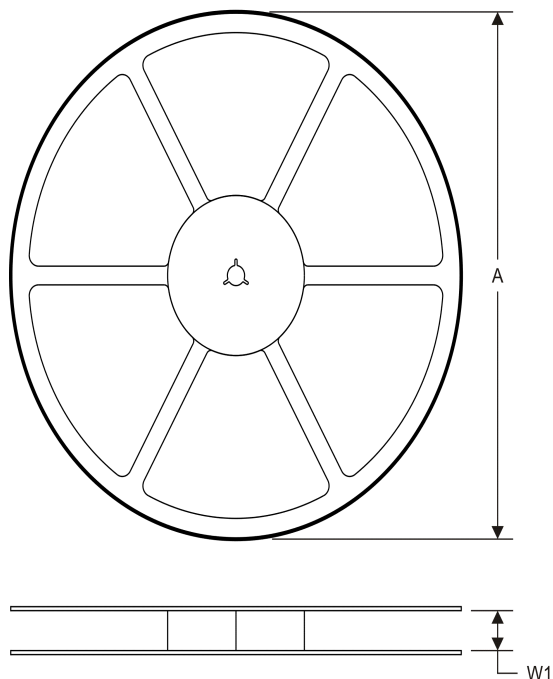
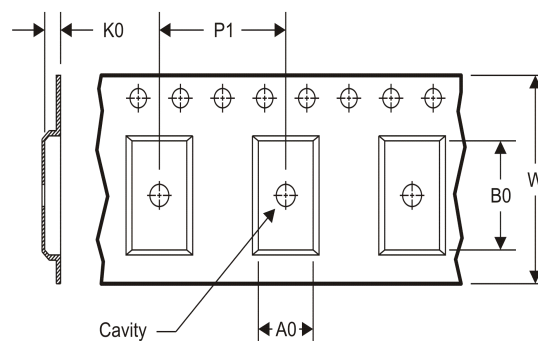
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


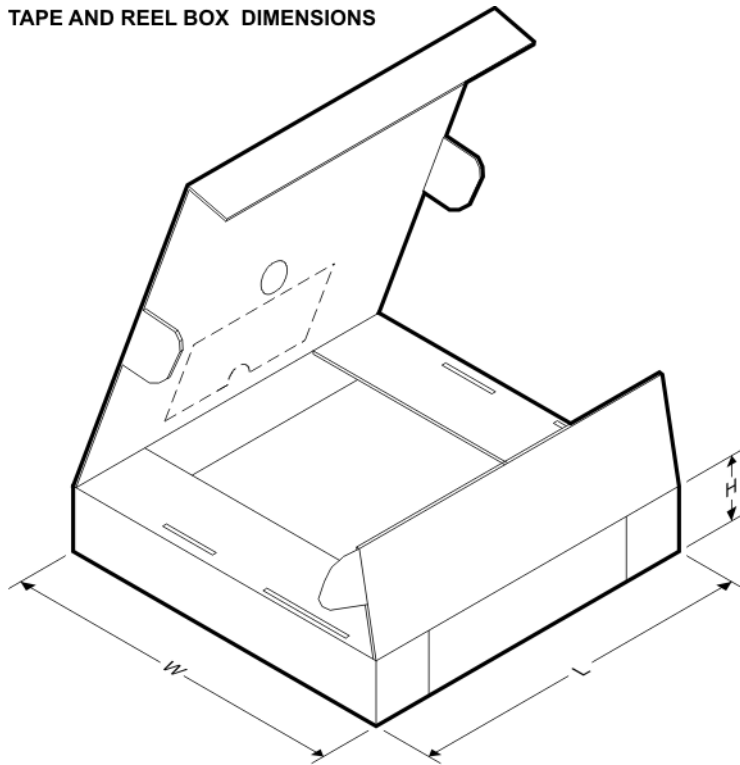
|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TS5L100DR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| TS5L100PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

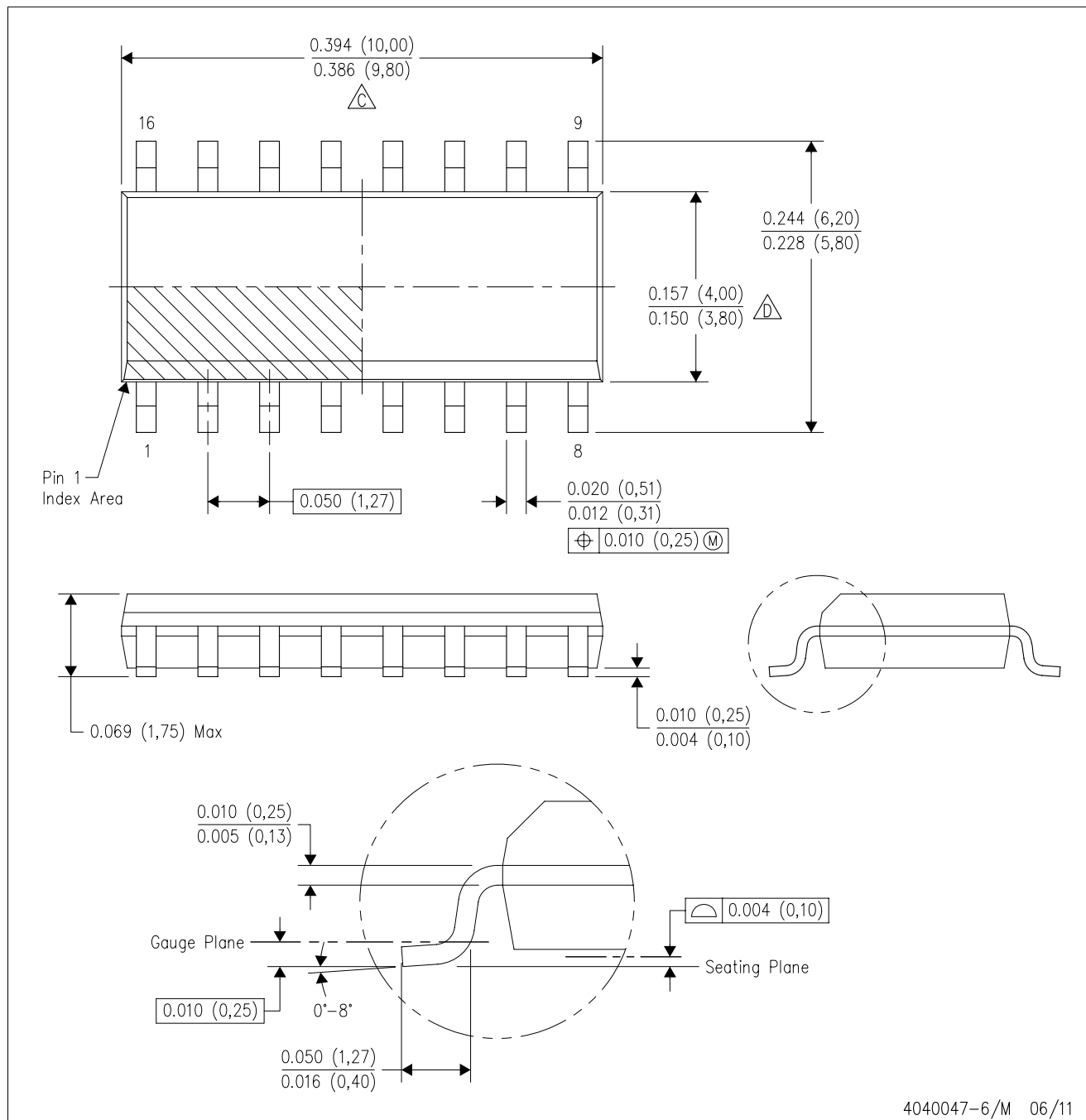


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TS5L100DR  | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| TS5L100PWR | TSSOP        | PW              | 20   | 2000 | 367.0       | 367.0      | 38.0        |

D (R-PDSO-G16)

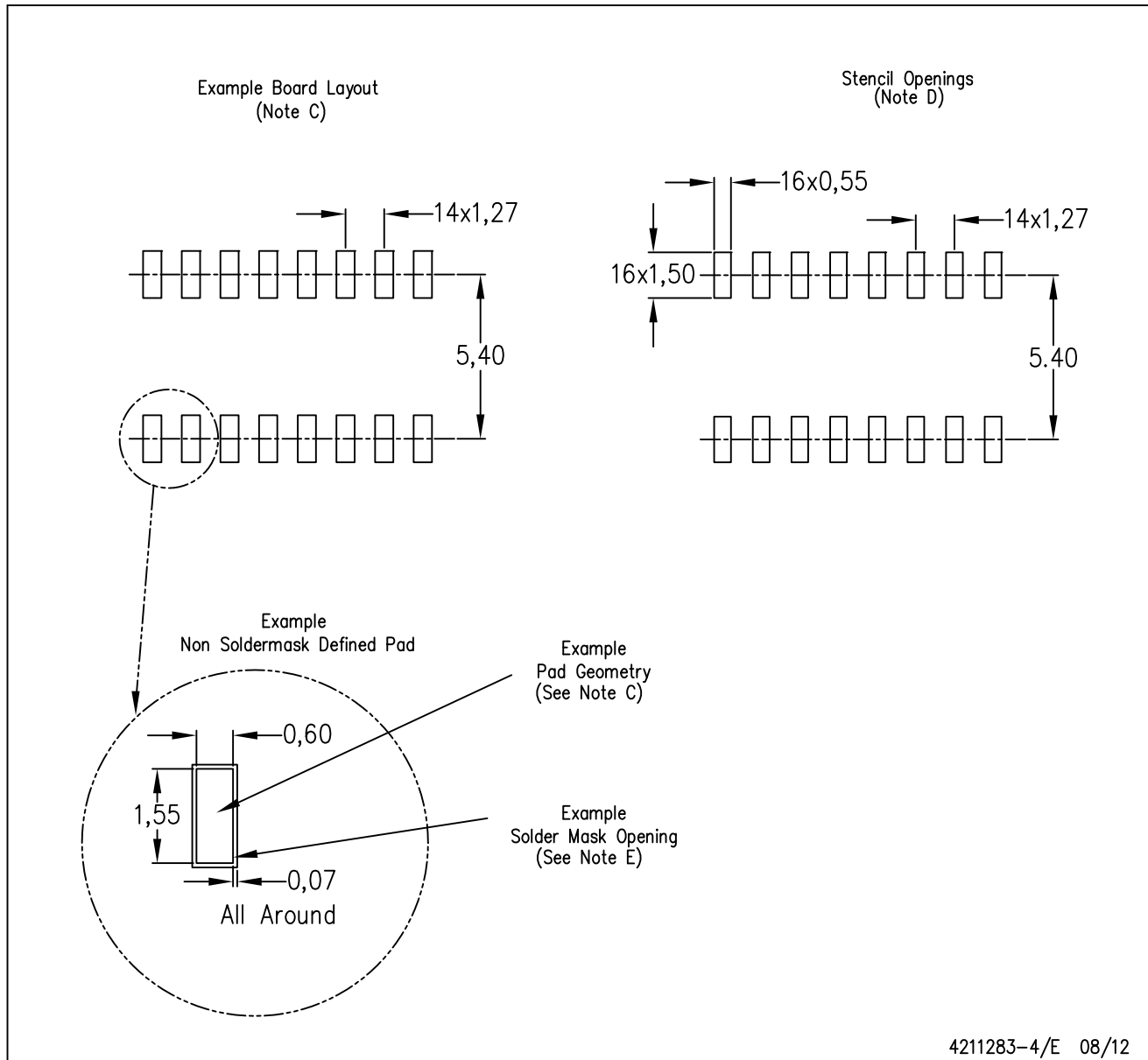
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

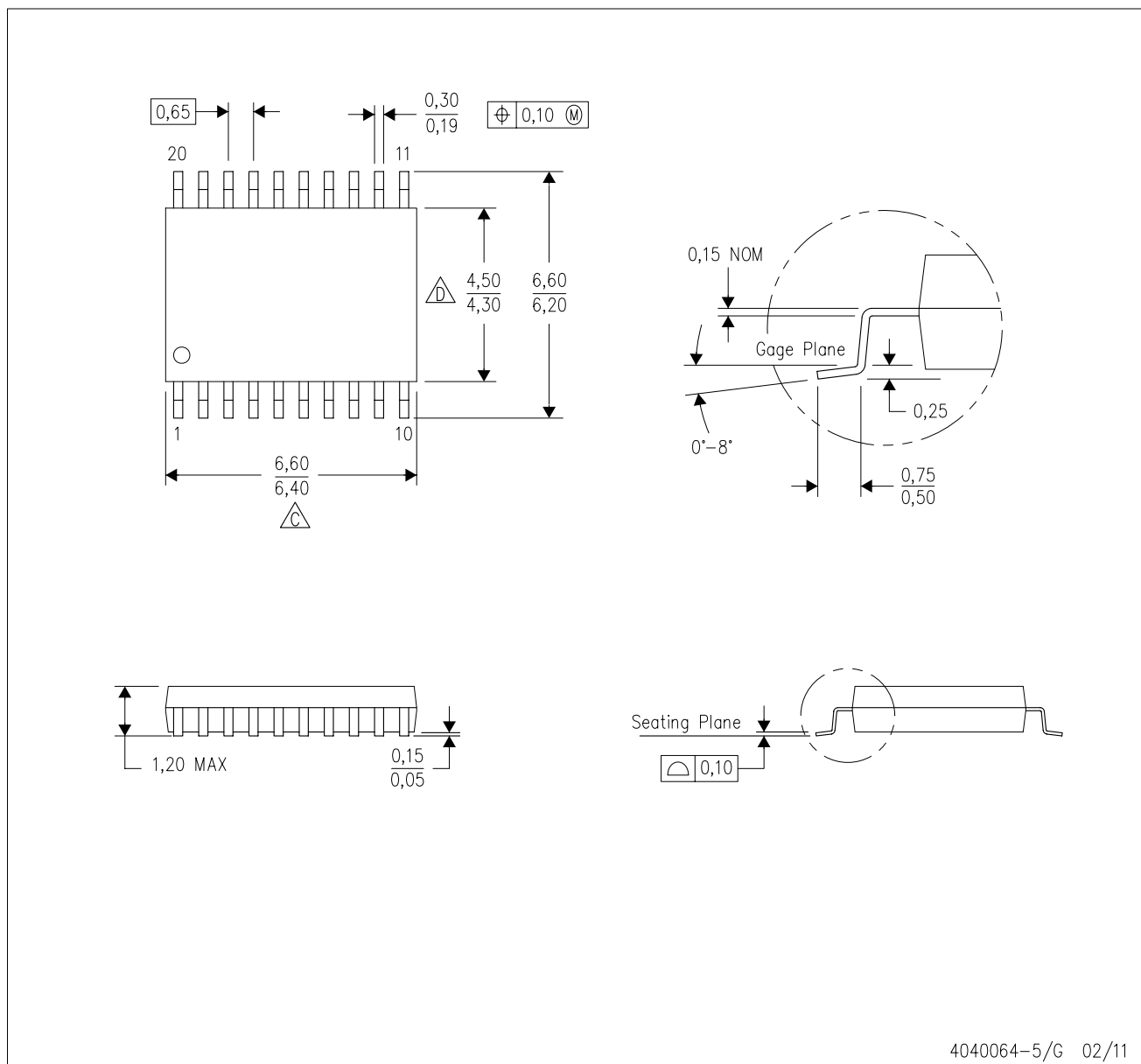
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

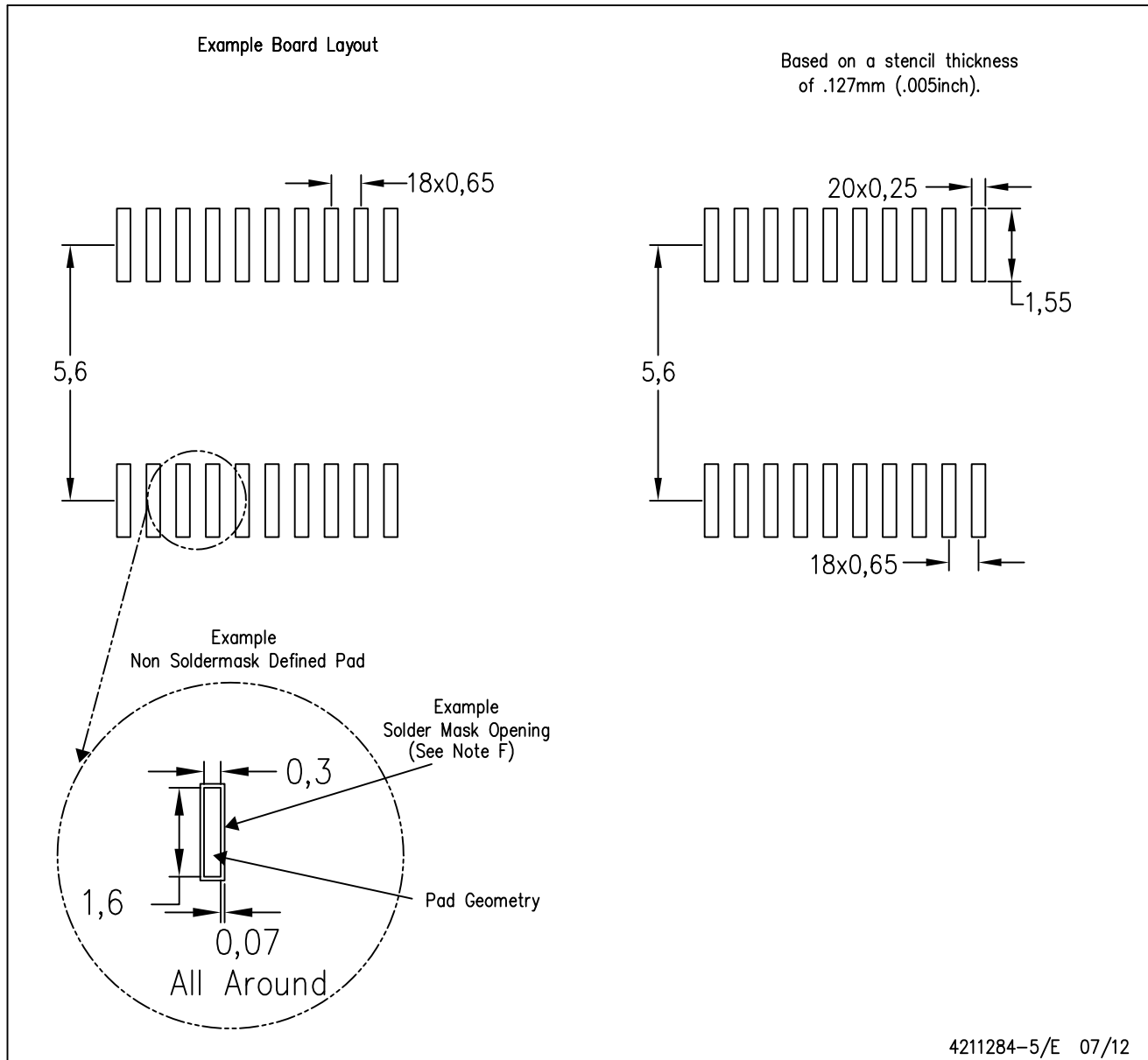


4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

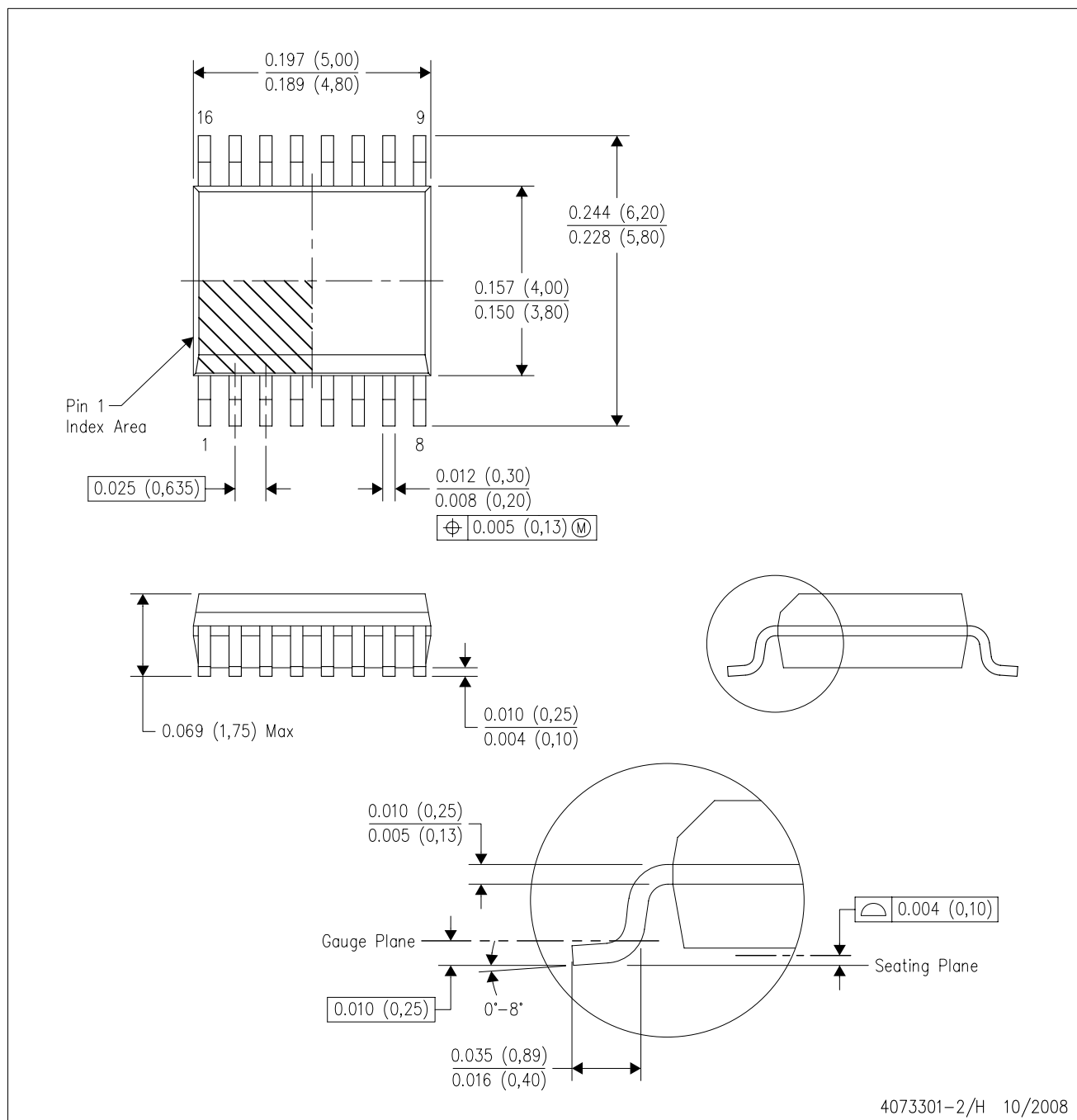
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R-PDSO-G16)

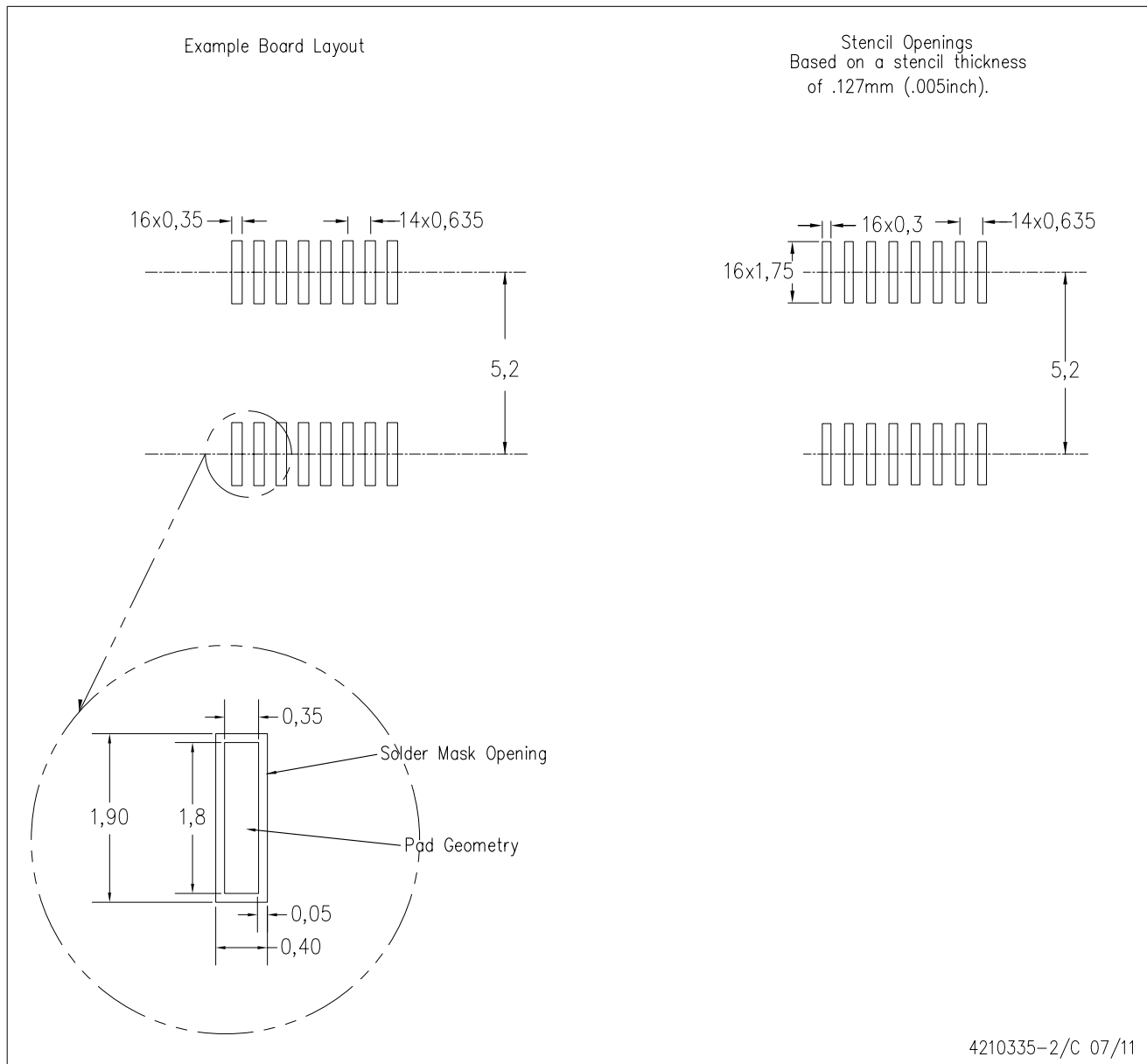
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AB.

DBQ (R-PDSO-G16)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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