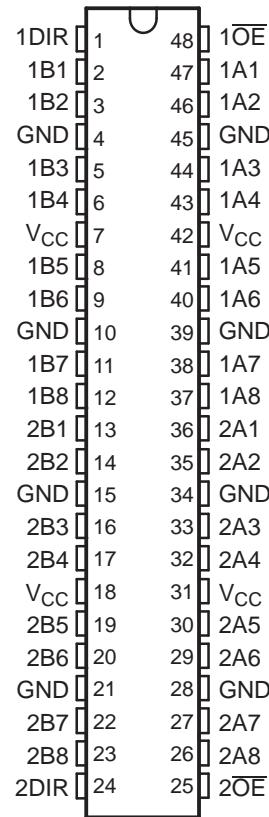


## FEATURES

- Member of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

SN54LVT16245B . . . WD PACKAGE  
SN74LVT16245B . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

### ORDERING INFORMATION

| $T_A$                                      | PACKAGE <sup>(1)</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|--|------------------------|--------------|-----------------------|------------------|
| $-40^\circ\text{C}$ to $85^\circ\text{C}$  | FBGA – GRD             | Reel of 1000 | SN74LVT16245BGRDR     | VD245B           |
|  | FBGA – ZRD (Pb-free)   |              | SN74LVT16245BZRDR     |                  |
|  | SSOP – DL              | Tube of 25   | SN74LVT16245BDL       | LVT16245B        |
|  |                        |              | SN74LVT16245BDLG4     |                  |
|  |                        | Reel of 1000 | SN74LVT16245BDLDR     |                  |
|  |                        |              | 74LVT16245BDLRG4      |                  |
|  | TSSOP – DGG            | Reel of 2000 | SN74LVT16245BDGGR     | LVT16245B        |
|  |                        |              | 74LVT16245BDGGRE4     |                  |
|  | TVSOP – DGV            | Reel of 2000 | SN74LVT16245BDGVR     | VD245B           |
|  |                        |              | 74LVT16245BDGVRE4     |                  |
| $-55^\circ\text{C}$ to $125^\circ\text{C}$ | VFBGA – GQL            | Reel of 1000 | SN74LVT16245BGQLR     | VD245B           |
|  | VFBGA – ZQL (Pb-free)  |              | SN74LVT16245BZQLR     |                  |
|  | CFP – WD               | Tube         | SNJ54LVT16245BWD      | SNJ54LVT16245BWD |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

**SN54LVT16245B, SN74LVT16245B  
3.3-V ABT 16-BIT BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

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**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

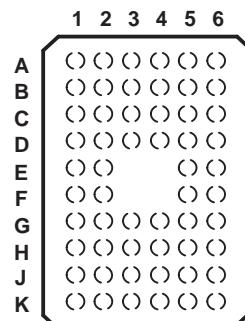
The 'LVT16245B devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ( $\overline{OE}$ ) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess  $I_{CC}$  and  $I_{CCZ}$ .

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

**GQL OR ZQL PACKAGE  
(TOP VIEW)**

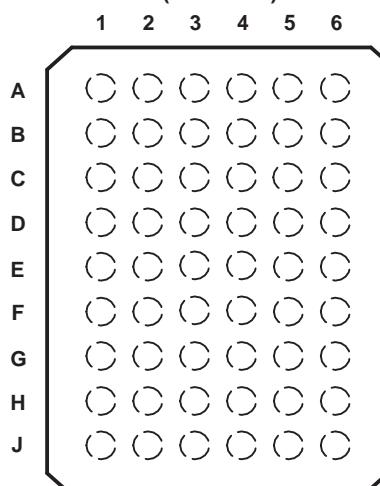


**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(56-Ball GQL/ZQL Package)**

|          | 1    | 2   | 3        | 4        | 5   | 6               |
|----------|------|-----|----------|----------|-----|-----------------|
| <b>A</b> | 1DIR | NC  | NC       | NC       | NC  | $\overline{OE}$ |
| <b>B</b> | 1B2  | 1B1 | GND      | GND      | 1A1 | 1A2             |
| <b>C</b> | 1B4  | 1B3 | $V_{CC}$ | $V_{CC}$ | 1A3 | 1A4             |
| <b>D</b> | 1B6  | 1B5 | GND      | GND      | 1A5 | 1A6             |
| <b>E</b> | 1B8  | 1B7 |          |          | 1A7 | 1A8             |
| <b>F</b> | 2B1  | 2B2 |          |          | 2A2 | 2A1             |
| <b>G</b> | 2B3  | 2B4 | GND      | GND      | 2A4 | 2A3             |
| <b>H</b> | 2B5  | 2B6 | $V_{CC}$ | $V_{CC}$ | 2A6 | 2A5             |
| <b>J</b> | 2B7  | 2B8 | GND      | GND      | 2A8 | 2A7             |
| <b>K</b> | 2DIR | NC  | NC       | NC       | NC  | $\overline{OE}$ |

(1) NC – No internal connection

**GRD OR ZRD PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(54-Ball GRD/ZRD Package)**

|          | 1   | 2   | 3        | 4               | 5   | 6   |
|----------|-----|-----|----------|-----------------|-----|-----|
| <b>A</b> | 1B1 | NC  | 1DIR     | $\overline{OE}$ | NC  | 1A1 |
| <b>B</b> | 1B3 | 1B2 | NC       | NC              | 1A2 | 1A3 |
| <b>C</b> | 1B5 | 1B4 | $V_{CC}$ | $V_{CC}$        | 1A4 | 1A5 |
| <b>D</b> | 1B7 | 1B6 | GND      | GND             | 1A6 | 1A7 |
| <b>E</b> | 2B1 | 1B8 | GND      | GND             | 1A8 | 2A1 |
| <b>F</b> | 2B3 | 2B2 | GND      | GND             | 2A2 | 2A3 |
| <b>G</b> | 2B5 | 2B4 | $V_{CC}$ | $V_{CC}$        | 2A4 | 2A5 |
| <b>H</b> | 2B7 | 2B6 | NC       | NC              | 2A6 | 2A7 |
| <b>J</b> | 2B8 | NC  | 2DIR     | $\overline{OE}$ | NC  | 2A8 |

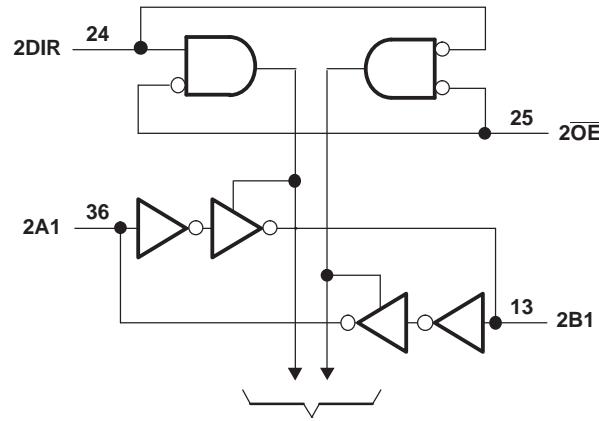
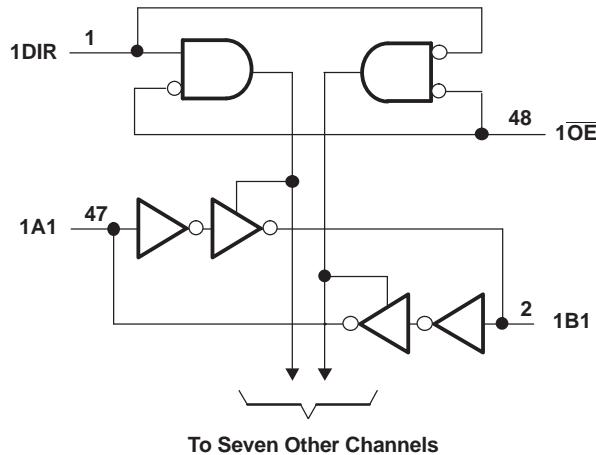
(1) NC – No internal connection

**FUNCTION TABLE<sup>(1)</sup>  
(each 8-bit section)**

| CONTROL INPUTS  |     | OUTPUT CIRCUITS |         | OPERATION       |
|-----------------|-----|-----------------|---------|-----------------|
| $\overline{OE}$ | DIR | A PORT          | B PORT  |                 |
| L               | L   | Enabled         | Hi-Z    | B data to A bus |
| L               | H   | Hi-Z            | Enabled | A data to B bus |
| H               | X   | Hi-Z            | Hi-Z    | Isolation       |

(1) Input circuits of the data I/Os always are active.

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**SN54LVT16245B, SN74LVT16245B  
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**Absolute Maximum Ratings<sup>(1)</sup>**

over recommended operating free-air temperature range (unless otherwise noted)

|               |   | MIN             | MAX            | UNIT |
|---------------|---|-----------------|----------------|------|
| $V_{CC}$      | Supply voltage range  | -0.5            | 4.6            | V    |
| $V_I$         | Input voltage range <sup>(2)</sup>  | -0.5            | 7              | V    |
| $V_O$         | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | -0.5            | 7              | V    |
| $V_O$         | Voltage range applied to any output in the high state <sup>(2)</sup>                        | -0.5            | $V_{CC} + 0.5$ | V    |
| $I_O$         | Current into any output in the low state  | SN54LVT16245B   | 96             | mA   |
|               |   | SN74LVT16245B   | 128            |      |
| $I_O$         | Current into any output in the high state <sup>(3)</sup>                                    | SN54LVT16245B   | 48             | mA   |
|               |   | SN74LVT16245B   | 64             |      |
| $I_{IK}$      | Input clamp current   | $V_I < 0$       | -50            | mA   |
| $I_{OK}$      | Output clamp current  | $V_O < 0$       | -50            | mA   |
| $\theta_{JA}$ | Package thermal impedance <sup>(4)</sup>  | DGG package     | 70             | °C/W |
|               |   | DGV package     | 58             |      |
|               |   | DL package      | 63             |      |
|               |   | GQL/ZQL package | 42             |      |
|               |   | GRD/ZRD package | 36             |      |
| $T_{stg}$     | Storage temperature range   | -65             | 150            | °C   |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This current flows only when the output is in the high state and  $V_O > V_{CC}$ .

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)</sup>**

|                     |                                    | SN54LVT16245B <sup>(2)</sup> |     | SN74LVT16245B |     | UNIT |
|---------------------|------------------------------------|------------------------------|-----|---------------|-----|------|
|                     |                                    | MIN                          | MAX | MIN           | MAX |      |
| V <sub>CC</sub>     | Supply voltage                     | 2.7                          | 3.6 | 2.7           | 3.6 | V    |
| V <sub>IH</sub>     | High-level input voltage           | 2                            |     | 2             |     | V    |
| V <sub>IL</sub>     | Low-level input voltage            |                              |     | 0.8           |     | V    |
| V <sub>I</sub>      | Input voltage                      |                              |     | 5.5           |     | V    |
| I <sub>OH</sub>     | High-level output current          |                              |     | -24           | -32 | mA   |
| I <sub>OL</sub>     | Low-level output current           |                              |     | 48            | 64  | mA   |
| Δt/Δv               | Input transition rise or fall rate | Outputs enabled              |     | 10            | 10  | ns/V |
| Δt/ΔV <sub>CC</sub> | Power-up ramp rate                 |                              |     | 200           | 200 | μs/V |
| T <sub>A</sub>      | Operating free-air temperature     | -55                          | 125 | -40           | 85  | °C   |

(1) All unused or undriven (floating) inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V<sub>CC</sub> or GND) to ensure proper device operation and minimize power. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) Product preview

**SN54LVT16245B, SN74LVT16245B  
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**Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                | TEST CONDITIONS   | SN54LVT16245B <sup>(1)</sup> |                    |                 | SN74LVT16245B  |                    |           | UNIT          |
|--------------------------|---|------------------------------|--------------------|-----------------|----------------|--------------------|-----------|---------------|
|                          |   | MIN                          | TYP <sup>(2)</sup> | MAX             | MIN            | TYP <sup>(2)</sup> | MAX       |               |
| $V_{IK}$                 | $V_{CC} = 2.7 \text{ V}$ , $I_I = -18 \text{ mA}$   |                              |                    | -1.2            |                |                    | -1.2      | V             |
| $V_{OH}$                 | $V_{CC} = 2.7 \text{ to } 3.6 \text{ V}$ , $I_{OH} = -100 \mu\text{A}$  | $V_{CC} - 0.2$               |                    |                 | $V_{CC} - 0.2$ |                    |           | V             |
|                          | $V_{CC} = 2.7 \text{ V}$ , $I_{OH} = -8 \text{ mA}$   | 2.4                          |                    |                 | 2.4            |                    |           |               |
|                          | $V_{CC} = 3 \text{ V}$  | $I_{OH} = -24 \text{ mA}$    | 2                  |                 |                |                    | 2         |               |
| $V_{OL}$                 |   | $I_{OH} = -32 \text{ mA}$    |                    |                 |                |                    |           | V             |
| $V_{CC} = 2.7 \text{ V}$ | $I_{OL} = 100 \mu\text{A}$  |                              | 0.2                |                 |                | 0.2                |           |               |
|                          | $I_{OL} = 24 \text{ mA}$  |                              | 0.5                |                 |                | 0.5                |           |               |
|                          | $I_{OL} = 16 \text{ mA}$  |                              | 0.4                |                 |                | 0.4                |           |               |
|                          | $I_{OL} = 32 \text{ mA}$  |                              | 0.5                |                 |                | 0.5                |           |               |
| $V_{CC} = 3 \text{ V}$   | $I_{OL} = 48 \text{ mA}$  |                              | 0.55               |                 |                |                    |           |               |
|                          | $I_{OL} = 64 \text{ mA}$  |                              |                    |                 |                | 0.55               |           |               |
| $I_I$                    | $V_{CC} = 3.6 \text{ V}$ , $V_I = V_{CC} \text{ or } \text{GND}$  |                              |                    | $\pm 1$         |                |                    | $\pm 1$   | $\mu\text{A}$ |
|                          | $V_{CC} = 0 \text{ or } 3.6 \text{ V}$ , $V_I = 5.5 \text{ V}$  |                              |                    | 10              |                |                    | 10        |               |
|                          | $V_{CC} = 3.6 \text{ V}$  | $V_I = 5.5 \text{ V}$        |                    | 20              |                |                    | 20        |               |
|                          |   | $V_I = V_{CC}$               |                    | 5               |                |                    | 1         |               |
|                          |   | $V_I = 0$                    |                    | -5              |                |                    | -5        |               |
| $I_{off}$                | $V_{CC} = 0$ , $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$  |                              |                    |                 |                |                    | $\pm 100$ | $\mu\text{A}$ |
| $I_{OZPU}$               | $V_{CC} = 0 \text{ to } 1.5 \text{ V}$ , $V_O = 0.5 \text{ V to } 3 \text{ V}$ , $\overline{OE} = \text{don't care}$        |                              |                    | $\pm 100^{(4)}$ |                |                    | $\pm 100$ | $\mu\text{A}$ |
| $I_{OZPD}$               | $V_{CC} = 1.5 \text{ V to } 0$ , $V_O = 0.5 \text{ V to } 3 \text{ V}$ , $\overline{OE} = \text{don't care}$                |                              |                    | $\pm 100^{(4)}$ |                |                    | $\pm 100$ | $\mu\text{A}$ |
| $I_{CC}$                 | $V_{CC} = 3.6 \text{ V}$ , $I_O = 0$ , $V_I = V_{CC} \text{ or } \text{GND}$  | Outputs high                 |                    | 0.19            |                |                    | 0.19      | $\text{mA}$   |
|                          |   | Outputs low                  |                    | 5               |                |                    | 5         |               |
|                          |   | Outputs disabled             |                    | 0.19            |                |                    | 0.19      |               |
| $\Delta I_{CC}^{(5)}$    | $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ , One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC}$ or $\text{GND}$ |                              |                    | 0.2             |                |                    | 0.2       | $\text{mA}$   |
| $C_I$                    | $V_I = 3 \text{ V or } 0$   |                              |                    | 4               |                |                    | 4         | $\text{pF}$   |
| $C_{io}$                 | $V_O = 3 \text{ V or } 0$   |                              |                    | 10              |                |                    | 10        | $\text{pF}$   |

(1) Product preview

(2) All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(3) Unused pins at  $V_{CC}$  or  $\text{GND}$ .

(4) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(5) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or  $\text{GND}$ .

## Switching Characteristics

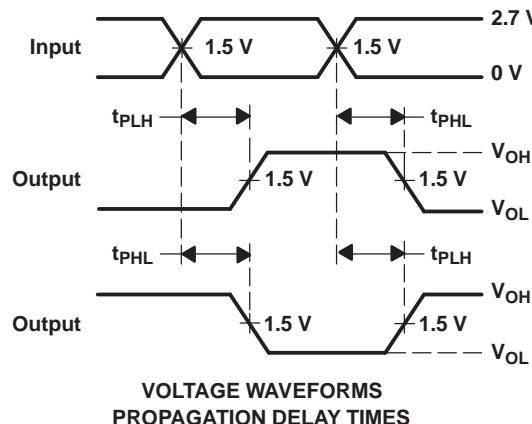
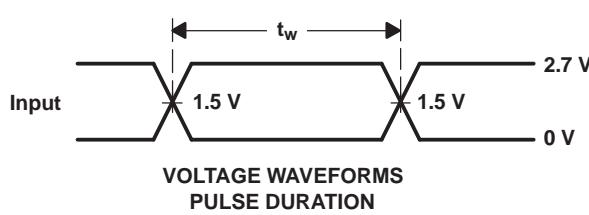
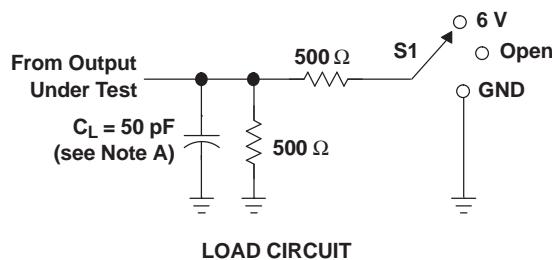
over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see [Figure 1](#))

| PARAMETER    | FROM<br>(INPUT) | TO<br>(OUTPUT) | SN54LVT16245B <sup>(1)</sup>               |     | SN74LVT16245B            |     |  |                    | UNIT |    |
|--------------|-----------------|----------------|--|-----|--------------------------|-----|--|--------------------|------|----|
|              |                 |                | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ |     | $V_{CC} = 2.7 \text{ V}$ |     | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ |                    |      |    |
|              |                 |                | MIN  | MAX | MIN                      | MAX | MIN  | TYP <sup>(2)</sup> | MAX  |    |
| $t_{PLH}$    | A or B          | B or A         | 0.5  | 4.5 | 4.6                      | 1.5 | 2.3  | 3.3                | 3.7  | ns |
| $t_{PHL}$    |                 |                | 0.5  | 4.4 | 3.9                      | 1.3 | 2.1  | 3.3                | 3.5  |    |
| $t_{PZH}$    | $\overline{OE}$ | A or B         | 0.5  | 6.5 | 6.6                      | 1.5 | 2.8  | 4.5                | 5.3  | ns |
| $t_{PZL}$    |                 |                | 0.5  | 5.4 | 6.2                      | 1.6 | 2.9  | 4.6                | 5.2  |    |
| $t_{PHZ}$    | $\overline{OE}$ | A or B         | 1  | 6.8 | 7                        | 2.3 | 3.7  | 5.1                | 5.5  | ns |
| $t_{PLZ}$    |                 |                | 1  | 6.2 | 6.3                      | 2.2 | 3.5  | 5.1                | 5.4  |    |
| $t_{sk(LH)}$ |                 |                |  |     |                          |     |  | 0.5                |      | ns |
| $t_{sk(HL)}$ |                 |                |  |     |                          |     |  | 0.5                |      |    |

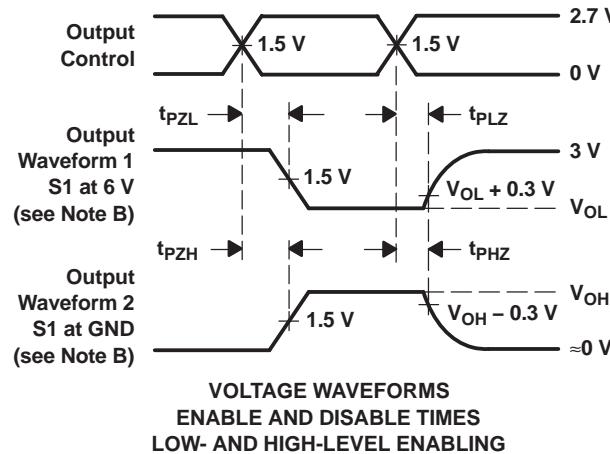
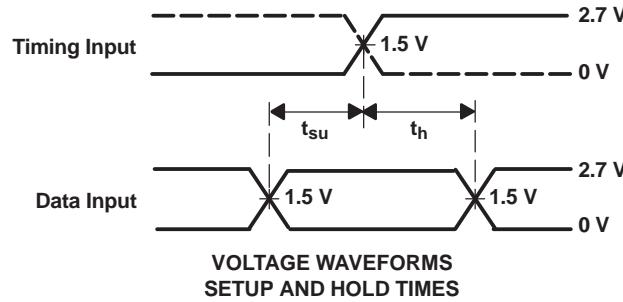
(1) Product preview

(2) All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## PARAMETER MEASUREMENT INFORMATION



| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V  |
| $t_{PHZ}/t_{PZH}$ | GND  |



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $\text{PRR} \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable Device  | Status<br>(1) | Package Type               | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples   |
|-------------------|---------------|----------------------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|---|
| 74LVT16245BDGGRE4 | ACTIVE        | TSSOP                      | DGG             | 48   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LVT16245B               | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| 74LVT16245BDGGRG4 | ACTIVE        | TSSOP                      | DGG             | 48   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LVT16245B               | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LVT16245BDGGR | ACTIVE        | TSSOP                      | DGG             | 48   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LVT16245B               | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LVT16245BDGVR | ACTIVE        | TVSOP                      | DGV             | 48   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | VD245B                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LVT16245BDL   | ACTIVE        | SSOP                       | DL              | 48   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LVT16245B               | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LVT16245BDLG4 | ACTIVE        | SSOP                       | DL              | 48   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LVT16245B               | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LVT16245BDLRL | ACTIVE        | SSOP                       | DL              | 48   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LVT16245B               | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LVT16245BGQLR | OBsolete      | BGA<br>MICROSTAR<br>JUNIOR | GQL             | 56   |             | TBD                     | Call TI                 | Call TI              | -40 to 85    |                         |   |
| SN74LVT16245BGRDR | OBsolete      | BGA<br>MICROSTAR<br>JUNIOR | GRD             | 54   |             | TBD                     | Call TI                 | Call TI              | -40 to 85    |                         |   |
| SN74LVT16245BZQLR | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZQL             | 56   | 1000        | Green (RoHS & no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | VD245B                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN74LVT16245BZRDR | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZRD             | 54   | 1000        | Green (RoHS & no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | VD245B                  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

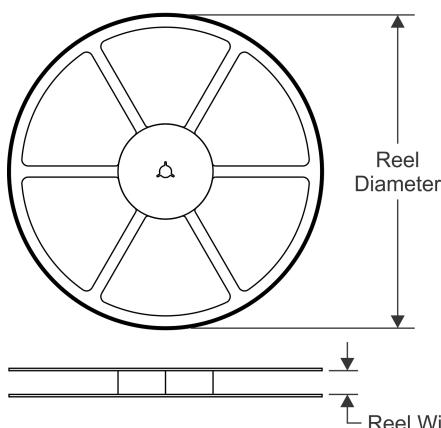
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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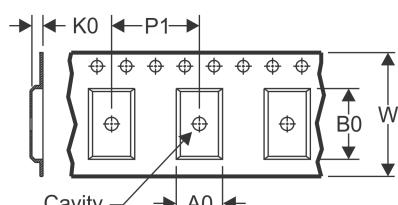
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## TAPE AND REEL INFORMATION

## REEL DIMENSIONS

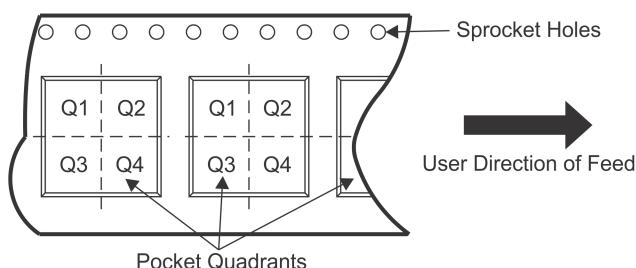


## TAPE DIMENSIONS



|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| All dimensions are nominal |                      |                 |      |      |                    |                    |         |         |         |         |        |               |  |
|----------------------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|--|
| Device                     | Package Type         | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |  |
| SN74LVT16245BDGGR          | TSSOP                | DGG             | 48   | 2000 | 330.0              | 24.4               | 8.6     | 15.8    | 1.8     | 12.0    | 24.0   | Q1            |  |
| SN74LVT16245BDGVR          | TVSOP                | DGV             | 48   | 2000 | 330.0              | 16.4               | 7.1     | 10.2    | 1.6     | 12.0    | 16.0   | Q1            |  |
| SN74LVT16245BDLR           | SSOP                 | DL              | 48   | 1000 | 330.0              | 32.4               | 11.35   | 16.2    | 3.1     | 16.0    | 32.0   | Q1            |  |
| SN74LVT16245BZQLR          | BGA MICROSTAR JUNIOR | ZQL             | 56   | 1000 | 330.0              | 16.4               | 4.8     | 7.3     | 1.5     | 8.0     | 16.0   | Q1            |  |
| SN74LVT16245BZRDR          | BGA MICROSTAR JUNIOR | ZRD             | 54   | 1000 | 330.0              | 16.4               | 5.8     | 8.3     | 1.55    | 8.0     | 16.0   | Q1            |  |

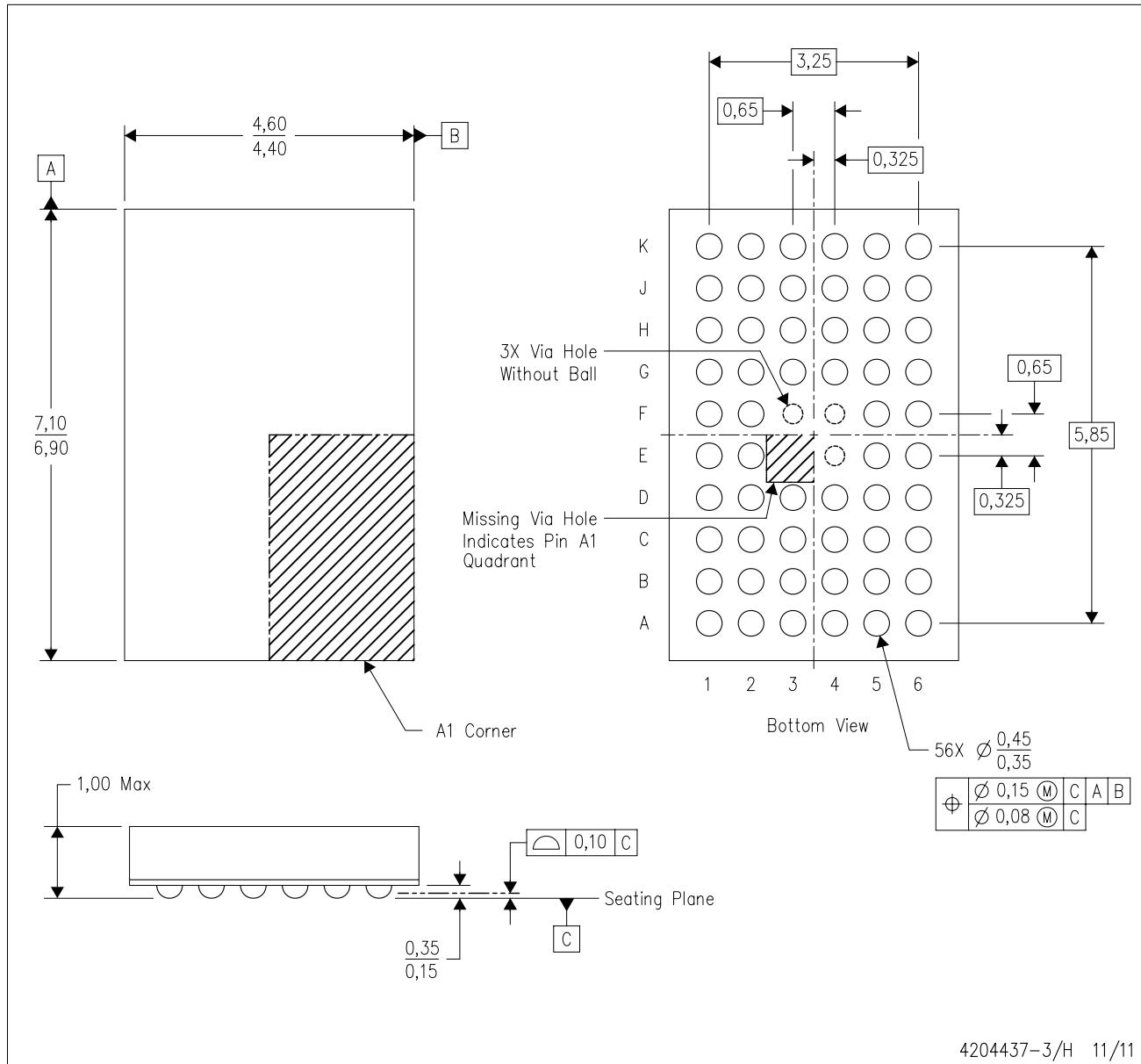
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device            | Package Type            | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|-------------------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVT16245BDGGR | TSSOP                   | DGG             | 48   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LVT16245BDGVR | TVSOP                   | DGV             | 48   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74LVT16245BDLR  | SSOP                    | DL              | 48   | 1000 | 367.0       | 367.0      | 55.0        |
| SN74LVT16245BZQLR | BGA MICROSTAR<br>JUNIOR | ZQL             | 56   | 1000 | 336.6       | 336.6      | 28.6        |
| SN74LVT16245BZRDR | BGA MICROSTAR<br>JUNIOR | ZRD             | 54   | 1000 | 336.6       | 336.6      | 28.6        |

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



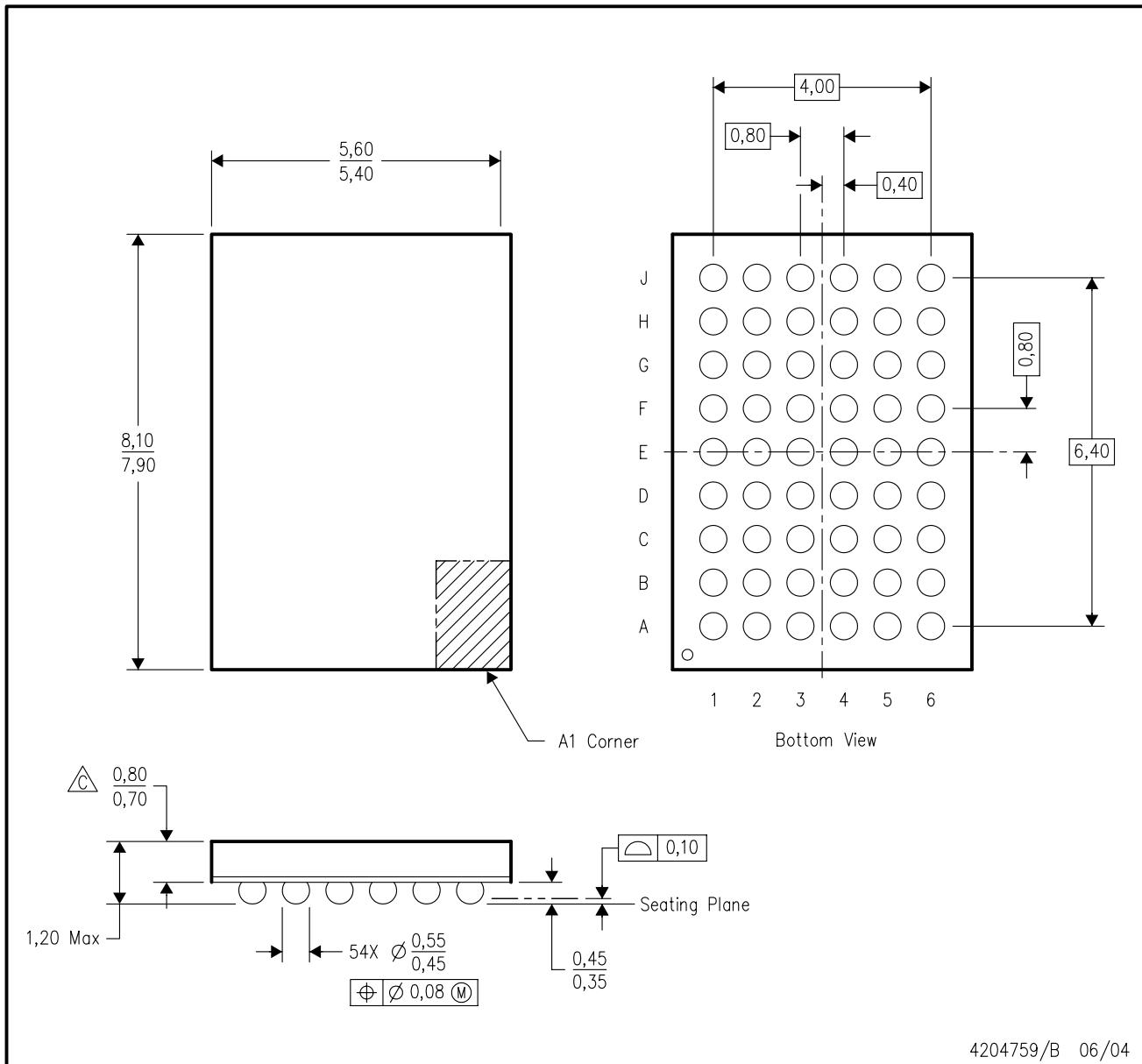
NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Falls within JEDEC MO-285 variation BA-2.
- This package is Pb-free. Refer to the 56 QGL package (drawing 4200583) for tin-lead (SnPb).

4204437-3/H 11/11

## GRD (R-PBGA-N54)

## PLASTIC BALL GRID ARRAY



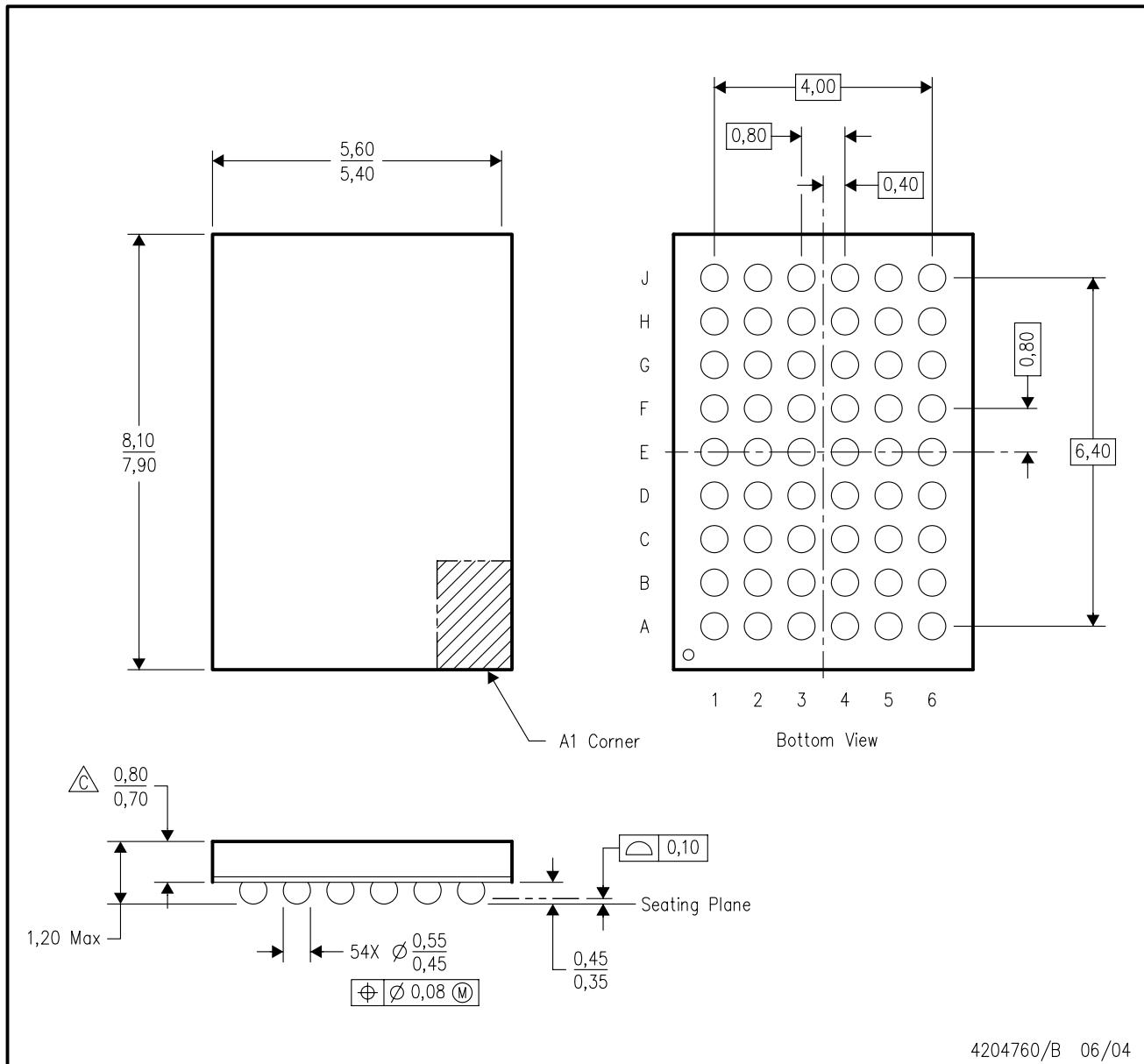
NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.

Falls within JEDEC MO-205 variation DD.

D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

## ZRD (R-PBGA-N54)

## PLASTIC BALL GRID ARRAY



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-205 variation DD.
- D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

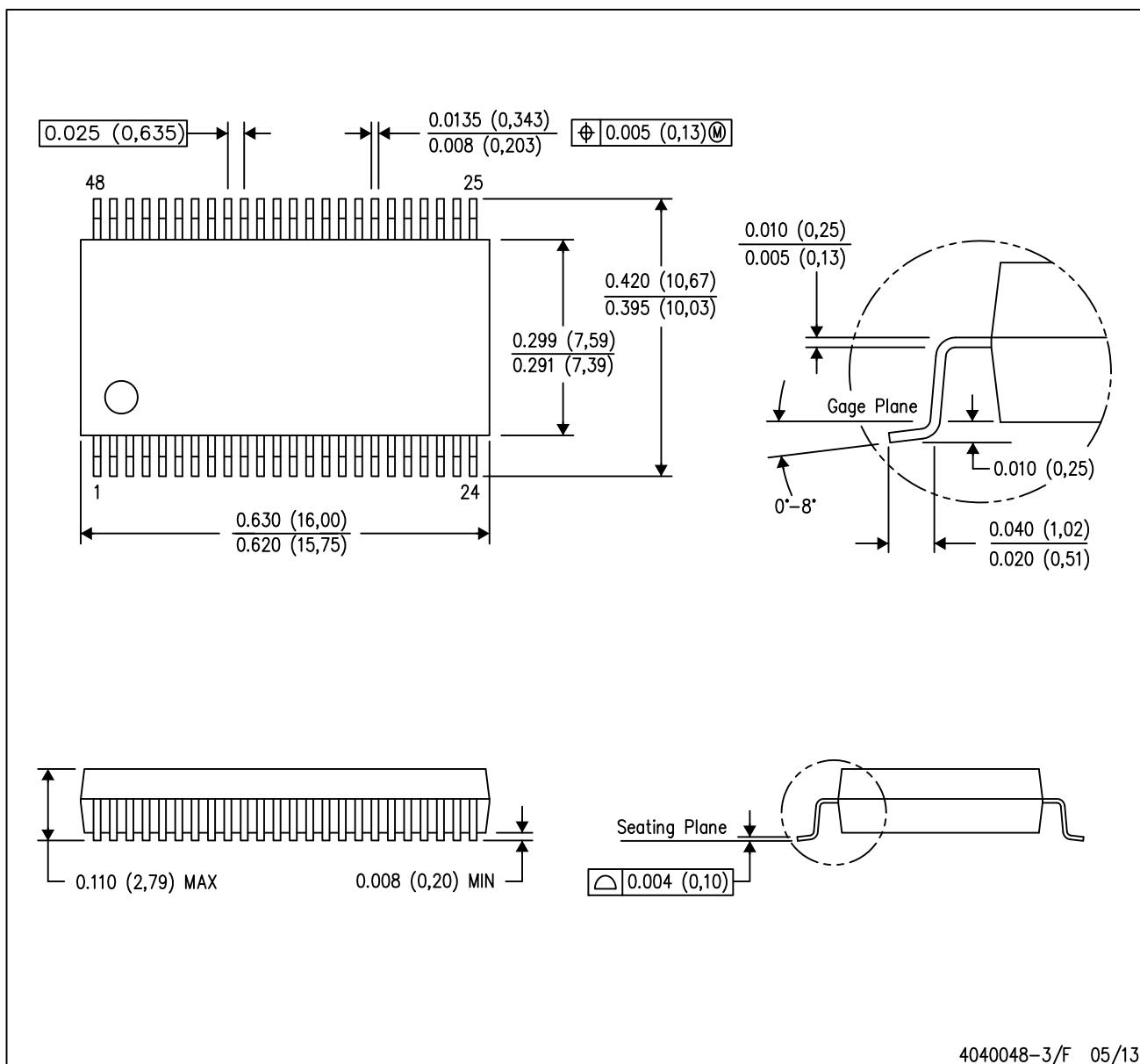
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



4040048-3/F 05/13

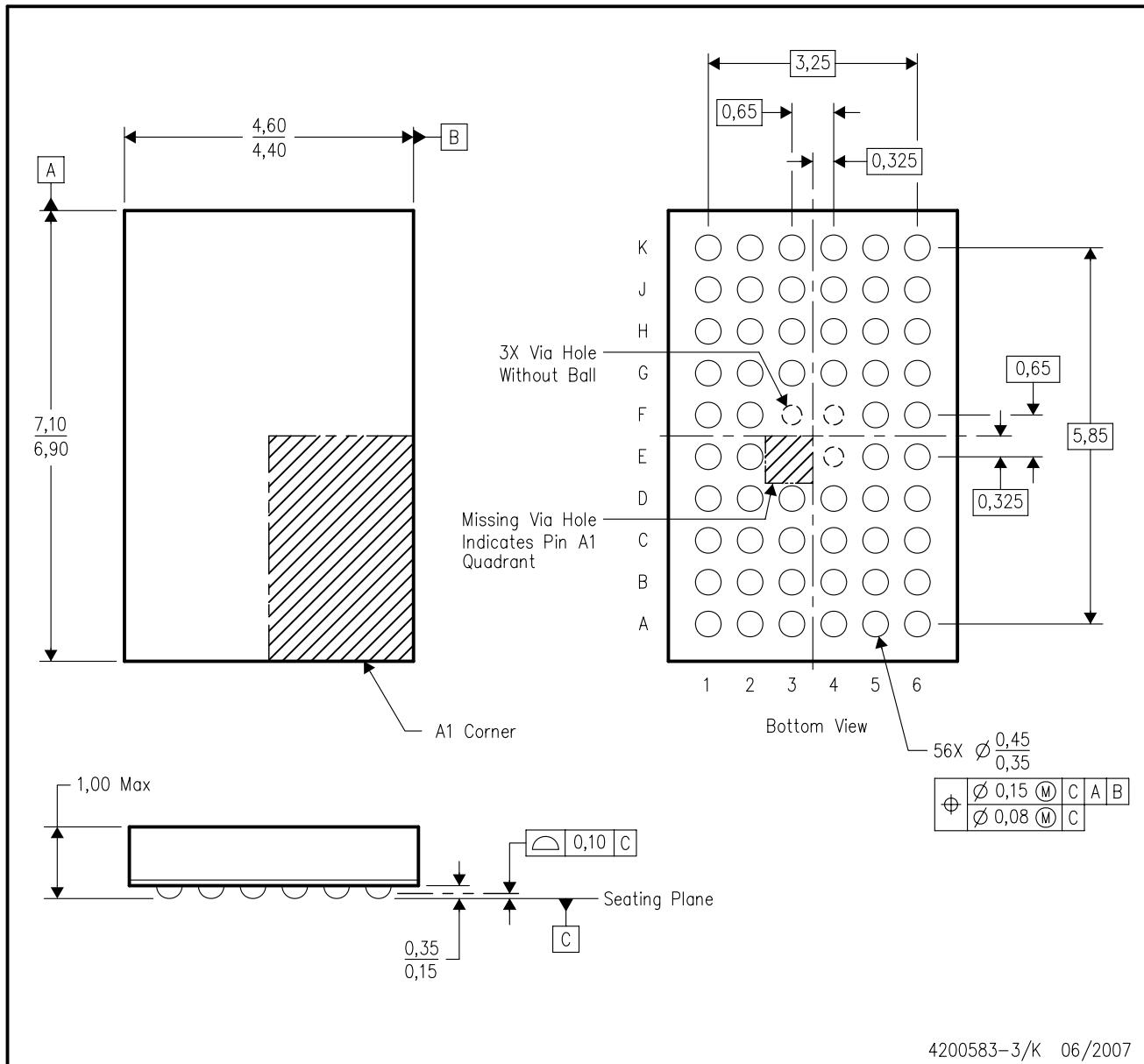
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MO-118

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## GQL (R-PBGA-N56)

## PLASTIC BALL GRID ARRAY



4200583-3/K 06/2007

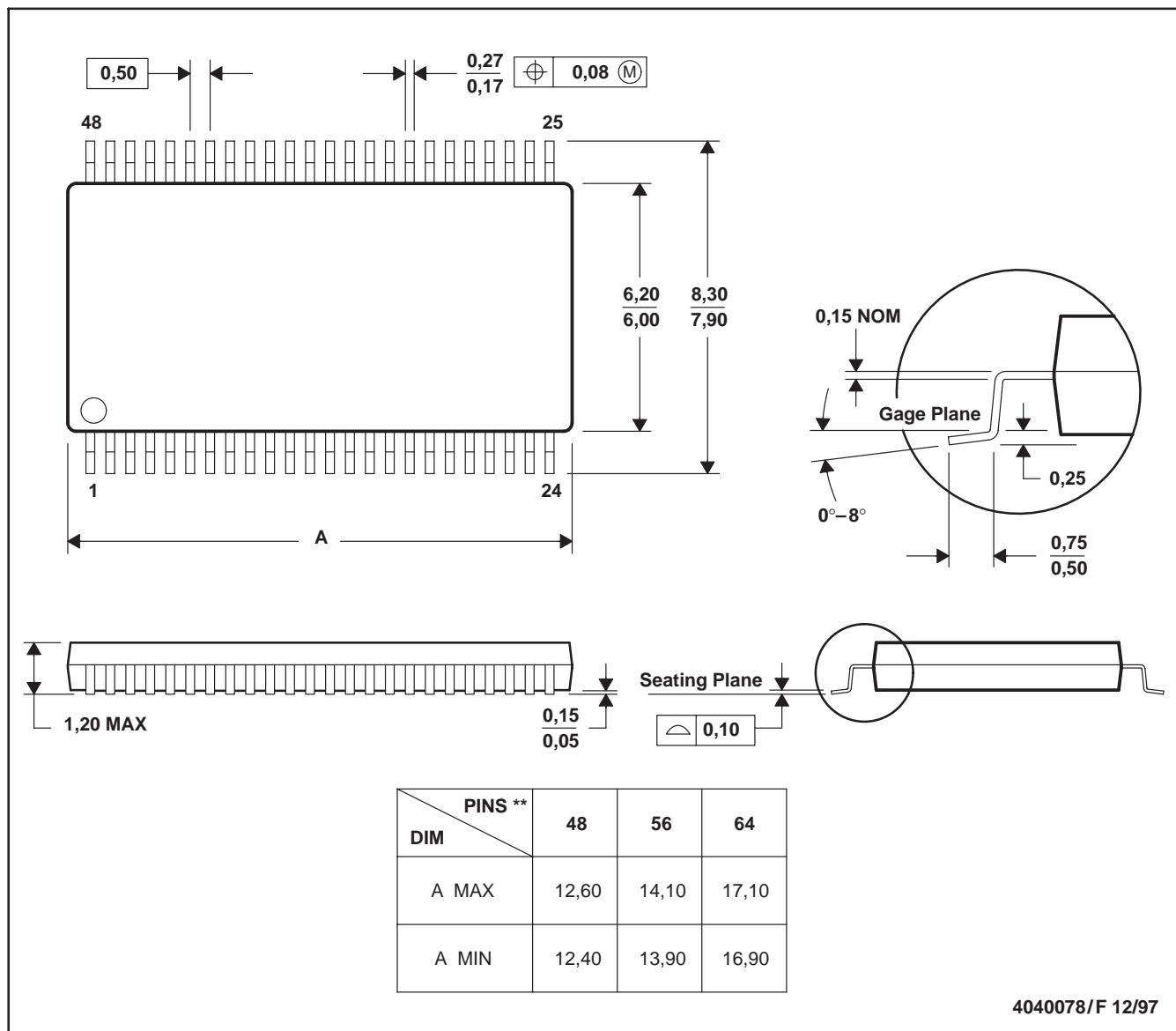
NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Falls within JEDEC MO-285 variation BA-2.
- This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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