

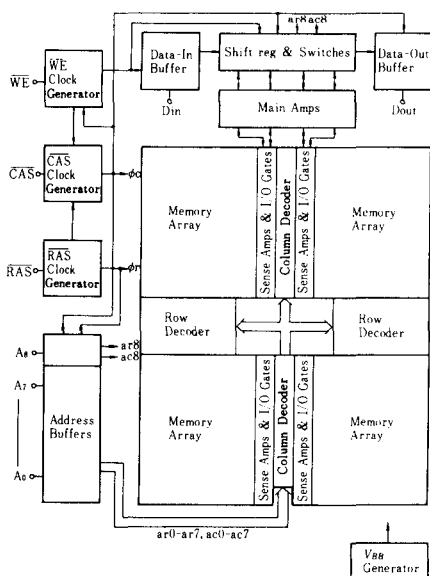
HM50257-12, HM50257-15, HM50257-20, HM50257P-12, HM50257P-15, HM50257P-20

262144-word $\times$ 1-bit Dynamic Random Access Memory

■ FEATURES

- Industry standard 16-pin DIP
- Single 5V ($\pm 10\%$)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns (max.)
- Common I/O capability using early write operation
- Nibble mode capability
- TTL compatible
- 256 refresh cycles (4ms)
- 3 Variations of refresh: RAS only refresh, CAS before RAS refresh, Hidden refresh

■ BLOCK DIAGRAM



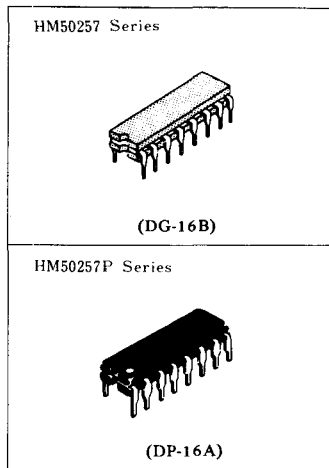
■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} -1V to +7V
 Operating temperature, T_a (Ambient) 0°C to $+70^\circ\text{C}$
 Storage temperature (Cerdip) -65°C to $+150^\circ\text{C}$
 (Plastic DIP) -55°C to $+125^\circ\text{C}$
 Power dissipation 1W
 Short circuit output current 50mA

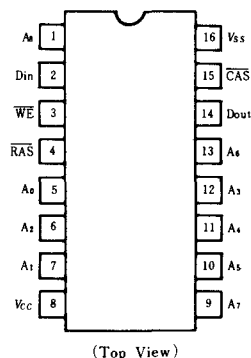
■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

Note 1) All voltages referenced to V_{SS} .



■ PIN ARRANGEMENT



$A_0 \sim A_8$	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
WE	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 \sim A_7$	Refresh Address Inputs

■DC ELECTRICAL CHARACTERISTICS ($T_a=0$ to $+70^{\circ}\text{C}$, $V_{CC}=5\text{V}\pm 10\%$, $V_{SS}=0\text{V}$)

Parameter	Symbol	HM50257-12		HM50257-15		HM50257-20		Unit	Notes
		min	max	min	max	min	max		
Operating Current (RAS, CAS Cycling: $t_{RC}=\text{min}$)	I_{CC1}	—	83	—	70	—	55	mA	1
Stand by Current (RAS= V_{IH} , Dout=High Impedance)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA	
Refresh Current (RAS only Refresh, $t_{RC}=\text{min}$)	I_{CC3}	—	62	—	53	—	42	mA	
Standby Current (RAS= V_{IH} , Dout Enable)	I_{CC5}	—	10	—	10	—	10	mA	1
Refresh Current (CAS before RAS Refresh, $t_{RC}=\text{min}$)	I_{CC6}	—	69	—	58	—	45	mA	
Input leakage ($0 < V_{in} < 7\text{V}$)	I_{LI}	-10	10	-10	10	-10	10	μA	
Output leakage ($0 < V_{out} < 7\text{V}$)	I_{LO}	-10	10	-10	10	-10	10	μA	
Output levels High ($I_{out}=-5\text{mA}$)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low ($I_{out}=4.2\text{mA}$)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected I_{CC} max. is specified at the output open condition.

■CAPACITANCE ($V_{CC}=5\text{V}\pm 10\%$, $T_a=25^{\circ}\text{C}$)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-In	C_{I1}	—	5	pF	1
	Clocks, Data-Out	C_{I2}	—	7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. CAS= V_{IH} to disable Dout.

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($T_a=0$ to $+70^{\circ}\text{C}$, $V_{CC}=5\text{V}\pm 10\%$, $V_{SS}=0\text{V}$) ^{1), 10), 11)}

Parameter	Symbol	HM50257/P-12		HM50257/P-15		HM50257/P-20		Unit	Notes
		min	max	min	max	min	max		
Access Time from RAS	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time from CAS	t_{CAC}	—	60	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	30	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
RAS Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
RAS Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
RAS Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
RAS to CAS Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
RAS Hold Time	t_{RSH}	60	—	75	—	100	—	ns	
CAS Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
CAS to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time referenced to RAS	t_{AR}	80	—	100	—	130	—	ns	
WE Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time referenced to RAS	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to RAS Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to CAS Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	8, 9
Data-in Hold Time referenced to RAS	t_{DHR}	100	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to CAS	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to RAS	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	

(to be continued)

Parameter	Symbol	HM50257/P-12		HM50257/P-15		HM50257/P-20		Unit	Notes
		min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	265	—	310	—	390	—	ns	
CAS to WE Delay	t_{CWD}	60	—	75	—	100	—	ns	8
RAS to WE Delay	t_{RWD}	120	—	150	—	200	—	ns	
CAS Precharge Time	t_{CPN}	50	—	60	—	80	—	ns	
CAS Setup Time	t_{CSR}	10	—	10	—	10	—	ns	
CAS Hold Time (CAS before RAS Refresh)	t_{CHR}	120	—	150	—	200	—	ns	
RAS Precharge to CAS Hold Time	t_{RPC}	0	—	0	—	0	—	ns	

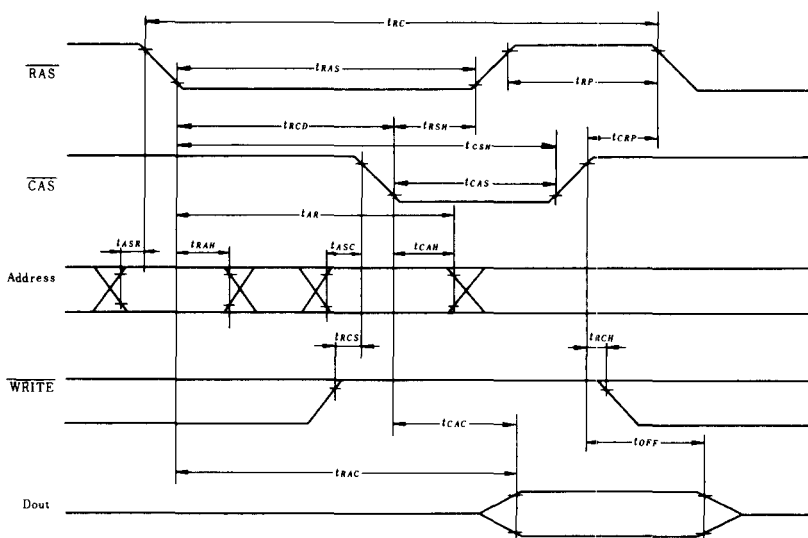
Notes

1. AC measurements assume $t_T = 5\text{ns}$.
2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
5. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
6. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
7. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, access time is controlled exclusively by t_{CAC} .

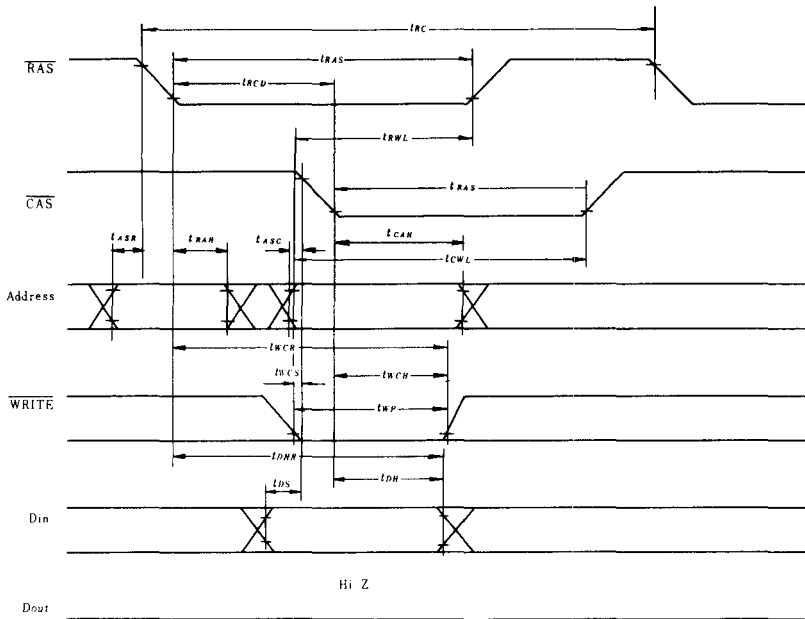
8. t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters.
They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{RWD} \geq t_{RWD}(\text{min})$, the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to CAS leading edge in early write cycles and to WE leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100 μs is required after power-up then excute at least 8 initialization cycles.
11. At least, 8 CAS before RAS refresh cycle are required before using internal refresh counter.

TIMING WAVEFORMS

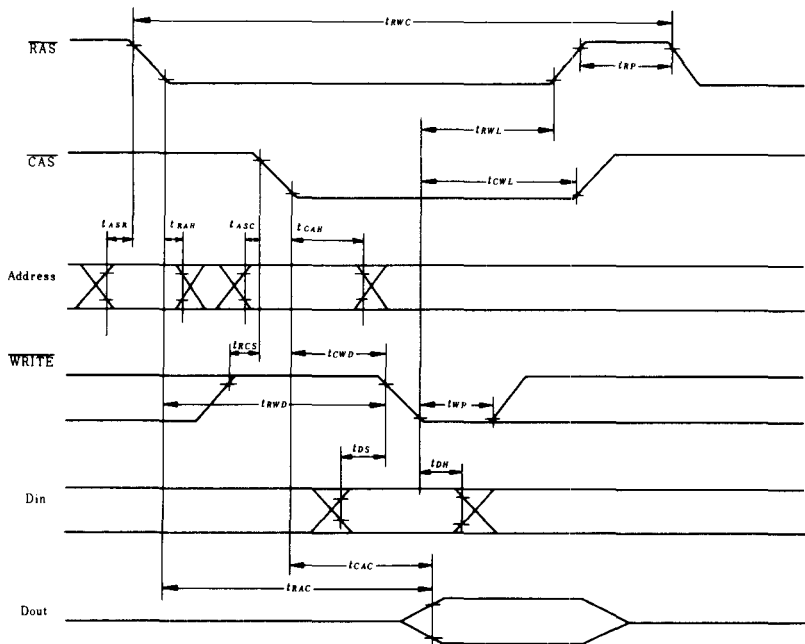
READ CYCLE



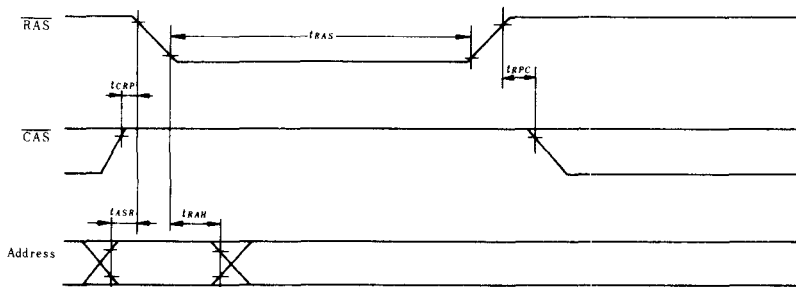
● WRITE CYCLE



● READ MODIFY WRITE CYCLE

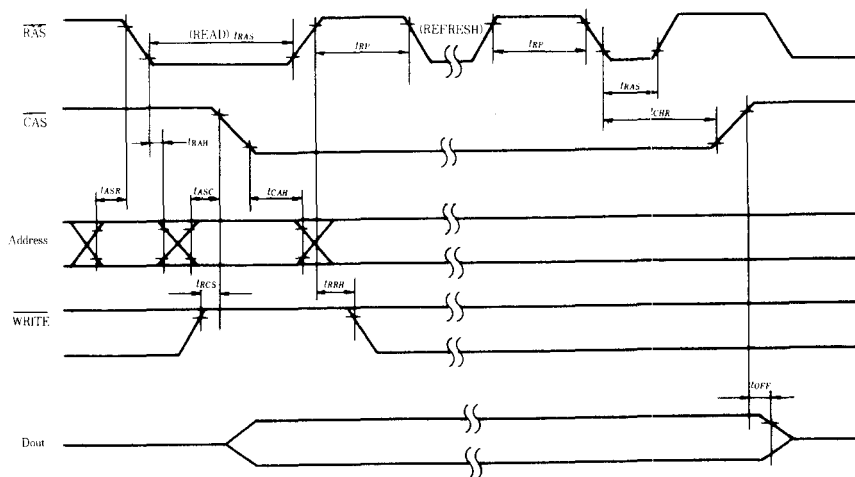


● RAS ONLY REFRESH CYCLE

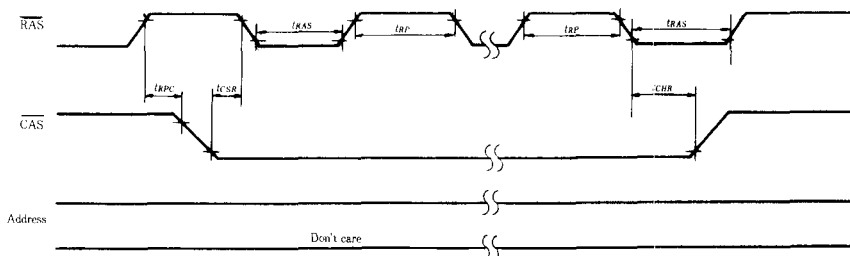


* REFRESH ADDRESS $A_0 - A_7 (AX_0 - AX_7)$

● HIDDEN REFRESH CYCLE



● CAS BEFORE RAS REFRESH CYCLE



● NIBBLE MODE WRITE CYCLE

