



LD6805 series

Low-dropout regulators, high PSRR, 150 mA

Rev. 4 — 7 June 2013

Product data sheet

1. Product profile

1.1 General description

The LD6805 series is a small-size Low DropOut regulator (LDO) family with ultra high Power Supply Rejection Ratio (PSRR) of 75 dB. The voltage drop is 250 mV at 150 mA current rating. Operating voltages can range from 2.3 V to 5.5 V. Each device has a fixed output voltage $V_{O(nom)}$ between 1.2 V and 3.6 V.

The LD6805K/xxH devices show a high-ohmic state (3-state) at the output pin when set to disabled mode. The LD6805K/xxP devices contain a pull-down switching transistor to provide a low-ohmic output state (auto discharge function) in disabled mode.

The LD6805 series devices are available in a DFN1010C-4 (SOT1194-1) plastic package with a size of $1 \times 1 \times 0.55$ mm. The devices are ideal for use in portable applications requiring component miniaturization.

1.2 Features and benefits

- High PSRR
- Overcurrent protection
- Auto discharge or high-ohmic output state when disabled
- Low quiescent current (0.1 μ A) in shutdown mode
- High-level ElectroStatic Discharge (ESD) protection (6 kV Human Body Model (HBM))
- DFN1010C-4 (SOT1194-1) plastic package with a size of $1 \times 1 \times 0.55$ mm
- Pb-free, Restriction of Hazardous Substances (RoHS) compliant, free of halogen and antimony (dark green compliant)

1.3 Applications

- Smartphones
- Mobile handsets
- Digital still cameras
- Tablet PCs
- Mobile internet devices
- Portable media players

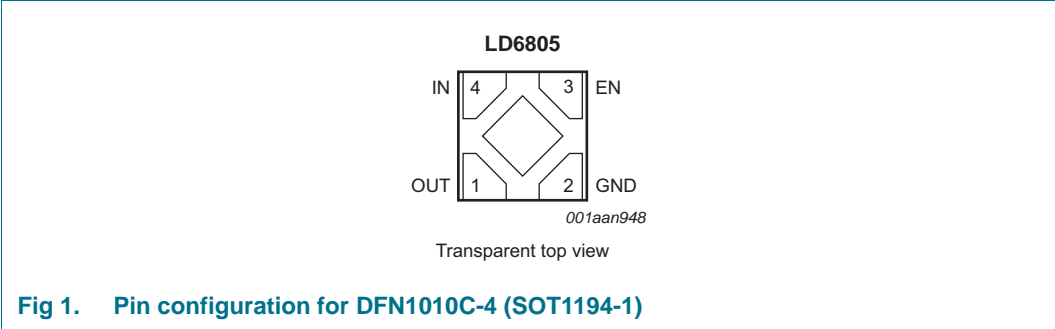
1.4 Quick reference data

- $I_O = 150$ mA
- PSRR = 75 dB at 1 kHz
- RMS noise $V_{n(o)RMS} = 40$ μ V at 10 Hz to 100 kHz
- $t_{startup(reg)} = 150$ μ s
- $V_I = 2.3$ V to 5.5 V
- $V_O = 1.2$ V to 3.6 V
- Dropout voltage $V_{do} = 250$ mV at $I_O = 150$ mA
- Quiescent current $I_q = 35$ μ A at 0 mA



2. Pinning information

2.1 Pinning



2.2 Pin description

Table 1. Pin description for DFN1010C-4 (SOT1194-1)

Symbol	Pin	Description
OUT	1	regulator output voltage
GND	2	supply ground
EN	3	device enable input; active HIGH
IN	4	regulator input voltage
i.c.	TAB	internal connected ^[1]

[1] The TAB is GND level (it is placed on the reverse side of the IC). It is recommended to connect the TAB to GND. Leaving it unconnected is also allowed but it may result in lower thermal performance.

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
LD6805 series	DFN1010C-4	plastic thermal enhanced ultra thin small outline package; no leads; 4 terminals; body 1 × 1 × 0.55 mm	SOT1194-1

Further ordering options see [Section 3.1 “Ordering options”](#).

3.1 Ordering options

Further information on output voltage is available on request; see [Section 20 “Contact information”](#). An explanation of high-ohmic and pull-down type is in [Section 4 “Block diagram”](#).

Table 3. Type number extension of high-ohmic output

Type number	Nominal output voltage $V_{O(nom)}$	Type number	Nominal output voltage $V_{O(nom)}$
LD6805K/12H	1.2 V	LD6805K/22H	2.2 V
LD6805K/13H	1.3 V	LD6805K/23H	2.3 V
LD6805K/14H	1.4 V	LD6805K/25H	2.5 V
LD6805K/15H	1.5 V	LD6805K/28H	2.8 V
LD6805K/16H	1.6 V	LD6805K/29H	2.9 V
LD6805K/18H	1.8 V	LD6805K/30H	3.0 V
LD6805K/185H	1.85 V	LD6805K/31H	3.1 V
LD6805K/20H	2.0 V	LD6805K/33H	3.3 V
LD6805K/21H	2.1 V	LD6805K/36H	3.6 V

Table 4. Type number extension of pull-down output

Type number	Nominal output voltage $V_{O(nom)}$	Type number	Nominal output voltage $V_{O(nom)}$
LD6805K/12P	1.2 V	LD6805K/23P	2.3 V
LD6805K/13P	1.3 V	LD6805K/25P	2.5 V
LD6805K/14P	1.4 V	LD6805K/26P	2.6 V
LD6805K/15P	1.5 V	LD6805K/28P	2.8 V
LD6805K/16P	1.6 V	LD6805K/29P	2.9 V
LD6805K/18P	1.8 V	LD6805K/30P	3.0 V
LD6805K/20P	2.0 V	LD6805K/31P	3.1 V
LD6805K/21P	2.1 V	LD6805K/33P	3.3 V
LD6805K/22P	2.2 V	LD6805K/36P	3.6 V

4. Block diagram

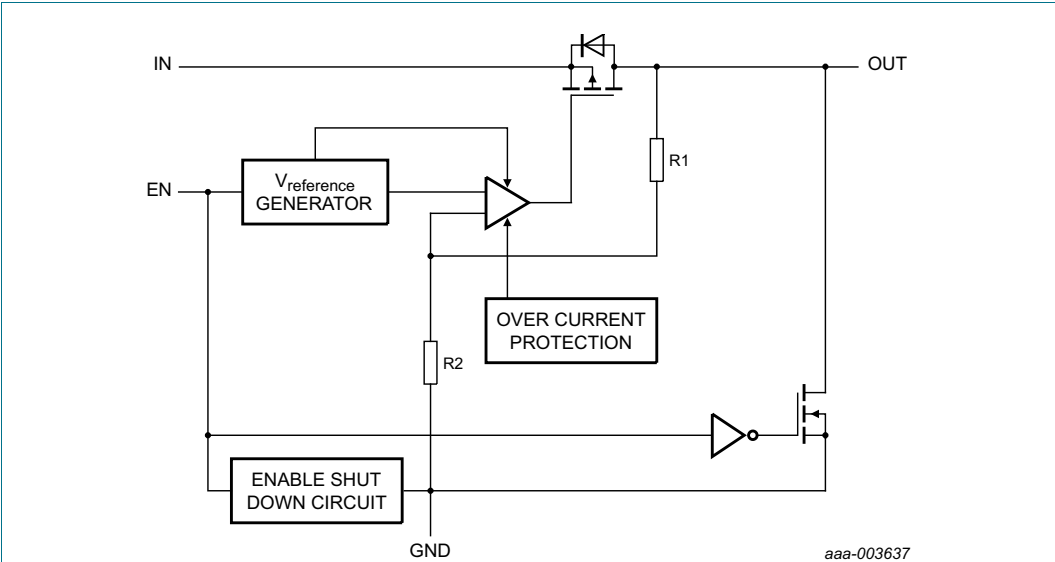


Fig 2. Block diagram of LD6805K/xxP (auto discharge function)

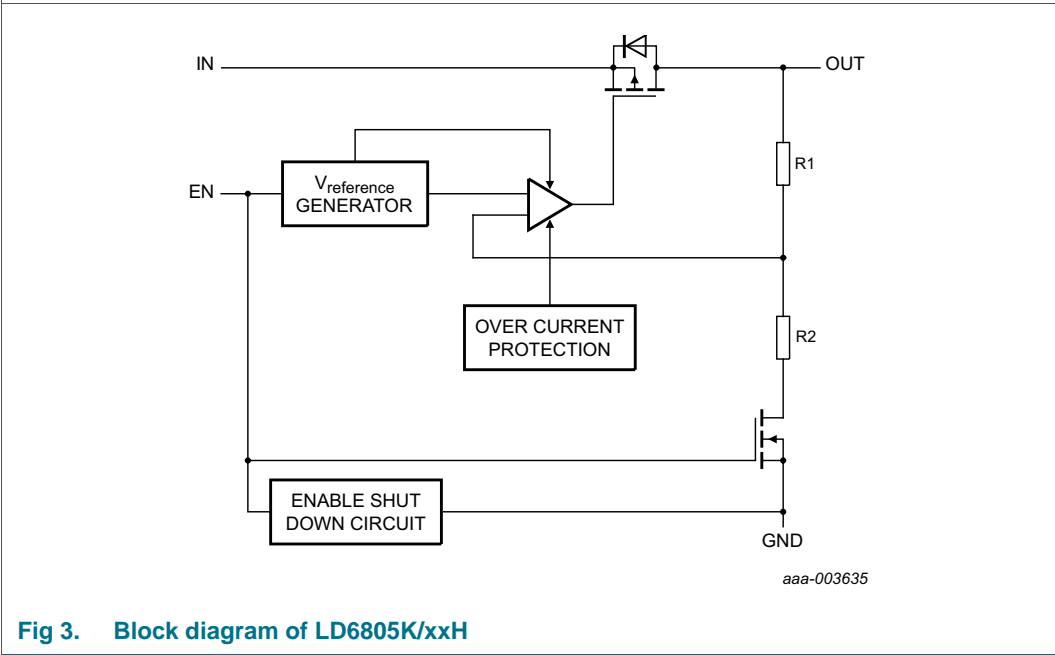


Fig 3. Block diagram of LD6805K/xxH

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _I	input voltage	4 ms transient	−0.5	+6	V
V _{EN}	voltage on pin EN		−0.5	+6	V
V _O	output voltage		−0.5	+6	V
P _{tot}	total power dissipation		[1] -	400	mW
T _{stg}	storage temperature		−55	+150	°C
T _j	junction temperature		−40	+125	°C
T _{amb}	ambient temperature		−40	+85	°C
V _{ESD}	electrostatic discharge voltage	human body model level 6	[2] -	±6	kV
		machine model class 3	[3] -	±400	V

[1] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 25 °C and the use of a two-layer Printed-Circuit Board (PCB).

[2] According to IEC 61340-3-1.

[3] According to JESD22-A115C.

6. Recommended operating conditions

Table 6. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{amb}	ambient temperature		−40	-	+85	°C
T _j	junction temperature		-	-	+125	°C
Pin IN						
V _I	input voltage		2.3	-	5.5	V
Pin EN						
V _{EN}	voltage on pin EN		0	-	V _I	V
Pin OUT						
V _O	output voltage		−0.5	-	V _I + 0.3	V
C _{L(ext)}	external load capacitance		[1] 0.7	1.0	-	μF

[1] See [Section 10.1 "Capacitor values"](#).

7. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1][2] 250	K/W

- [1] The overall $R_{th(j-a)}$ can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$, all pins must have a solid connection to larger Cu layer areas for example to the power and ground layer. In multilayer PCB applications, the second layer is used to create a large heat spreader area directly below the LDO. If this layer is either ground or power, it is connected with several vias to the top layer connecting to the device ground or supply. Avoid the use of solder-stop varnish under the chip.
- [2] Use the measurement data given for a rough estimation of the $R_{th(j-a)}$ in your application. The actual $R_{th(j-a)}$ value can vary in applications using different layer stacks and layouts.

8. Characteristics

Table 8. Electrical characteristics

At recommended input voltages and $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output voltage						
V_{do}	dropout voltage	$I_O = 150\text{ mA}$; $V_I < V_{O(nom)}$	-	250	-	mV
ΔV_O	output voltage variation	$V_O \geq 1.8\text{ V}$; $I_O = 1\text{ mA}$				
		$T_{amb} = +25\text{ }^{\circ}\text{C}$	-2	± 0.5	+2	%
		$-30\text{ }^{\circ}\text{C} \leq T_{amb} \leq +85\text{ }^{\circ}\text{C}$	-3	-	+3	%
		$V_O < 1.8\text{ V}$; $I_O = 1\text{ mA}$				
		$T_{amb} = +25\text{ }^{\circ}\text{C}$	-3	± 0.5	+3	%
		$-30\text{ }^{\circ}\text{C} \leq T_{amb} \leq +85\text{ }^{\circ}\text{C}$	-4	-	+4	%
Line regulation error						
$\Delta V_O / (V_O \times \Delta V_I)$	relative output voltage variation with input voltage	$V_I = (V_{O(nom)} + 0.5\text{ V})$ to 5.5 V	-0.1	-	+0.1	%/V
Load regulation error						
$\Delta V_O / (V_O \times \Delta I_O)$	relative output voltage variation with output current	$1\text{ mA} \leq I_O \leq 150\text{ mA}$	-	0.0025	0.01	%/mA
Output current						
I_O	output current		-	-	150	mA
I_{OM}	peak output current	$V_I = (V_{O(nom)} + 0.5\text{ V})$ to 5.5 V				
		$V_{O(nom)} > 1.8\text{ V}$; $V_O = 0.95 \times V_{O(nom)}$	200	-	-	mA
		$V_{O(nom)} < 1.8\text{ V}$; $V_O = 0.9 \times V_{O(nom)}$	200	-	-	mA
I_{sc}	short-circuit current	pin OUT	-	300	-	mA
Regulator quiescent current						
I_q	quiescent current	$V_{EN} = 1.1\text{ V}$; $I_O = 0\text{ mA}$	-	35	-	μA
		$V_{EN} = 1.1\text{ V}$; $1\text{ mA} \leq I_O \leq 150\text{ mA}$	-	150	-	μA
		$V_{EN} \leq 0.4\text{ V}$	-	0.1	1	μA

Table 8. Electrical characteristics ...continued

At recommended input voltages and $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

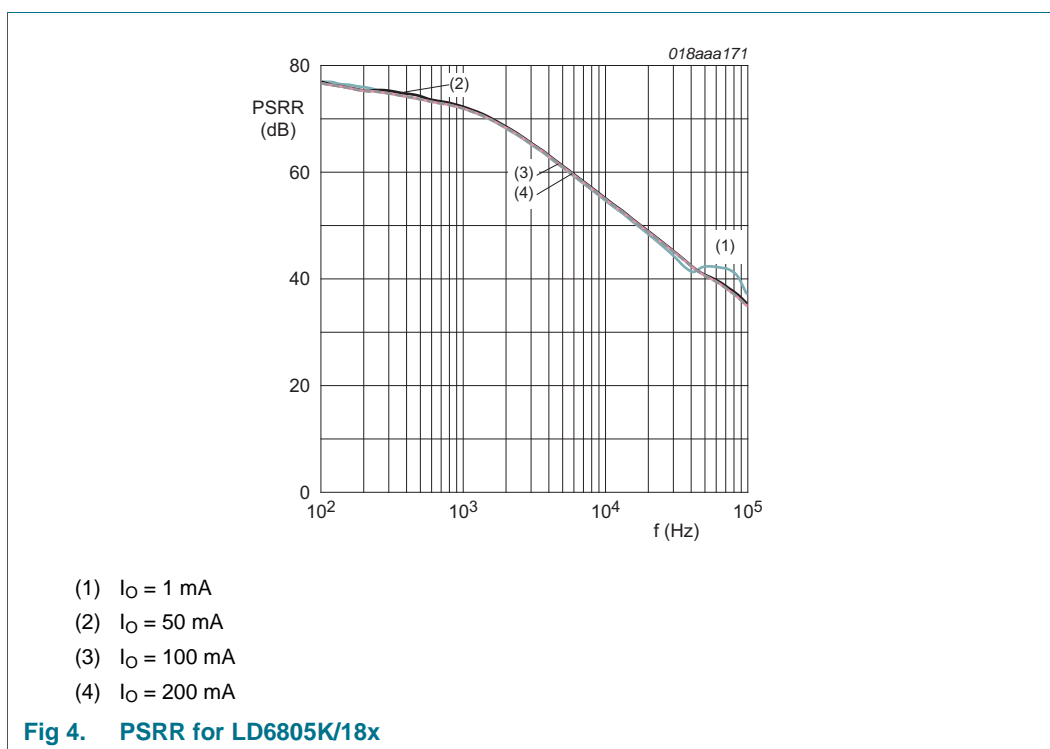
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Ripple rejection and output noise						
PSRR	power supply rejection ratio	$V_I = V_{O(nom)} + 1.0\text{ V}$; $I_O = 50\text{ mA}$; $f_{ripple} = 1\text{ kHz}$	-	75	-	dB
$V_{n(o)(RMS)}$	RMS output noise voltage	$f_{ripple} = 10\text{ Hz to }100\text{ kHz}$; $C_{L(ext)} = 1\text{ }\mu\text{F}$	-	40	-	μV
Enable input and timing						
V_{IL}	LOW-level input voltage	pin EN	0	-	0.4	V
V_{IH}	HIGH-level input voltage	pin EN	1.1	-	5.5	V
$t_{startup(reg)}$	regulator start-up time	$V_I = 5.5\text{ V}$; $V_O = 0.95 \times V_{O(nom)}$; $I_O = 150\text{ mA}$; $C_{L(ext)} = 1\text{ }\mu\text{F}$	-	150	-	μs
LD6805K/xxP; auto discharge function						
$t_{sd(reg)}$	regulator shutdown time	$V_I = 5.5\text{ V}$; $V_O = 0.05 \times V_{O(nom)}$; $C_{L(ext)} = 1\text{ }\mu\text{F}$	-	300	-	μs
R_{pd}	pull-down resistance		-	100	-	Ω

9. Dynamic behavior

9.1 Power Supply Rejection Ratio (PSRR)

PSRR stands for the capability of the regulator to suppress unwanted signals on the input voltage like noise or ripples.

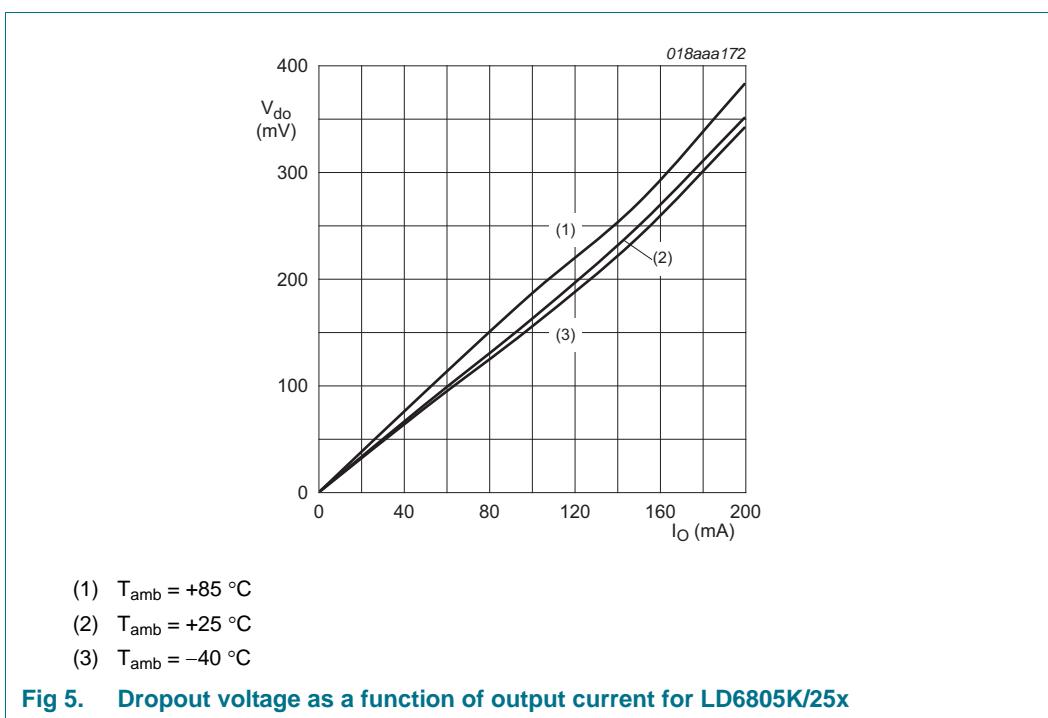
$$PSRR[dB] = (-20)\log \frac{V_{O(ripple)}}{V_{I(ripple)}} \quad \text{for all frequencies}$$



9.2 Dropout

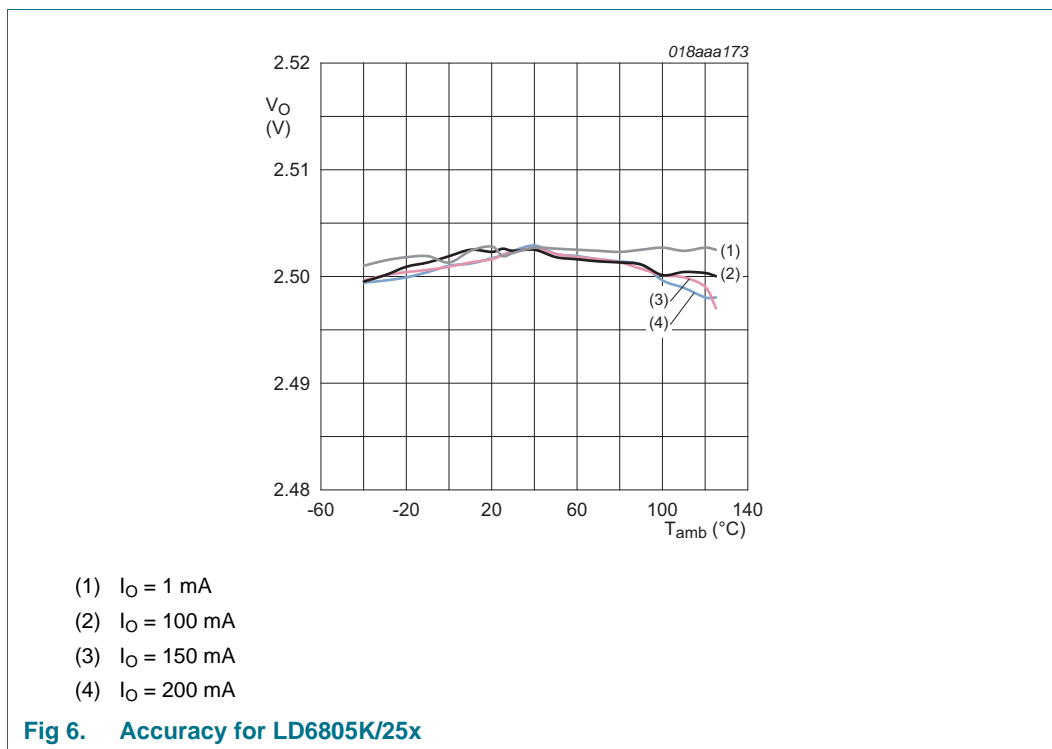
The dropout voltage is defined as the smallest input to output voltage difference at a specified load current when the regulator operates within its linear region. This means that the input voltage is below the nominal output voltage value and the pass transistor works as a plain resistor.

A small dropout voltage guarantees lower power consumption and efficiency maximization.



9.3 Accuracy

The LD6805 series guarantees high accuracy of the nominal output voltage.



10. Application information

10.1 Capacitor values

The LD6805 series requires external capacitors at the output to guarantee a stable regulator behavior. Do not under-run the specified minimum Equivalent Series Resistance (ESR). The absolute value of the total capacitance attached to the output pin OUT influences the shutdown time ($t_{sd(reg)}$) of the LD6805 series. Also an input capacitor is recommended to keep the input voltage stable.

Table 9. External load capacitor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{ext(IN)}$	external capacitance on pin IN	[1]	0.7	1.0		μF
$C_{L(ext)}$	external load capacitance	[1]	0.7	1.0	-	μF
ESR	equivalent series resistance		5	-	500	m Ω

[1] The minimum value of capacitance for stability and correct operation is 0.7 μF . The specified capacitor tolerance is $\pm 30\%$ or better over the temperature and operating conditions range. The recommended capacitor type is X7R to meet the full device temperature specification of $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$.

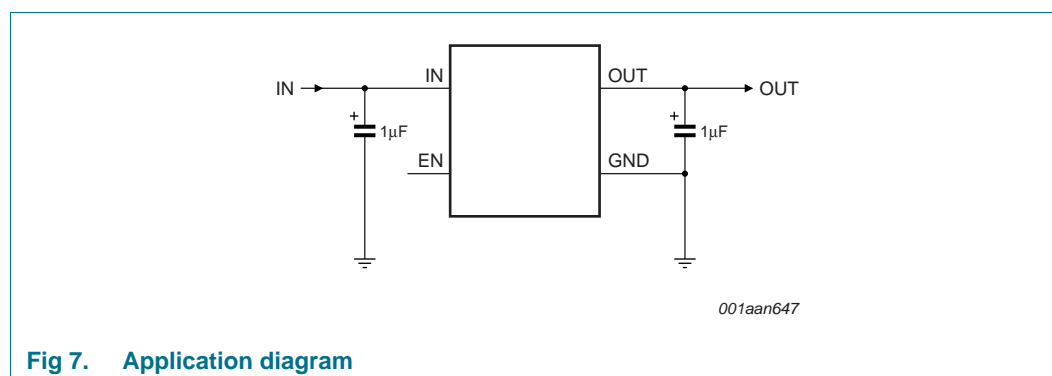


Fig 7. Application diagram

11. Test information

11.1 Quality information

This product has been qualified in accordance with *NX1-00023 NXP Semiconductors Quality and Reliability Specification* and is suitable for use in consumer applications.

12. Marking

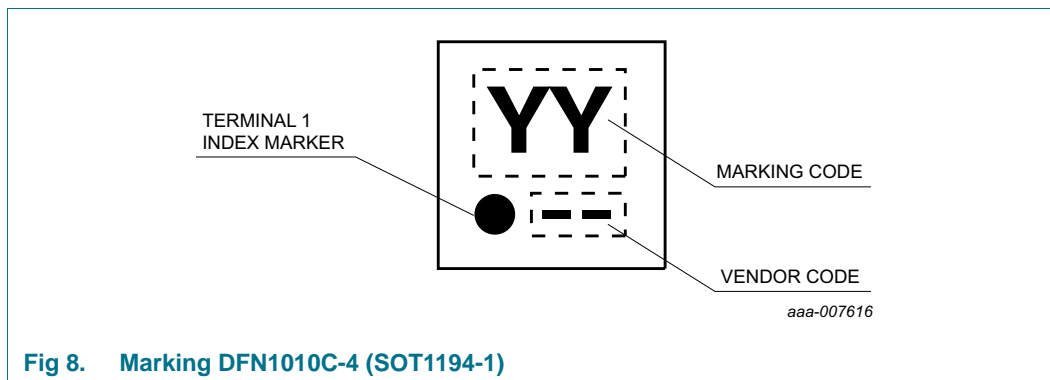


Table 10. Marking of high-ohmic output

Type number	Nominal output voltage $V_{O(nom)}$	Marking code	Type number	Nominal output voltage $V_{O(nom)}$	Marking code
LD6805K/12H	1.2 V	AH	LD6805K/22H	2.2 V	KH
LD6805K/13H	1.3 V	BH	LD6805K/23H	2.3 V	LH
LD6805K/14H	1.4 V	CH	LD6805K/25H	2.5 V	NH
LD6805K/15H	1.5 V	DH	LD6805K/28H	2.8 V	QH
LD6805K/16H	1.6 V	EH	LD6805K/29H	2.9 V	RH
LD6805K/18H	1.8 V	GH	LD6805K/30H	3.0 V	SH
LD6805K/185H	1.85 V	5H	LD6805K/31H	3.1 V	TH
LD6805K/20H	2.0 V	IH	LD6805K/33H	3.3 V	VH
LD6805K/21H	2.1 V	JH	LD6805K/36H	3.6 V	YH

Table 11. Marking of pull-down output

Type number	Nominal output voltage $V_{O(nom)}$	Marking code	Type number	Nominal output voltage $V_{O(nom)}$	Marking code
LD6805K/12P	1.2 V	AP	LD6805K/23P	2.3 V	LP
LD6805K/13P	1.3 V	BP	LD6805K/25P	2.5 V	NP
LD6805K/14P	1.4 V	CP	LD6805K/25P	2.5 V	NP
LD6805K/15P	1.5 V	DP	LD6805K/26P	2.6 V	OP
LD6805K/16P	1.6 V	EP	LD6805K/29P	2.9 V	RP
LD6805K/18P	1.8 V	GP	LD6805K/30P	3.0 V	SP
LD6805K/20P	2.0 V	IP	LD6805K/31P	3.1 V	TP
LD6805K/21P	2.1 V	JP	LD6805K/33P	3.3 V	VP
LD6805K/22P	2.2 V	KP	LD6805K/36P	3.6 V	YP

13. Package outline

Plastic thermal enhanced ultra thin small outline package; no leads;
4 terminals; body 1 x 1 x 0.55 mm

SOT1194-1

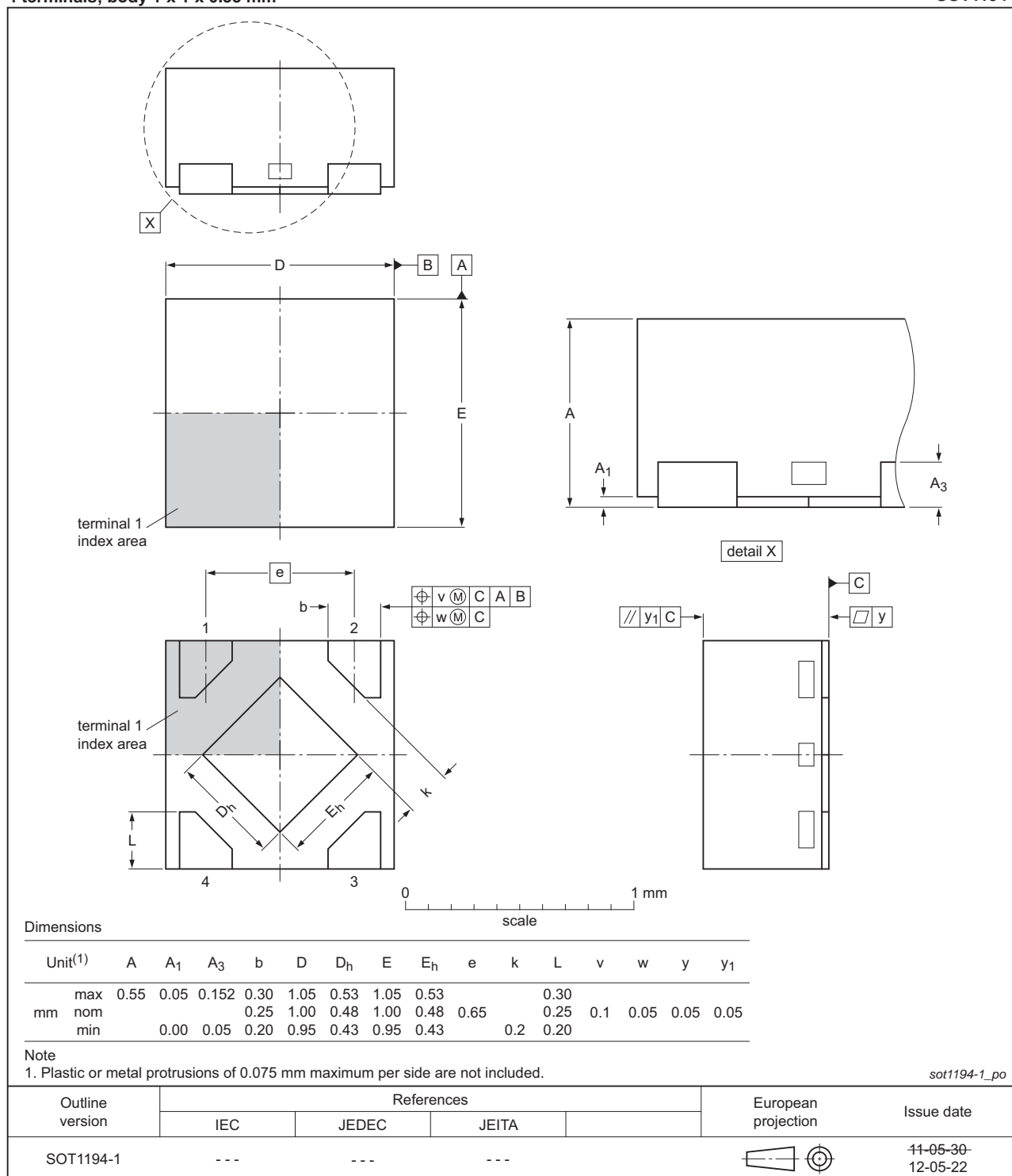


Fig 9. Package outline DFN1010C-4 (SOT1194-1)

14. Packing information

14.1 Packing methods

Table 12. Packing methods

Type number	Package	Description	Orientation [1]	12NC ending	Packing quantity
LD6805K	DFN1010C-4 (SOT1194-1)	2 mm pitch, 8 mm tape and reel	Q1	115	10000

[1] For further information about orientation, see [Section 14.2](#).

14.2 Carrier tape information

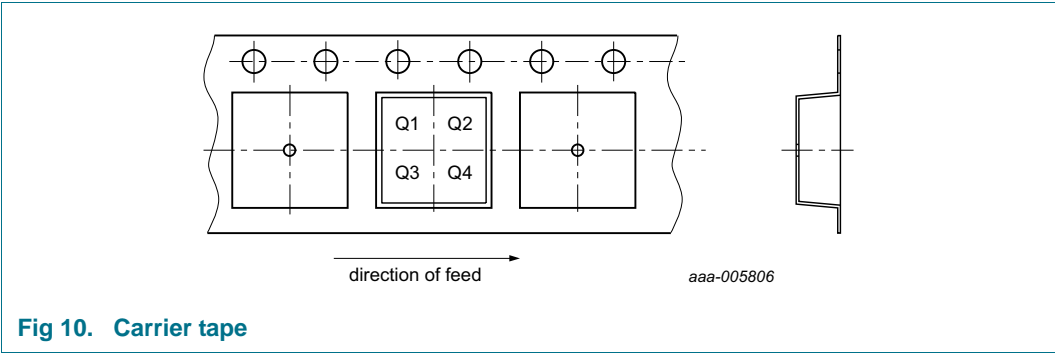


Table 13. Orientations

Orientation	Meaning	Pin 1 location
Q1	quadrant 1	upper left
Q2	quadrant 2	upper right
Q3	quadrant 3	lower left
Q4	quadrant 4	lower right

15. Soldering

Footprint information for reflow soldering of HXSON4 package

SOT1194-1

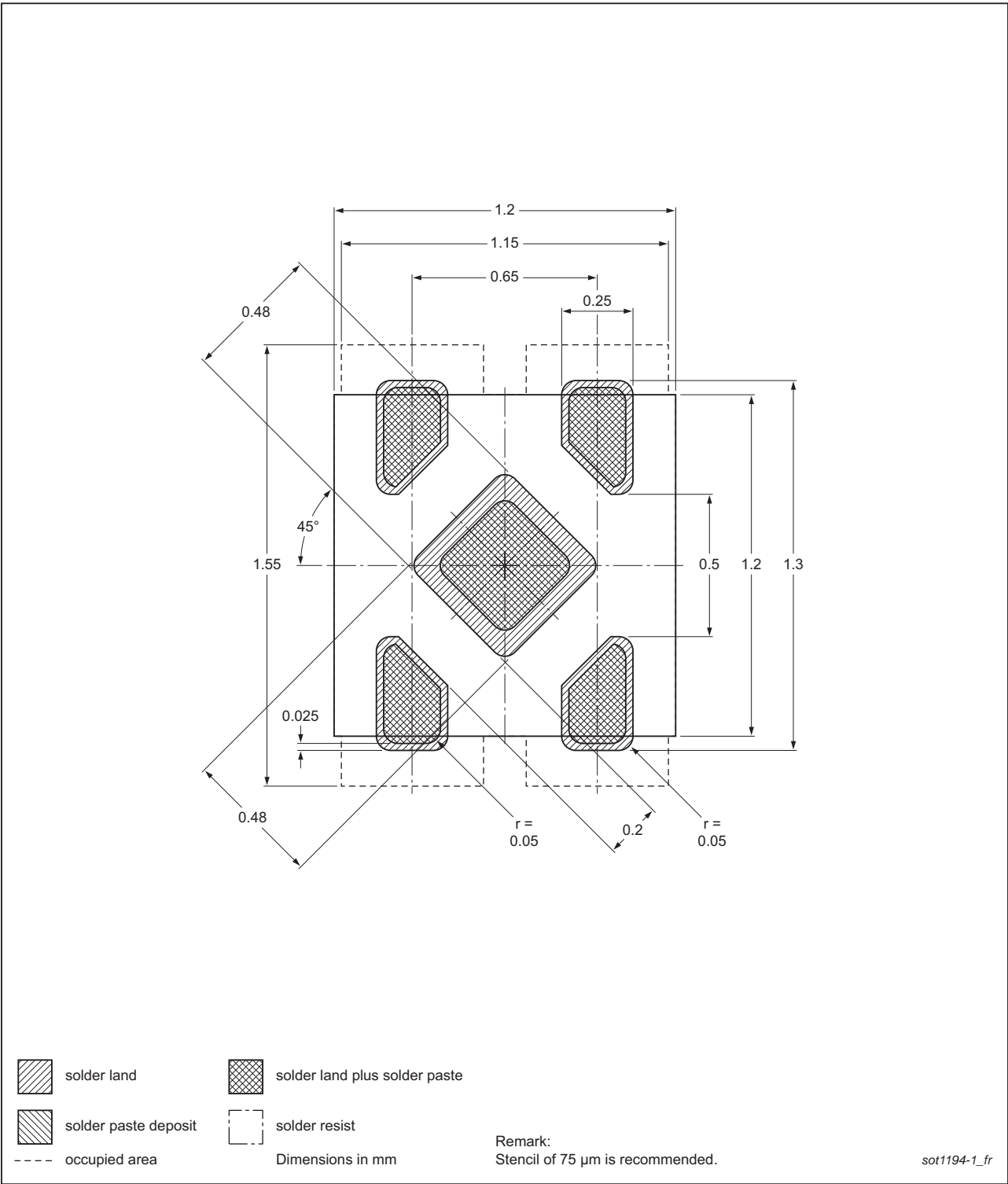


Fig 11. Soldering footprint DFN1010C-4 (SOT1194-1)

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 12](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 14](#) and [15](#)

Table 14. SnPb eutectic process (from J-STD-020D)

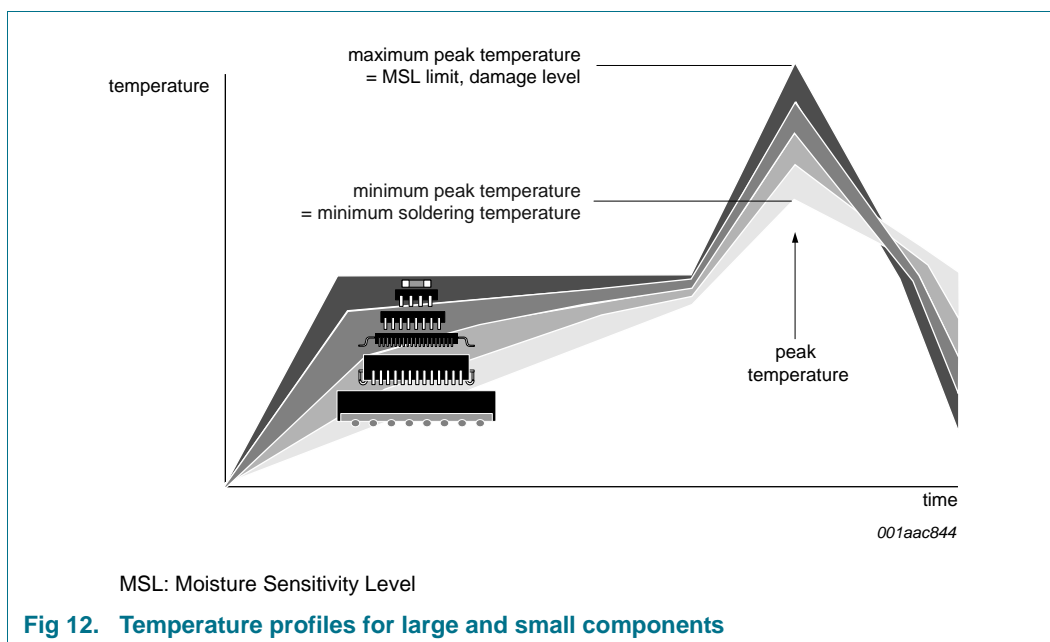
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 15. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 12](#).



For further information on temperature profiles, refer to Application Note *AN10365* "Surface mount reflow soldering description".

17. References

- [1] **IEC 60134** — Rating systems for electronic tubes and valves and analogous semiconductor devices
- [2] **IEC 61340-3-1** — Methods for simulation of electrostatic effects - Human body model (HBM) electrostatic discharge test waveforms
- [3] **JESD22-A115C** — Electrostatic discharge (ESD) Sensitivity Testing Machine Model (MM)
- [4] **NX2-00001** — NXP Semiconductors Quality and Reliability Specification
- [5] **AN10365** — Surface-mount reflow soldering description

18. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LD6805_SER v.4	20130607	Product data sheet	-	LD6805_SER v.3
Modifications:	<ul style="list-style-type: none">• Added type number LD6805K/26P• Section 1.2 “Features and benefits”: updated• Section 9.1 “Power Supply Rejection Ratio (PSRR)”: corrected equation			
LD6805_SER v.3	20130503	Product data sheet	-	LD6805_SER v.2
LD6805_SER v.2	20120625	Product data sheet	-	LD6805_SER v.1
LD6805_SER v.1	20110922	Objective data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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