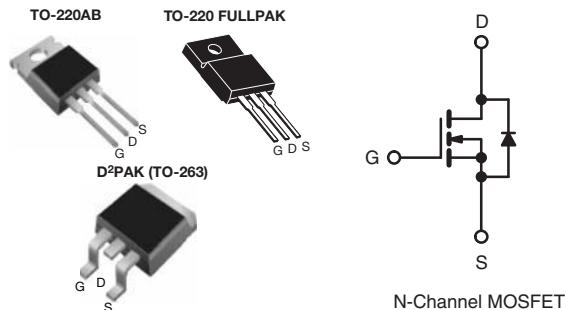


Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V) at T_J max.	560
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V 0.38
Q_g (Max.) (nC)	68
Q_{gs} (nC)	17.6
Q_{gd} (nC)	21.8
Configuration	Single



FEATURES

- Low Figure-of-Merit $R_{on} \times Q_g$
- 100 % Avalanche Tested
- Gate Charge Improved
- T_{rr}/Q_{rr} Improved
- Compliant to RoHS Directive 2002/95/EC


RoHS*
COMPLIANT

Note

* Pb containing terminations are not RoHS compliant, exemptions may apply

ORDERING INFORMATION			
Package	TO-220AB	D²PAK (TO-263)	TO-220 FULLPAK
	SiHP16N50C-E3	SiHB16N50C-E3	SiHF16N50C-E3
Lead (Pb)-free	-	SiHB16N50CTR-E3	-
	-	SiHB16N50CTL-E3	-

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 30	
Continuous Drain Current ($T_J = 150$ °C) ^a		V_{GS} at 10 V	$T_C = 25$ °C $T_C = 100$ °C	A
			16	
			10	
Pulsed Drain Current ^c		I_{DM}	40	
Linear Derating Factor			2	W/°C
Single Pulse Avalanche Energy ^b		E_{AS}	320	mJ
Maximum Power Dissipation		P_D	250	W
			38	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) ^d			300	

Notes

- Limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 2.5$ mH, $R_g = 25$ Ω , $I_{AS} = 16$ A.
- Repetitive rating; pulse width limited by maximum junction temperature.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TO220-AB D ² PAK (TO-263)	TO-220 FULLPAK	UNIT
Maximum Junction-to-Ambient	R _{thJA}	62	65	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	0.5	3.3	
Junction-to-Ambient (PCB mount) ^a	R _{thJA}	40	-	

Note

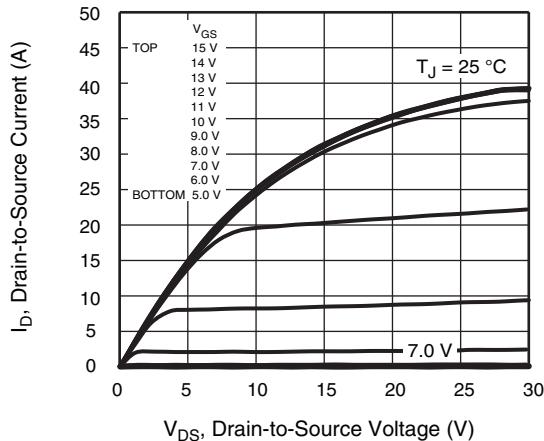
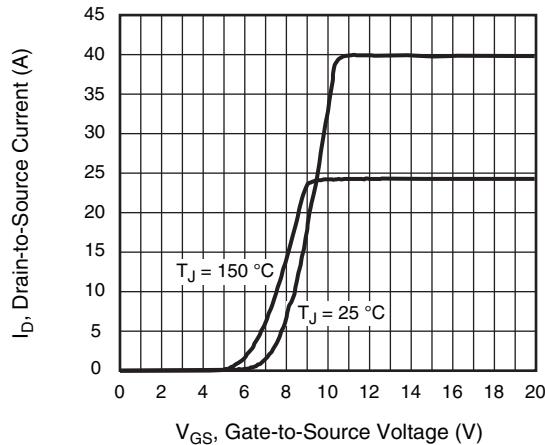
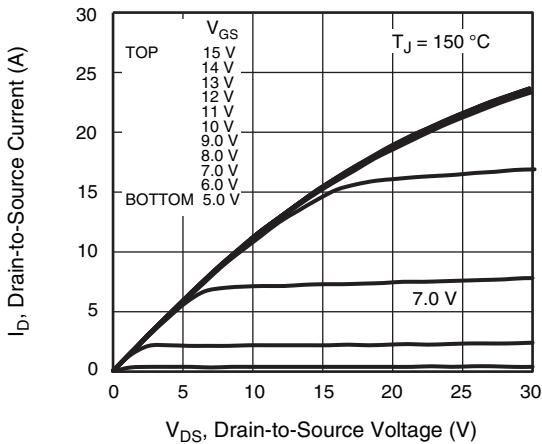
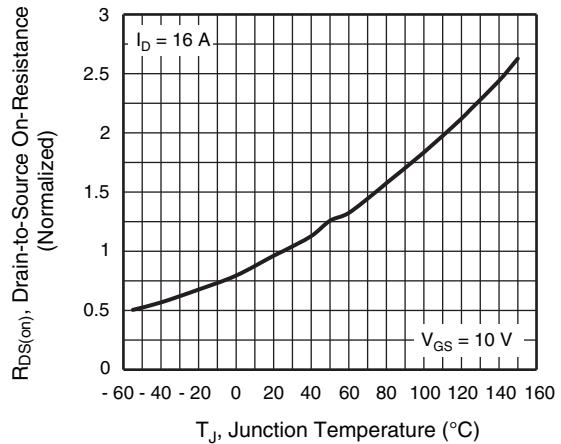
a. When mounted on 1" square PCB (FR-4 or G-10 material).

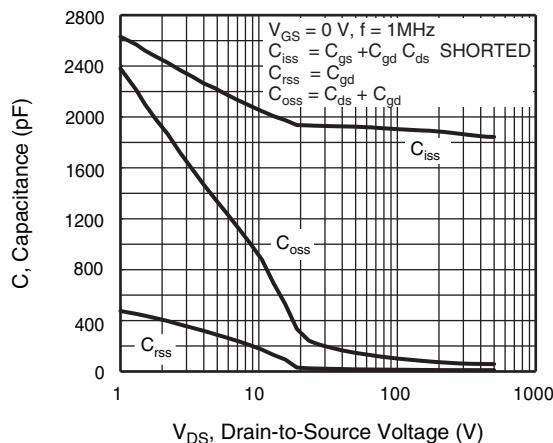
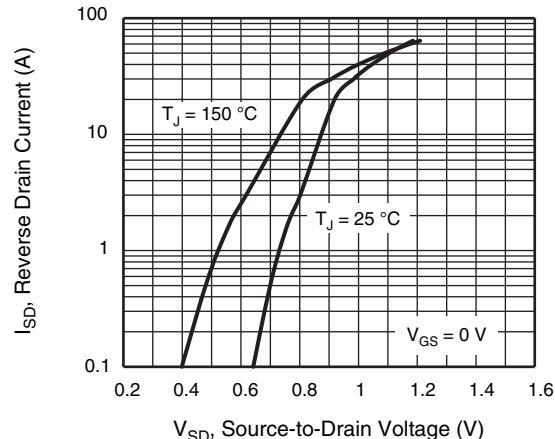
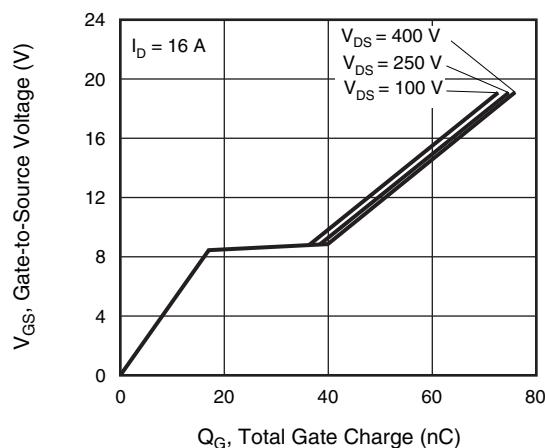
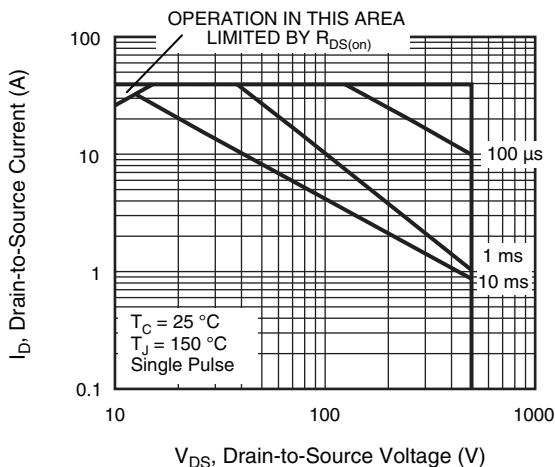
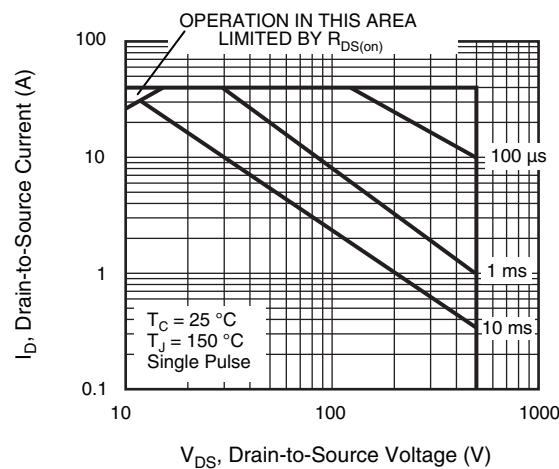
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

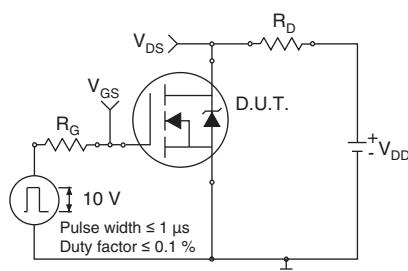
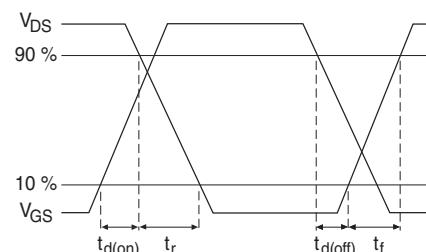
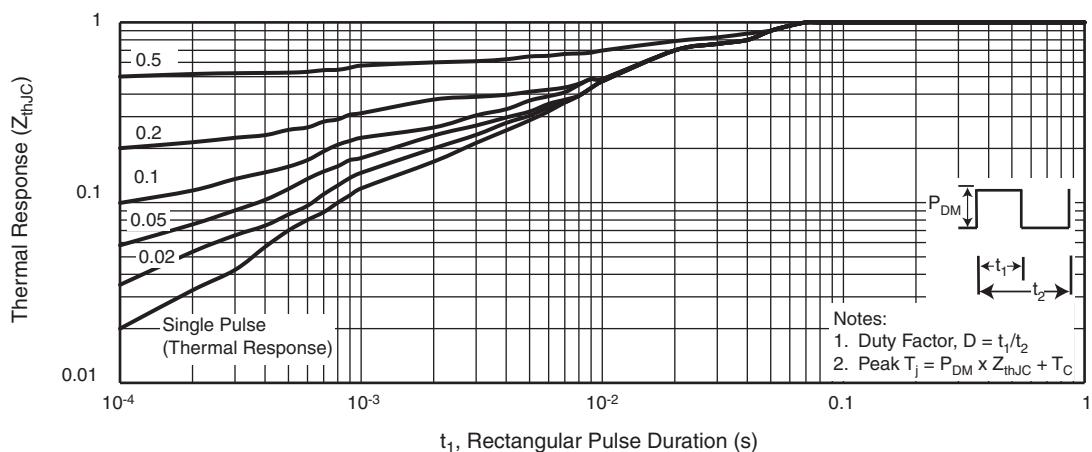
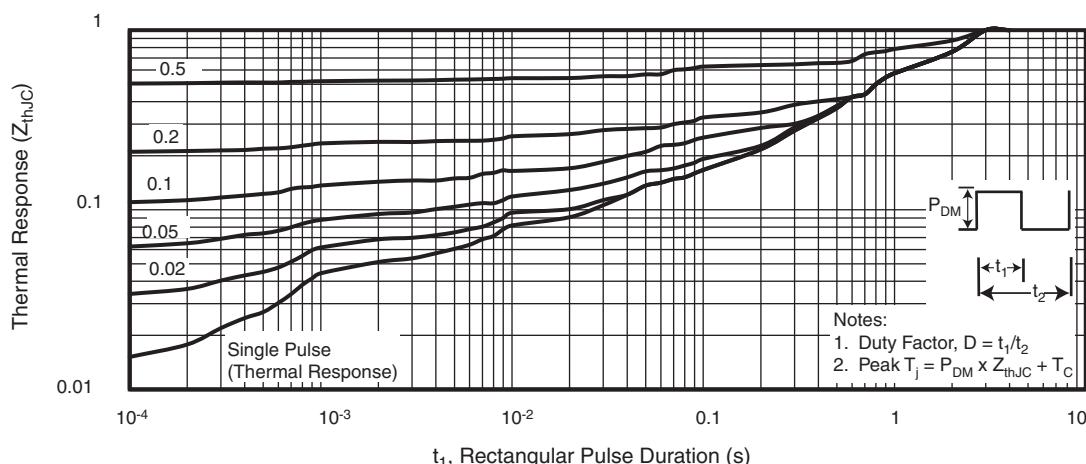
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.6	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3.0	-	5.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	50	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 8 A	-	0.31	0.38	Ω
Forward Transconductance ^a	g _f	V _{DS} = 50 V, I _D = 3 A		-	3	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz		-	1900	-	pF
Output Capacitance	C _{oss}			-	230	-	
Reverse Transfer Capacitance	C _{rss}			-	24	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 16 A, V _{DS} = 400 V	-	45	68	nC
Gate-Source Charge	Q _{gs}			-	18	-	
Gate-Drain Charge	Q _{gd}			-	22	-	
Turn-On Delay Time	t _{d(on)}			-	27	-	
Rise Time	t _r	V _{DD} = 250 V, I _D = 16 A, R _g = 9.1 Ω, V _{GS} = 10 V		-	156	-	ns
Turn-Off Delay Time	t _{d(off)}		-	29	-		
Fall Time	t _f		-	31	-		
Gate Input Resistance	R _g	f = 1 MHz, open drain		-	1.6	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	16	A
Pulsed Diode Forward Current	I _{SM}			-	-	30	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 10 A, V _{GS} = 0 V		-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S , dI/dt = 100 A/μs, V _R = 20 V		-	555	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	5.5	-		
Body Diode Reverse Recovery Current	I _{RRM}		-	18	-	A	

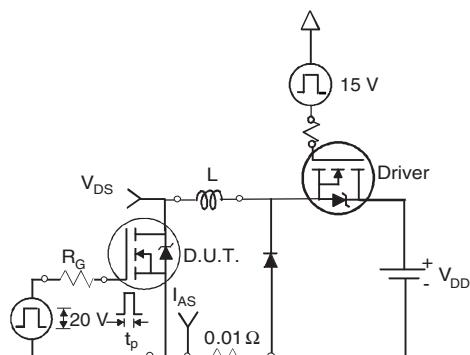
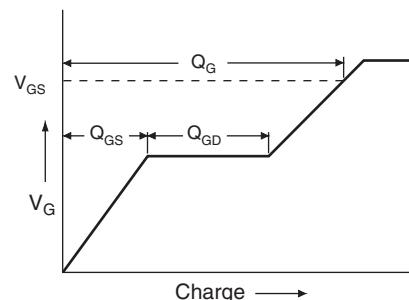
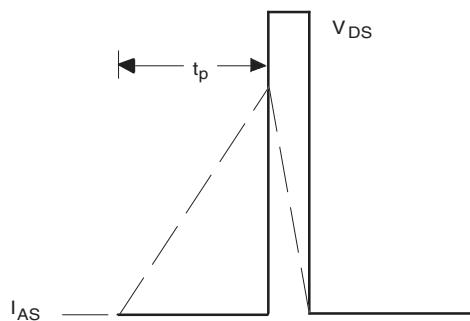
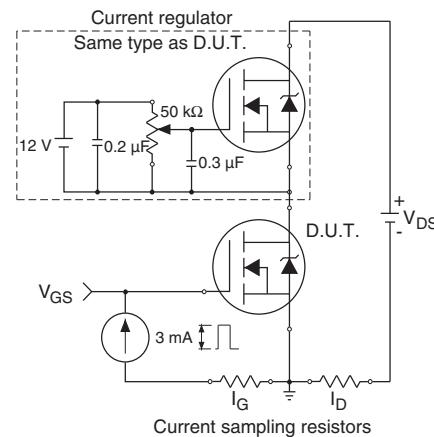
Note

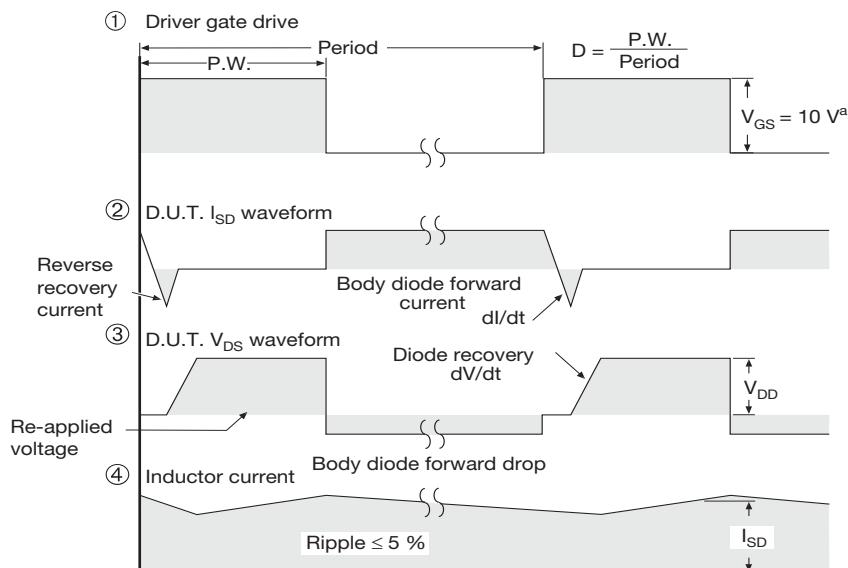
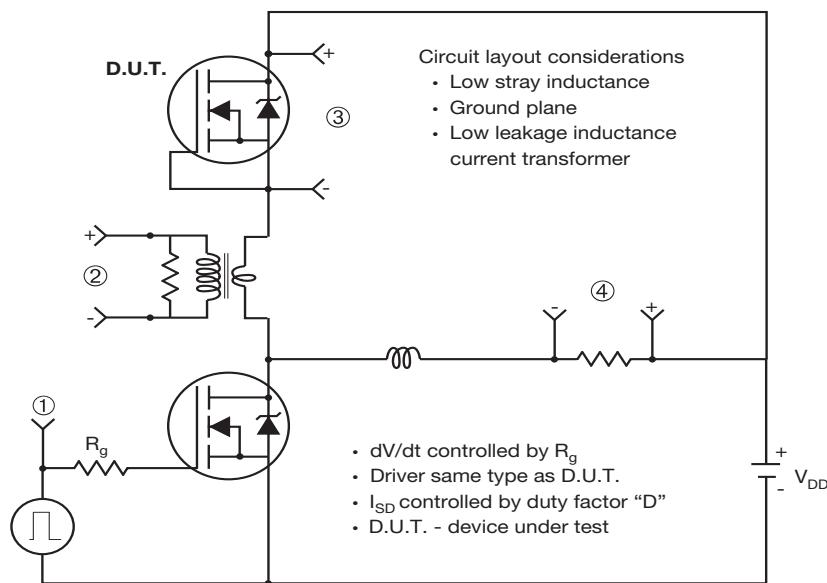
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics (TO-220)

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics (TO-220)

Fig. 4 - Normalized On-Resistance vs. Temperature


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area (TO-220AB, D²PAK)

Fig. 9 - Maximum Safe Operating Area (TO-220 FULLPAK)


Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220AB, D²PAK)

Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220 FULLPAK)


Fig. 13a - Unclamped Inductive Test Circuit

Fig. 14a - Basic Gate Charge Waveform

Fig. 13b - Unclamped Inductive Waveforms

Fig. 14b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

Note

a. $V_{GS} = 5 \text{ V}$ for logic level devices

Fig. 15 - For N-Channel

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